Genesys Logic, Inc.

GL3220

USB 3.0 Multi-LUN
Memory Card Reader Controller

Datasheet

Revision 1.31
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Revision History

Revision	Date	Description
1.00	03/16/2011	First formal release
1.10	03/28/2011	1. Modified 3.2 Pin descriptions, p.9 2. Add 5.4.1 Reset Timing, p.15 Add 5.4.2 SD/MMC Card Clock Frequency, p.16 Add 5.4.3 MS Card Clock Frequency, p.16
1.20	08/02/2011	1. Modified Chapter 1 – General Description, p.6 2. Modified Chapter 2 – Features, p.7 3. Modified Chapter 4.4 – MCU, p.13 4. Modified Chapter 4.5 – MHE (Media Hardware Engine), p.13 5. Modified Chapter 4.6 – Regulator, p.13 6. Modified Table 5.2 – Operating Conditions, p.14 7. Modified Table 5.5 – SD/MMC Card Clock Frequency, p.16 8. Modified Table 6.1 – SPI NOR Flash Support List, p.17
1.30	04/25/2013	1. Modified Chapter 2 – MMC v4.5, WHCK, WHQL ID, p.7 2. Modified Table 3.1 – Pin Description, p.11 3. Modified Chapter 5.1, 5.2, p14 4. Add Note in Table 5.5 – SD/MMC Card Clock Frequency, p16 5. Add PCT SPI Flash in Chapter 6, p.17
1.31	04/11/2016	Update CH2 Features

Table of Contents

List of Figures

List of Tables

CHAPTER 1 GENERAL DESCRIPTION

GL3220 is a super speed USB 3.0 compliant Mulit-LUN card reader controller which can support various types of memory cards, such as CompactFlash™, Secure Digital™ (SD), SDHC, miniSD, microSD (T-Flash), MultiMediaCard™ (MMC), RS-MMC, MMCmicro, MMCmobile, Memory Stick™ (MS), Memory Stick Duo™ (MS Duo), High Speed Memory Stick™ (HS MS), Memory Stick PRO™ (MS PRO), Memory Stick PRO™ Duo (MS PRO Duo), Memory Stick PRO-HG™ (MS PRO-HG), MS PRO Micro and xD-picture card on one chip. It also supports next generation high density memory cards (Capacity up to 2TB), such as SDXC and Memory Stick XC, and next generation high speed memory cards, SD3.0 UHS-I cards.

The GL3220 integrates a high speed 8051 microprocessor and a high efficiency hardware engine for the best data transfer performance between USB and various memory card interfaces. It supports ISP (In System Programming) for firmware upgrade from the external SPI Flash via USB port. It also integrates 5V to 3.3V and 3.3V to 1.2V regulators and power MOSFETs which can reduce the system BOM cost.

CHAPTER 2 FEATURES

- USB specification compliance
  - Comply with Universal Serial Bus 3.0 Specification rev. 1.0 (USB 3.0)
  - Comply with Universal Serial Bus Specification rev. 2.0 (USB 2.0)
  - Comply with USB Mass Storage Class Specification rev. 1.0
  - Support USB Mass Storage Class Bulk-Only Transport (BOT)
  - Support 1 device address and up to 4 endpoints: Control (0) / Bulk Data Write Out (1) / Bulk Data Read In (2) / Interrupt In (3)
  - Support 5 Gbps SuperSpeed, 480 Mbps high-speed, and 12 Mbps full-speed transfer rates
- Integrated USB building blocks
  - USB2.0 transceiver macro (UTM), Serial Interface Engine (SIE), embedded Power-On Reset (POR)
- Embedded high speed 8051 micro-controller
- High efficient DMA hardware engine improves transfer rate between USB and flash card interfaces
- Support CompactFlash™ v6.0 with PIO mode 6 / Ultra DMA mode 7 and LBA48 (Capacity up to 144PB)
- Support Ssecure Digital™ v1.0 / v1.1 / v2.0/ SDHC / SDXC (Capacity up to 2TB)
- Support Secure Digital™ v3.0 UHS-I (Ultra High Speed): SDR12/SDR25/SDR50/DDR50/SDR104
- Support Secure Digital™ v5.0
- Compliant with MultiMediaCard™ (MMC)
  - MMC specification v3.x / v4.0 / v4.1 / v4.2 / v4.3 / v4.4 / v4.5
  - x1 / x4 / x8 bit data bus
- Support Memory Stick™ / Memory Stick PRO / Memory Stick PRO Duo / Memory Stick Micro /Memory Stick PRO-HG / Memory Stick XC (Capacity up to 32GB)
  - Compliant with Memory Stick Series Specification: MS v1.43, MS PRO v1.05, MS Micro v1.04 (MS HG Micro v1.00), MS PRO-HG Duo 1.03, MS XC Duo v1.00, MS XC-HG Duo v1.00, MS XC Micro v1.00 and MS XC-HG Micro v1.00
  - Support Read/Write quad data access (512Bytex4) for MS PRO-HG to enhance the transmission rate
- Support xD-PictureTM v1.2C Type M/H
- Support ISP (In System Programming) for firmware upgrade from the external SPI Flash via USB port
- On-Chip power MOSFETs for supplying flash media card power
- On-chip 5V to 3.3V and 3.3V to 1.2V regulator
- On board 25 MHz Crystal driver circuit
- Pass the USB-IF Test Procedure for SuperSpeed product, TID:340000020
- Pass WHCK (Windows Hardware Certification Kit) test for Windows 8 (Submission ID: 1511499)
- Pass WHCK (Windows Hardware Certification Kit) test for Windows 8 ARM (Submission ID: 1551618)
- Pass WHQL (Windows Hardware Quality Lab) test for Windows 7 (Submission ID: 1439281)
- Package available in 128 pin LQFP that can support 5 LUNs: CF, SD, MS, xD and microSD/M2

CHAPTER 3 PIN ASSIGNMENT

3.1 LQFP 128 Pinout

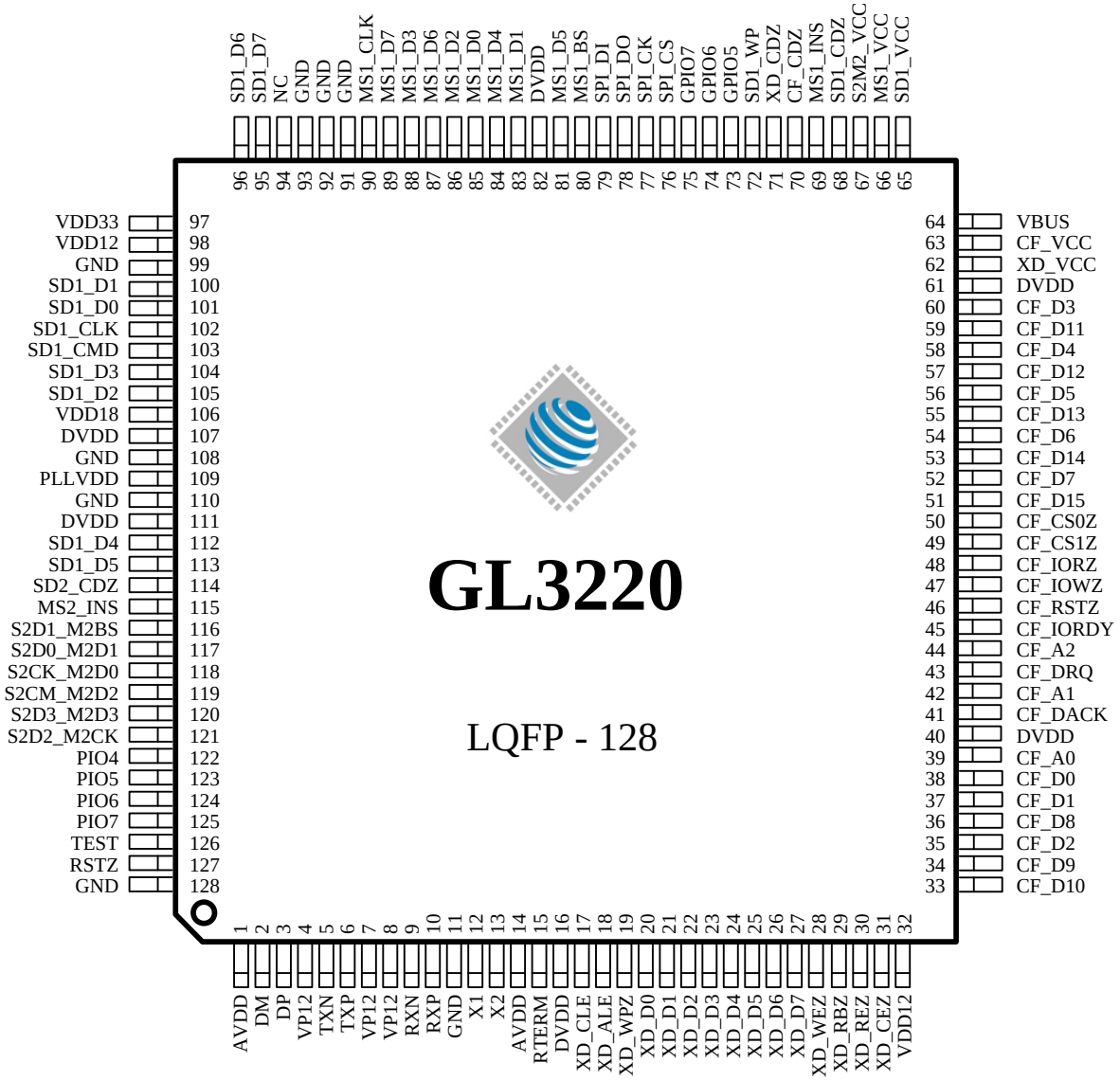

Figure 3.1 - LQFP 128 Pinout Diagram

3.2 Pin Description

Table 3.1 - Pin Description

Pin Name	LQFP 128 pin	Type	Description
Power/Ground			
AVDD	1,14	P	3.3V Analog power
DVDD	16,40,61,82,107, 111	P	3.3V Digital power
PLLVDD	109	P	3.3V PLL power
VP12	4,7,8	P	1.2V Analog power
VDD12	32,98	P	1.2V Core power
VDD18	106	P	SD 3.0 IO PAD Power, the power source of this pin comes from the internal regulator of GL3220 and no need of external 1.8V power input
VDD33	97	P	3.3V to 1.2V regulator power
VBUS	64	P	5V Power source
XD_VCC	62	P	xD card power
CF_VCC	63	P	CF card power
SD1_VCC	65	P	SD card power
MS1_VCC	66	P	MS card power
S2M2_VCC	67	P	microSD/M2 card power
GND	11,91,92,93,99, 108,110,128	P	Ground
USB PHY Interface			
DM	2	A	USB 2.0 D-
DP	3	A	USB 2.0 D+
TXN	5	A	USB 3.0 TX-
TXP	6	A	USB 3.0 TX+
RXN	9	A	USB 3.0 RX-
RXP	10	A	USB 3.0 RX+
RTERM	15	A	USB reference resistor. This pin is used to control the level of USB signal. A 680ohm, 1% resistor is recommended to be laid between RREF and GND
X1	12	I	25MHz XTAL input. It can be connected to external 25MHz clock input
X2	13	B	25MHz XTAL output
Memory Card Interface			
CF_CDZ	70	I, pu	CF card detect 0: Card insert 1: No card
CF_D[15:0]	51,53,55,57,59, 33,34,36,52,54, 56,58,60,35,37, 38	B	CF data pins

CF_CS0Z	50	O	CF chip select 0
CF_CS1Z	49	O	CF chip select 1
CF_IORZ	48	O	CF IO read
CF_IOWZ	47	O	CF IO write
CF_RSTZ	46	O	CF reset
CF_IORDY	45	I, pd	CF IO ready
CF_DRQ	43	I, pd	CF DMA request
CF_DACK	41	O	CF DMA acknowledge
CF_A[2:0]	44,42,39	O	CF address
XD_D[7:0]	27,26,25,24,23, 22,21,20	B	xD data pins
XD_WPZ	19	O	xD write protect
XD_WEZ	28	O	xD write enable
XD_ALE	18	O	xD_ALE
XD_CLE	17	O	xD command latch enable
XD_CEZ	31	O	xD card enable
XD_REZ	30	O	xD read enable
XD_RBZ	29	I, pu	xD read/busy
XD_CDZ	71	I, pu	xD card detect 0: Card insert 1: No card
SD1_WP	72	I, pu	SD write protect 0: write enable 1: write protection
SD_CDZ	68	I, pu	SD card detect 0: Card insert 1: No card
SD1_D[7:0]	95,96,113,112, 104,105,100,101	B	SD data pins
SD1_CLK	102	O	SD clock
SD1_CMD	103	B,pu	SD command/response
MS1_BS	80	O	MS/MSP bus state
MS1_INS	69	I, pu	MS insertion detect 0: Card insert 1: No card
MS1_D[7:0]	89,87,81,84,88, 86,83,85	B	MS/MSP data signal
MS1_CLK	90	O	MS clock
SD2_CDZ	114	I, pu	SD card detect 0: Card insert 1: No card
MS2_INS	115	I, pu	MS insertion detect 0: Card insert 1: No card
S2D1_M2BS	116	B	SD data pin

		O	MS/MSP bus state
S2D0_M2D1	117	B	SD data pin
		B	MS/MSP data signal
S2CK_M2D0	118	O	SD clock (SD High Speed Mode, 50MHz max.)
		B	MS/MSP data signal
S2CM_M2D2	119	B,pu	SD command/response
		B	MS/MSP data signal
S2D3_M2D3	120	B	SD data pin
		B	MS/MSP data signal
S2D2_M2CK	121	B	SD data pin
		O	MS clock
Others			
GPIO[7:5]	75,74,73	B	Hardware configuration
PIO[7:4]	125,124,123,122	B	Hardware configuration
SPI_CS	76	O	SPI interface: chip select
SPI_CK	77	O	SPI interface: clock
SPI_DO	78	O	SPI interface: data output
SPI_DI	79	I	SPI interface: data input
TEST	126	I, pd	Test mode
RSTZ	127	I, pu	System reset, active low

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	pu	internal pull-up when input
	pd	internal pull-down when input
	P	Power / Ground
	A	Analog

CHAPTER 4 BLOCK DIAGRAM

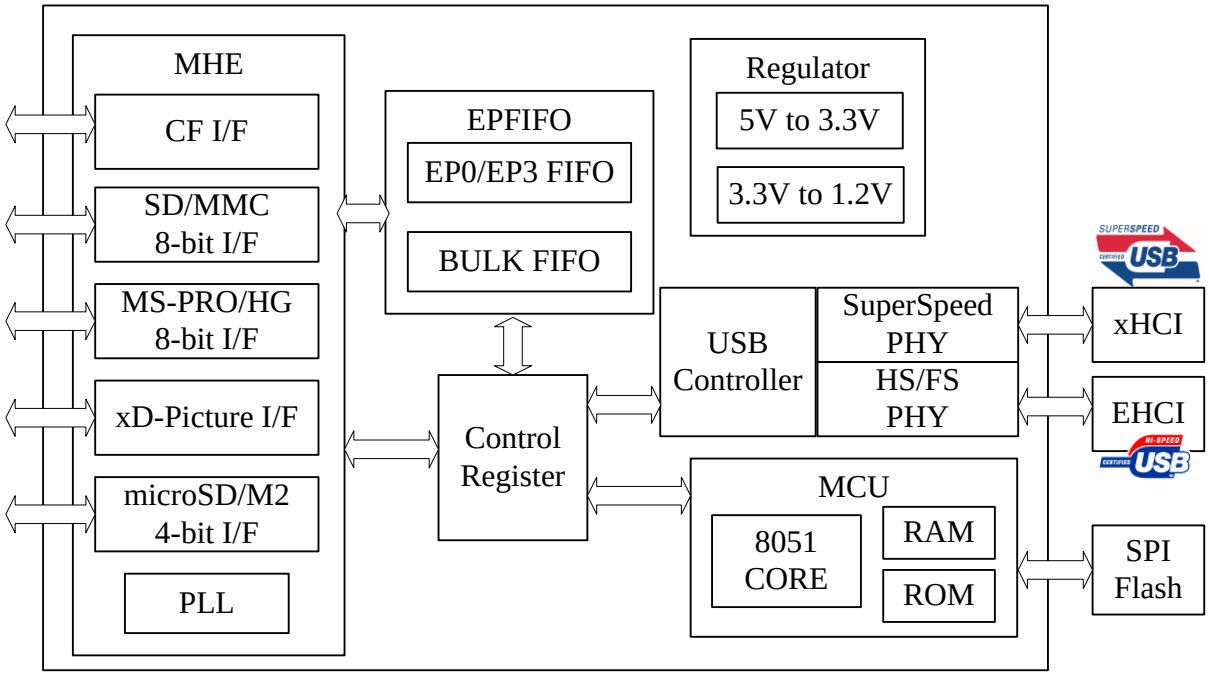

Figure 4.1 - Functional Block Diagram

4.1 Super Speed and HS/FS PHY

The transceiver macro cell is the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB to one that is compatible with the general logic.

4.2 USB Controller

The USB Controller, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

4.3 EPFIFO

Endpoint FIFO includes Control FIFO (FIFO0), Interrupt FIFO (FIFO3), Bulk In/Out FIFO

- **EP0 FIFO** FIFO of control endpoint 0. It is 512-byte FIFO and used for endpoint 0 data transfer.
- **EP3 FIFO** 32-byte depth FIFO of endpoint 3 for status interrupt
- **Bulk In/Out FIFO** It can be in the TX mode or RX mode:
  1. It can be transmit/receive 512-byte data of USB 2.0 and 1K-byte data of USB 3.0 continuously.
  2. It can be directly accessed by micro-controller

4.4 MCU

8051 micro-controller inside.

- **8051 Core** Compliant with Intel 8051 high speed micro-controller
- **ROM** Firmware code on ROM
- **SRAM** Internal RAM area for MCU access

4.5 MHE (Media Hardware Engine)

Media Interface: CF/xD/SD/MMC/MS/MS PRO/MS PRO-HG

4.6 Regulator

- **5V to 3.3V** 3.3V Power Source
- **3.3V to 1.2V** 1.8V Power Source

CHAPTER 5 ELECTRICAL CHARACTERISTICS

5.1 Temperature Conditions

Table 5.1 - Temperature Conditions

Parameter	Value
Storage Temperature	-65°C to +150 °C
Operating Temperature	0°C to 70 °C

5.2 Operating Conditions

Table 5.2 - Operating Conditions

Parameter	Value
Supply Voltage	+4.75V to +5.25V
Ground Voltage	0V
F_{OSC} (Oscillator or Crystal Frequency)	25 MHz ± 0.03%

5.3 DC Characteristics

Table 5.3 - DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.75	-	5.25	V
V_{IH}	Input High Voltage		2.0	-	-	V
V_{IL}	Input Low Voltage		-	-	0.4	V
I_I	Input Leakage Current	$0 < V_{IN} <$ DVDD	-10	-	10	µA
V_{OH}	Output High Voltage	DVDD = 3.3V	3.0	-	-	V
V_{OL}	Output Low Voltage		-	-	0.4	V
I_{OH}	Output Current High		-	8	-	mA
I_{OL}	Output Current Low		-	8	-	mA
C_{IN}	Input Pin Capacitance		-	5	-	pF
I_{NORMAL}	HS mode		-	46	-	mA
	SS mode	U0 state	-	140	-	mA
		U1 state	-	30	-	mA
		U2 state	-	16	-	mA
I_{ACTIVE}	HS mode		-	63	-	mA
	SS mode	U0 state	-	160	-	mA
I_{RESET}			-	48	-	mA
I_{SUS}	Suspend current	1.5K pull-up included	-	1.6	-	mA

R_{pu}	Reset Pad pull-up		44	61	92	KΩ
	SD_CDZ, SD_WP, MS_INS, GPIO Pad pull-up		44	61	92	KΩ
	SD_CMD pull-up		-	15	-	KΩ
	SD_CLK, D[3:0] Pad pull-up		-	15	-	KΩ
R_{pd}	SD_CMD pull-down		-	15	-	KΩ
	SD_CLK, D[3:0] Pad pull-down		-	15	-	KΩ
R_{IMP}	SD_CMD, SD_CLK, D[3:0] impedances		-	56.6	-	Ω

5.4 AC Characteristics of Reset Timing

5.4.1 Reset Timing

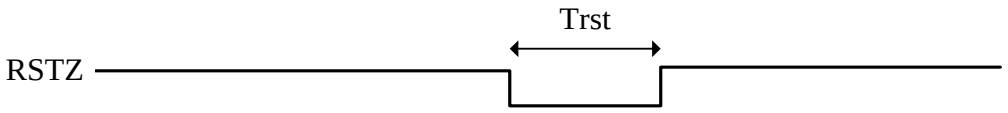

Figure 5.1 - Timing Diagram of Reset Width

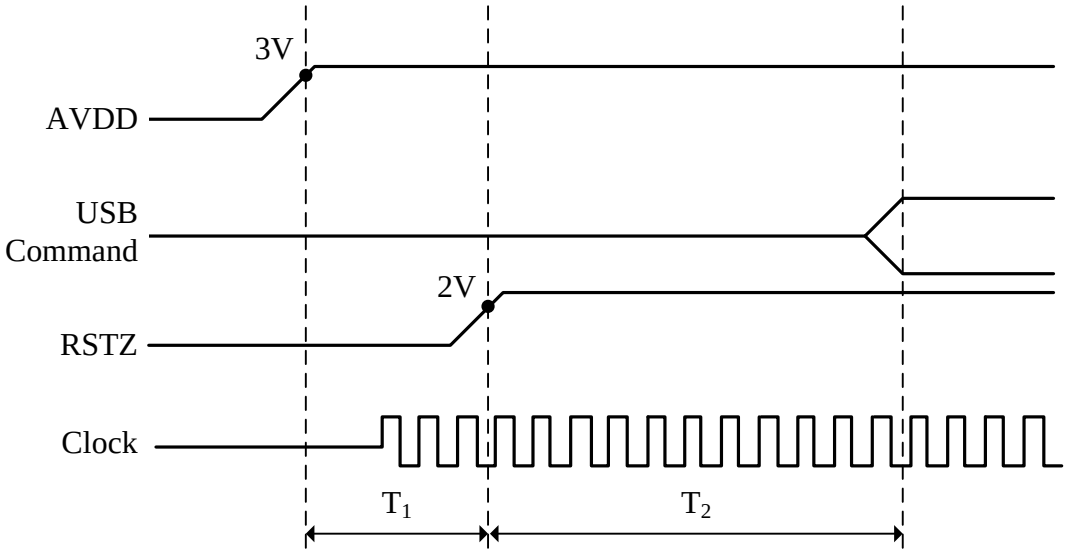

Figure 5.2 - Timing Diagram of Power Good to USB Command Receive Ready

Table 5.4 - Reset Timing

Parameter	Description	Min.	Unit
Trst	Chip reset sense timing width	2	us
T_1	AVDD power up to reset de-assert	500	us
T_2	Reset de-assert to respond USB command ready	80	ms

5.4.2 SD/MMC Card Clock Frequency

Table 5.5 - SD/MMC Card Clock Frequency

Parameter	Description	Max.	Unit
F_{ID}	Clock frequency Identification Mode	187	KHz
F_{DS}	Clock frequency Default Speed Mode	25	MHz
F_{HS}	SD Clock frequency High Speed Mode	50	MHz
F_{HS}	MMC Clock frequency High Speed Mode	52	MHz
F_{SDR25}	Clock frequency Ultra High Speed Mode: SDR25	50	MHz
F_{DDR50}	Clock frequency Ultra High Speed Mode: DDR50	50	MHz
F_{SDR50}	Clock frequency Ultra High Speed Mode: SDR50	100	MHz
F_{SDR104}	Clock frequency Ultra High Speed Mode: SDR104	208	MHz

Note: microSD interface support SD High Speed Mode, max. 50MHz

5.4.3 MS Card Clock Frequency

Table 5.6 - MS Card Clock Frequency

Parameter	Description	Typ.	Unit
F_{DS}	Clock frequency Default Speed Mode	20	MHz
F_{MSP}	Clock frequency MS PRO 4bit Mode	40	MHz
F_{MSPHG}	Clock frequency MS PRO HG 8bit Mode	60	MHz

CHAPTER 6 SPI NOR FLASH SUPPORT LIST

Table 6.1 - SPI NOR Flash Support List

Vendor	Model	
AMIC	A25L040	A25LS512
	A25L080	A25L016
	A25L032	
ATMEL	AT25F512B	
EON	EN25F10	
MXIC	MX25L5121E	MX25L6445E
	MX25L1021E	MX25L128451E
	MX25L1606E	MX25L8006E
PMC	PM25LV512A	PM25LD010
	PM25LV010A	PM25LD020
	PM25LV020	PM25LD512C
Sanyo	LE25FU206	
SST	SST25VF512	SST25LF020
	SST25VF010	SST25VF080B
	SST25VF016B	
ST	M25P05	M25P10
Winbond	W25X10A	W25X32A
	W25X20A	W25X80A
	W25X16A	
PCT	PCT25VF512	PCT25VF010

Note: To support ISP (In System Programming) for firmware upgrade from the external SPI Flash via USB port, the density of SPI NOR Flash shall be larger than or equal to 512Kb.

CHAPTER 7 PACKAGE DIMENSION

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A			1.60 (63)
A1	0.05 (2)		0.15 (6)
A2	1.35 (53)	1.40 (55)	1.45 (57)
b	0.13 (5)	0.18 (7)	0.23 (9)
c	0.09 (4)		0.20 (8)
D	16.00 (630) BSC		
D1	14.00 (551) BSC		
E	16.00 (630) BSC		
E1	14.00 (551) BSC		
e	0.40 (16) BSC		
L	0.45 (18)	0.60 (24)	0.75 (30)
L1	1.00 (39) REF		
Y			0.10 (4)
θ	0°	3.5°	7°

NOTE: 1. REFER TO JEDEC MS-026/BEE REV.B
2. ALL DIMENSIONS IN MILLIMETERS.

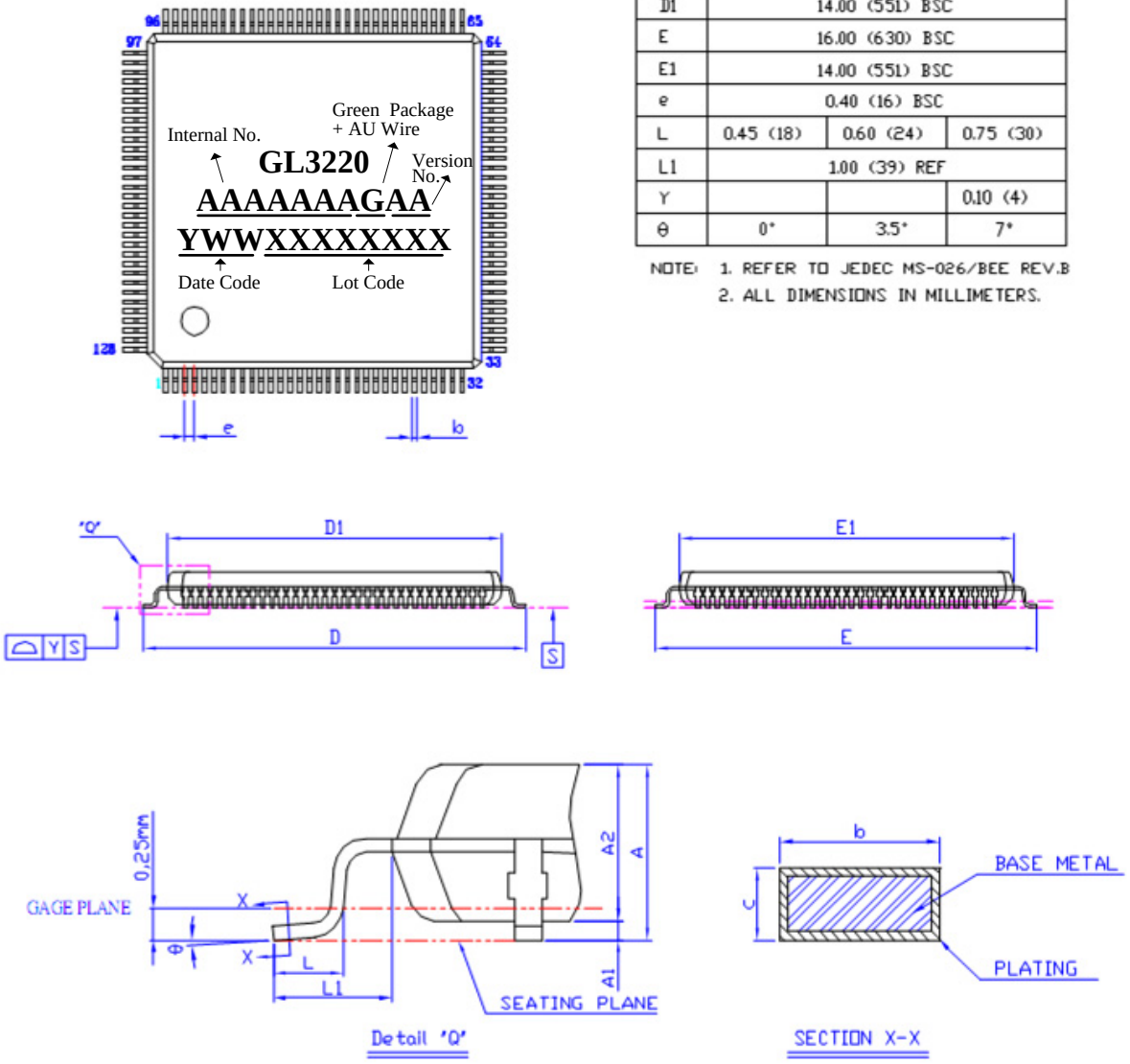

Figure 7.1 - LQFP 128 Pin Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Green/Wire Material	Version	Status
GL3220-MXGXX	LQFP 128	Green Package + AU Wire	XX	Available