Genesys Logic, Inc.

GL3221

USB 3.0 SD 3.0/MMC/MS
Memory Card Reader Controller

Datasheet

Revision 1.40
Oct. 12, 2011

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Revision History

Revision	Date	Description
1.00	03/22/2011	First formal release
1.10	03/28/2011	1. Modified 3.3 Pin descriptions, p.10 2. Add 4.1 ~ 4.6 Block diagram descriptions, p.12-13 3. Update 5.4 PMOS Characteristics, p.15 4. Add 5.5.1 ~5.5.3 timing and clock frequency, p.16-17
1.20	05/17/2011	Remove 5.5.1 Reset Timing
1.30	08/02/2011	1. Modified Chapter 1 – General Description, p.6 2. Modified Chapter 2 – Features, p.7 3. Modified Table 3.1 – Pin Description, p.10 4. Modified Chapter 4.4 – MCU, p.13 5. Modified Chapter 4.5 – MHE (Media Hardware Engine), p.13 6. Modified Chapter 4.6 – Regulator, p.13 7. Modified Table 5.2 – Operating Conditions, p.14 8. Modified Table 5.5 – SD/MMC Card Clock Frequency, p.16 9. Modified Table 6.1 – SPI NOR Flash Support List, p.17
1.40	10/12/2011	1. Add Table2.1 – GL3221 Dual LUNs Product Selection Guide

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CHAPTER 1 GENERAL DESCRIPTION

GL3221 is a super speed USB 3.0 compliant memory card reader controller which can support various types of memory cards, such as Secure Digital™ (SD), SDHC, SDXC, miniSD, microSD (T-Flash), MultiMediaCard™ (MMC), RS-MMC, MMCmicro, MMCmobile, Memory Stick™ (MS), Memory Stick Duo™ (MS Duo), High Speed Memory Stick™ (HS MS), Memory Stick PRO™ (MS PRO), Memory Stick PRO™ Duo (MS PRO Duo), Memory Stick PRO-HG™ (MS PRO-HG), MS PRO Micro and MS XC on one chip. It also supports next generation high density memory cards (Capacity up to 2TB), such as SDXC, and next generation high speed memory cards, SD3.0 UHS-I cards. GL3221 supports SD/MMC and MS separated data bus which can be configured as 1LUN (Logic Unit Number) or 2LUNs for the different applications.

GL3221 integrates a high speed 8051 microprocessor and a high efficiency hardware engine for the best data transfer performance between USB and various memory card interfaces. It supports ISP (In System Programming) for firmware upgrade from the external SPI Flash via USB port. It also integrates 5V to 3.3V and 3.3V to 1.2V regulators and power MOSFETs which can reduce the system BOM cost.

CHAPTER 2 FEATURES

- USB specification compliance
  - Comply with Universal Serial Bus 3.0 Specification rev. 1.0 (USB 3.0)
  - Comply with Universal Serial Bus Specification rev. 2.0 (USB 2.0)
  - Comply with USB Mass Storage Class Specification rev. 1.0
  - Support USB Mass Storage Class Bulk-Only Transport (BOT)
  - Support 1 device address and up to 4 endpoints: Control (0) / Bulk Data Write Out (1) / Bulk Data Read In (2) / Interrupt In (3)
  - Support 5 Gbps SuperSpeed, 480 Mbps high-speed, and 12 Mbps full-speed transfer rates
- Integrated USB building blocks
  - USB2.0 transceiver macro (UTM), Serial Interface Engine (SIE), embedded Power-On Reset (POR)
- Embedded high speed 8051 micro-controller
- Support Ssecure Digital™ v1.0 / v1.1 / v2.0/ SDHC / SDXC (Capacity up to 2TB)
- Support Secure Digital™ v3.0 UHS-I (Ultra High Speed): SDR12/SDR25/SDR50/DDR50/SDR104
- Compliant with MultiMediaCard™ (MMC)
  - MMC specification v3.x / v4.0 / v4.1 / v4.2 / v4.3 / v4.4
  - x1 / x4 bit data bus
- Support Memory Stick™ / Memory Stick PRO / Memory Stick PRO Duo / Memory Stick Micro /Memory Stick PRO-HG / Memory Stick XC (Capacity up to 32GB)
  - Compliant with Memory Stick Series Specification: MS v1.43, MS PRO v1.05, MS Micro v1.04 (MS HG Micro v1.00), MS PRO-HG Duo 1.03, MS XC Duo v1.00, MS XC-HG Duo v1.00, MS XC Micro v1.00 and MS XC-HG Micro v1.00
  - Support Read/Write quad data access (512Bytex4) for MS PRO-HG to enhance the transmission rate
- Support ISP (In System Programming) for firmware upgrade from the external SPI Flash via USB port
- On-Chip power MOSFETs for supplying flash media card power
- On-chip 5V to 3.3V and 3.3V to 1.2V regulator
- On board 25 MHz Crystal driver circuit
- Pass the USB-IF Test Procedure for SuperSpeed product, TID:340760046
- Package available in 48 pin LQFP (7x7 mm)
- Package available in 48 pin QFN (6x6 mm)

Table 2.1 – GL3221 Dual LUNs Product Selection Guide

Supporting Cards	Package	Version Naming Rule
SD/MS	**48QFN/48LQFP**	**01, 02, 03…**
SD/CF	80LQFP	01, 02, 03…
SD/SD	48QFN/48LQFP	10, 20, 30…

Note1: Version is showed with the last two character of the second line of marking information.

CHAPTER 3 PIN ASSIGNMENT

3.1 QFN 48 Pinout

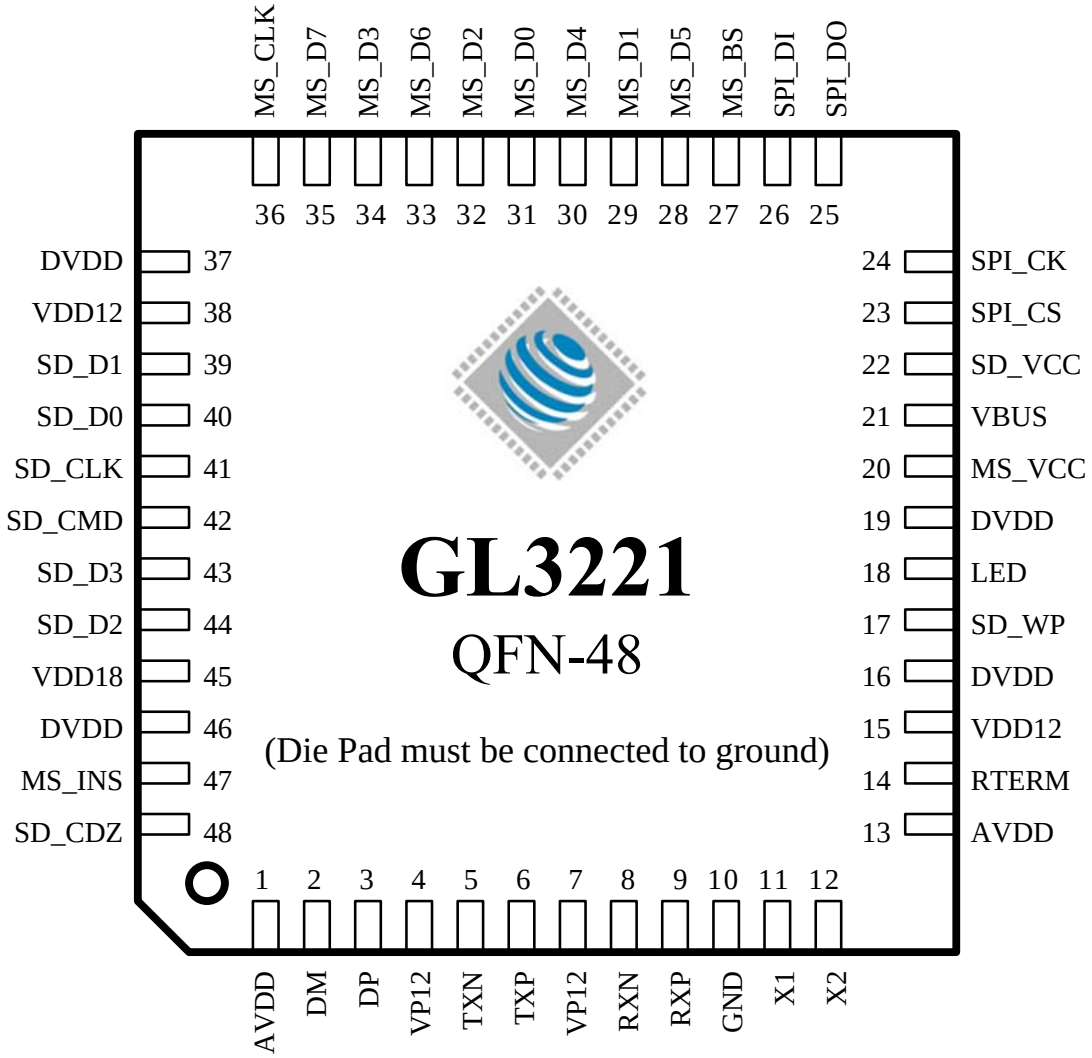


Figure 3.1 - QFN 48 Pinout Diagram

3.2 LQFP 48 Pinout

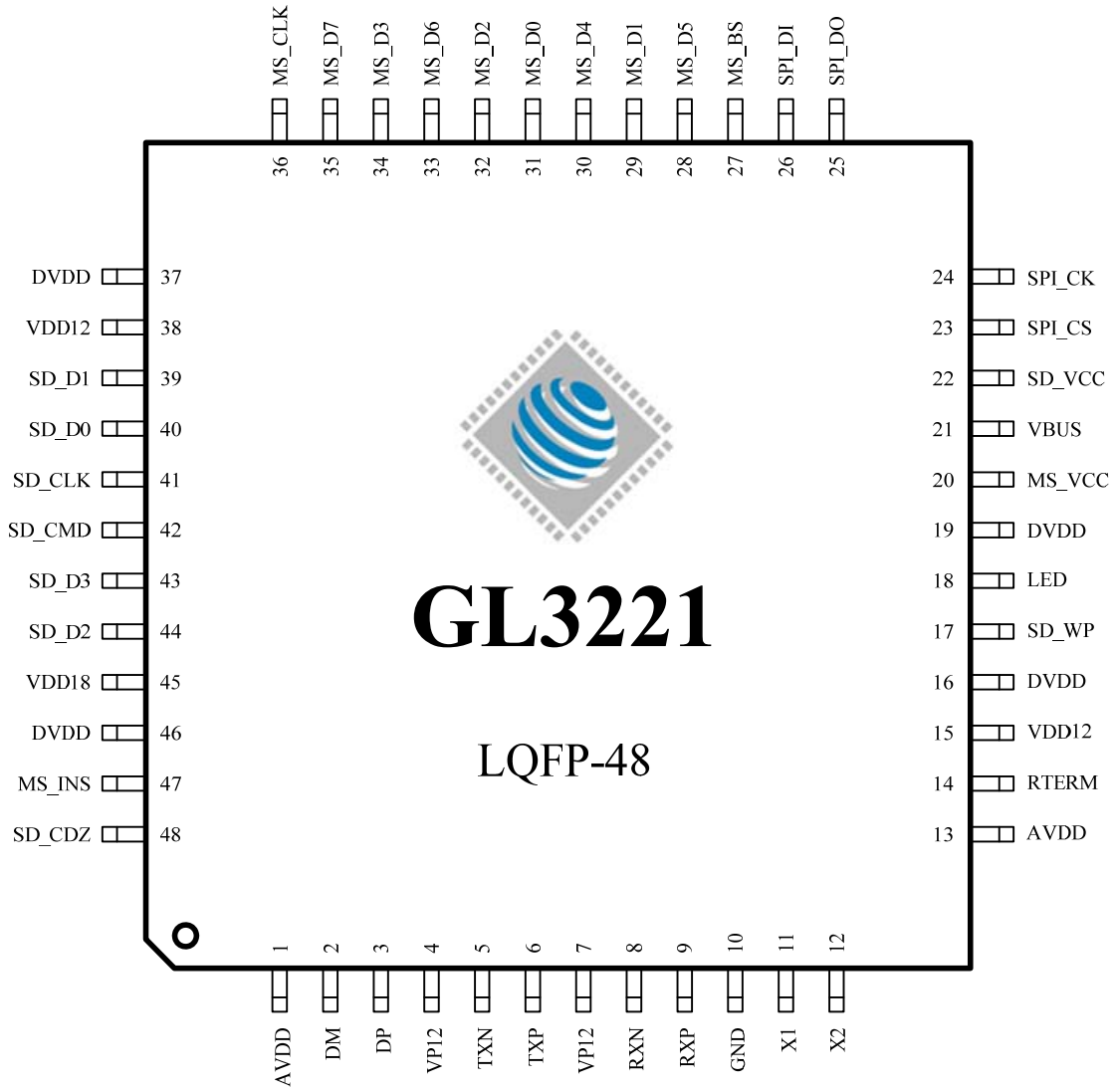


Figure 3.2 - LQFP 48 Pinout Diagram

3.3 Pin Description

Table 3.1 - Pin Description

Pin Name	QFN 48/ LQFP 48	Type	Description
Power/Ground			
AVDD	1,13	P	3.3V Analog power
DVDD	16,19,37,46	P	3.3V Digital power
VP12	4,7	P	1.2V Analog power
VDD12	15,38	P	1.2V Core power
VDD18	45	P	SD 3.0 IO PAD Power, the power source of this pin comes from the internal regulator of GL3221 and no need of external 1.8V power input
VBUS	21	P	5V Power source
SD_VCC	22	P	SD/MMC card power
MS_VCC	20	P	MS card power
GND	10	P	Ground
USB PHY Interface			
DM	2	A	USB 2.0 D-
DP	3	A	USB 2.0 D+
TXN	5	A	USB 3.0 TX-
TXP	6	A	USB 3.0 TX+
RXN	8	A	USB 3.0 RX-
RXP	9	A	USB 3.0 RX+
RTERM	14	A	USB reference resistor. This pin is used to control the level of USB signal. A 680ohm, 1% resistor is recommended to be laid between RREF and GND
X1	11	I	25MHz XTAL input. It can be connected to external 25MHz clock input
X2	12	B	25MHz XTAL output
Memory Card Interface			
SD_WP	17	I, pu	SD write protect 0: write enable 1: write protection
SD_CDZ	48	I, pu	SD card detect 0: Card insert 1: No card
SD_D[3:0]	43,44,39,40	B	SD data pins
SD_CLK	41	O	SD clock
SD_CMD	42	B	SD command/response
MS_BS	27	O	MS/MSP bus state
MS_INS	47	I, pu	MS insertion detect 0: Card insert 1: No card

MS_D[7:0]	35,33,28,30, 34,32,29,31	B	MS/MSP data signal
MS_CLK	36	O	MS clock
Others			
LED	18	O	Access LED
SPI_CS	23	O	SPI interface: chip select
SPI_CK	24	O	SPI interface: clock
SPI_DO	25	O	SPI interface: data output
SPI_DI	26	I	SPI interface: data input

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	pu	internal pull-up when input
	pd	internal pull-down when input
	P	Power / Ground
	A	Analog

CHAPTER 4 BLOCK DIAGRAM

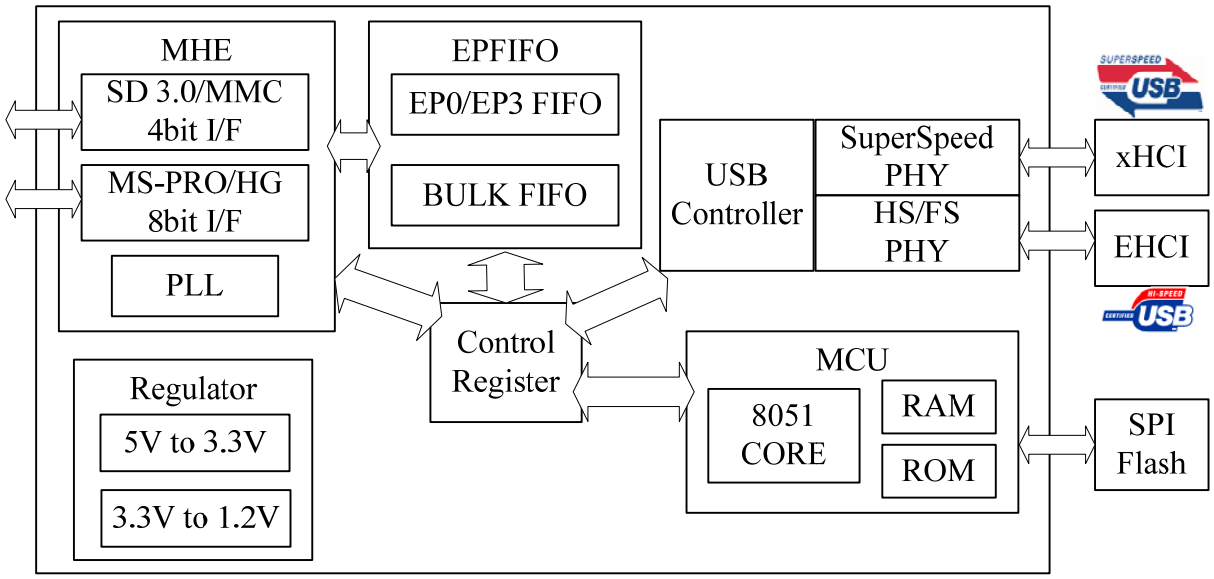


Figure 4.1 - Functional Block Diagram

4.1 Super Speed and HS/FS PHY

The transceiver macro cell is the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB to one that is compatible with the general logic.

4.2 USB Controller

The USB Controller, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

4.3 EPFIFO

Endpoint FIFO includes Control FIFO (FIFO0), Interrupt FIFO (FIFO3), Bulk In/Out FIFO

- **EP0 FIFO** FIFO of control endpoint 0. It is 512-byte FIFO and used for endpoint 0 data transfer.
- **EP3 FIFO** 32-byte depth FIFO of endpoint 3 for status interrupt
- **Bulk In/Out FIFO** It can be in the TX mode or RX mode:
  1. It can be transmit/receive 512-byte data of USB 2.0 and 1K-byte data of USB 3.0 continuously.
  2. It can be directly accessed by micro-controller

4.4 MCU

8051 micro-controller inside.

- **8051 Core** Compliant with Intel 8051 high speed micro-controller
- **ROM** FW code on ROM
- **SRAM** Internal RAM area for MCU access

4.5 MHE (Media Hardware Engine)

Media Interface: CF/xD/SD/MMC/MS/MS PRO/MS PRO-HG

4.6 Regulator

- **5V to 3.3V** 3.3V Power Source
- **3.3V to 1.2V** 1.8V Power Source

CHAPTER 5 ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Table 5.1 - Absolute Maximum Ratings

Parameter	Value
Storage Temperature	-65°C to +150 °C
Ambient Temperature	-40°C to +80 °C

5.2 Operating Conditions

Table 5.2 - Operating Conditions

Parameter	Value
Ta (Ambient Temperature Under Bias)	0°C to 70°C
Supply Voltage	+4.75V to +5.25V
Ground Voltage	0V
F_{OSC} (Oscillator or Crystal Frequency)	25 MHz ± 0.03%

5.3 DC Characteristics

Table 5.3 - DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.75	-	5.25	V
V_{IH}	Input High Voltage		2.0	-	-	V
V_{IL}	Input Low Voltage		-	-	0.4	V
I_I	Input Leakage Current	$0 < V_{IN} <$ DVDD	-10	-	10	μA
V_{OH}	Output High Voltage	DVDD = 3.3V	3.0	-	-	V
V_{OL}	Output Low Voltage		-	-	0.4	V
I_{OH}	Output Current High		-	8	-	mA
I_{OL}	Output Current Low		-	8	-	mA
C_{IN}	Input Pin Capacitance		-	5	-	pF
I_{NORMAL}	HS mode		-	46	-	mA
	SS mode	U0 state	-	140	-	mA
		U1 state	-	30	-	mA
		U2 state	-	16	-	mA
I_{ACTIVE}	HS mode		-	63	-	mA
	SS mode	U0 state	-	160	-	mA
I_{RESET}			-	48	-	mA

I_{SUS}	Suspend current	1.5K pull-up included	-	1.6	-	mA
R_{pu}	Reset Pad pull-up		44	61	92	KΩ
	SD_CDZ, SD_WP, MS_INS, GPIO Pad pull-up		44	61	92	KΩ
	SD_CMD pull-up		-	15	-	KΩ
	SD_CLK, D[3:0] Pad pull-up		-	15	-	KΩ
R_{pd}	SD_CMD pull-down		-	15	-	KΩ
	SD_CLK, D[3:0] Pad pull-down		-	15	-	KΩ
R_{IMP}	SD_CMD, SD_CLK, D[3:0] impedances		-	56	-	Ω

5.4 PMOS Characteristics

Table 5.4 - PMOS I-V table

Card Power / Loading	SD PMOS output	MS PMOS output
0 mA (No Loading)	3.27	3.27
200 mA	3.20	3.11
400 mA	3.12	3.08
600 mA	3.04	2.98
800 mA	2.96	---

(VBUS=5.0V, Temperature 25 °C)

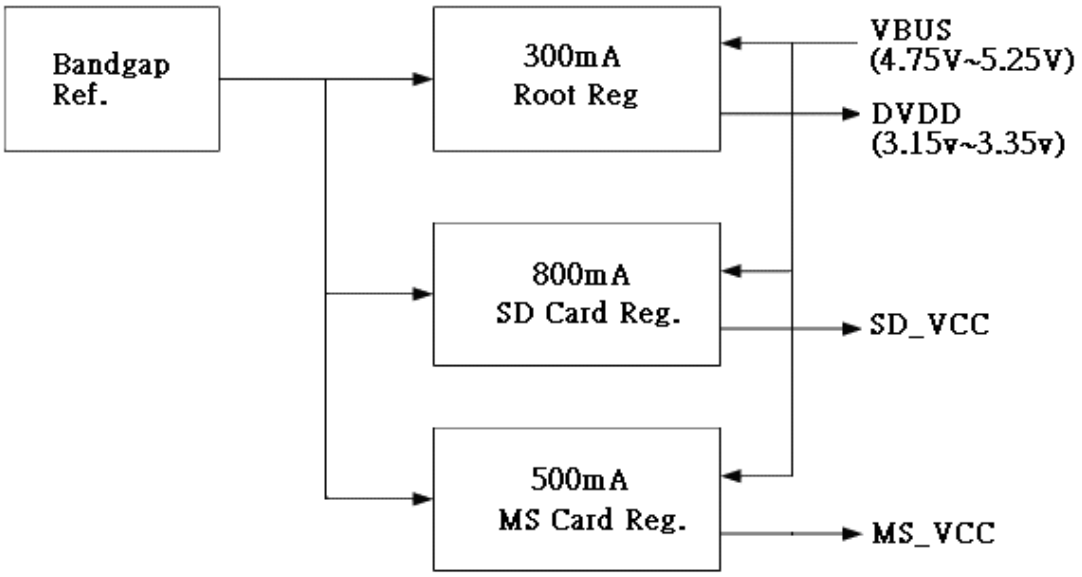


Figure 5.1 - PMOS Architecture

5.5 AC Characteristics

5.5.1 SD/MMC Card Clock Frequency

Table 5.5 - SD/MMC Card Clock Frequency

Parameter	Description	Max.	Unit
F_{ID}	Clock frequency Identification Mode	187	KHz
F_{DS}	Clock frequency Default Speed Mode	25	MHz
F_{HS}	SD Clock frequency High Speed Mode	50	MHz
F_{HS}	MMC Clock frequency High Speed Mode	52	MHz
F_{SDR25}	Clock frequency Ultra High Speed Mode: SDR25	50	MHz
F_{DDR50}	Clock frequency Ultra High Speed Mode: DDR50	50	MHz
F_{SDR50}	Clock frequency Ultra High Speed Mode: SDR50	100	MHz
F_{SDR104}	Clock frequency Ultra High Speed Mode: SDR104	208	MHz

5.5.2 MS Card Clock Frequency

Table 5.6 - MS Card Clock Frequency

Parameter	Description	Typ.	Unit
F_{DS}	Clock frequency Default Speed Mode	20	MHz
F_{MSP}	Clock frequency MS PRO 4bit Mode	40	MHz
F_{MSPHG}	Clock frequency MS PRO HG 8bit Mode	60	MHz

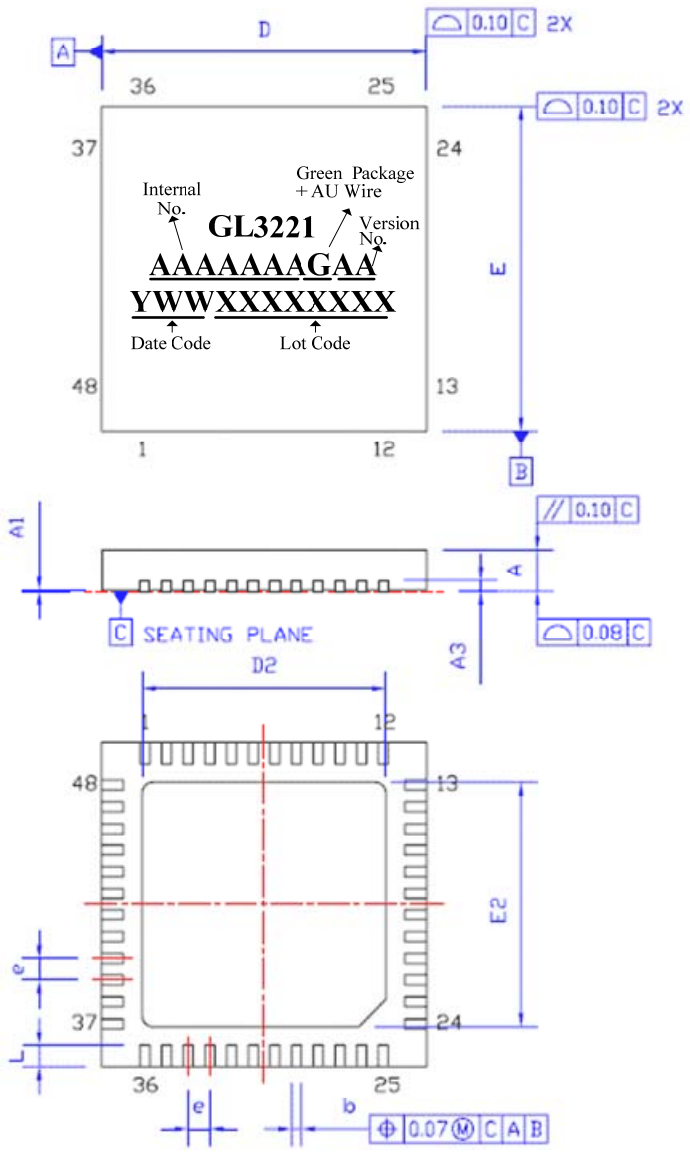
CHAPTER 6 SPI NOR FLASH SUPPORT LIST

Table 6.1 - SPI NOR Flash Support List

Vendor	Model	
AMIC	A25L040	A25LS512
	A25L080	
	A25L016	
	A25L032	
ATMEL	AT25F512B	
EON	EN25F10	
MXIC	MX25L5121E	MX25L6445E
	MX25L1021E	MX25L128451E
	MX25L1606E	
	MX25L8006E	
PMC	PM25LV512A	PM25LD010
	PM25LV010A	PM25LD020
	PM25LV020	
	PM25LD512C	
Sanyo	LE25FU206	
SST	SST25VF512	SST25LF020
	SST25VF010	
	SST25VF016B	
	SST25VF080B	
ST	M25P05	
	M25P10	
Winbond	W25X10A	W25X32A
	W25X20A	
	W25X16A	
	W25X80A	

Note: To support ISP (In System Programming) for firmware upgrade from the external SPI Flash via USB port, the density of SPI NOR Flash shall be larger than or equal to 512Kbit.

CHAPTER 7 PACKAGE DIMENSION



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.13 (5.1)	0.18 (7.1)	0.25 (9.8)
D	6.00 (236.2) BSC		
D2	4.40 (173.2)	4.50 (177.2)	4.60 (181.1)
E	6.00 (236.2) BSC		
E2	4.40 (173.2)	4.50 (177.2)	4.60 (181.1)
e	0.40 (15.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

Figure 6.1 - QFN 48 Pin Package

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	---	---	1.60 (63.0)
A1	0.05 (2.0)	---	0.15 (5.9)
A2	1.35 (53.1)	1.40 (55.1)	1.45 (57.1)
b	0.17 (6.7)	0.22 (8.7)	0.27 (10.6)
b1	0.17 (6.7)	0.20 (7.9)	0.23 (9.1)
c	0.09 (3.5)	---	0.20 (7.9)
c1	0.09 (3.5)	---	0.16 (6.3)
D	9.00 (354.3) BSC		
D1	7.00 (275.6) BSC		
e	0.50 (19.7) BSC		
E	9.00 (354.3) BSC		
E1	7.00 (275.6) BSC		
L	0.45 (17.7)	0.60 (23.6)	0.75 (29.5)
L1	1.00 (39.4) REF		
R1	0.08 (3.1)	---	---
R2	0.08 (3.1)	---	0.20 (7.9)
S	0.20 (7.9)	---	---
aaa	0.20 (7.9)		
bbb	0.20 (7.9)		
ccc	0.08 (3.1)		
ddd	0.08 (3.1)		
θ	0°	3.5°	7°
θ1	0°	---	---
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTE: 1. REFER TO JEDEC MS-026/BBC
2. ALL DIMENSIONS IN MILLIMETERS.

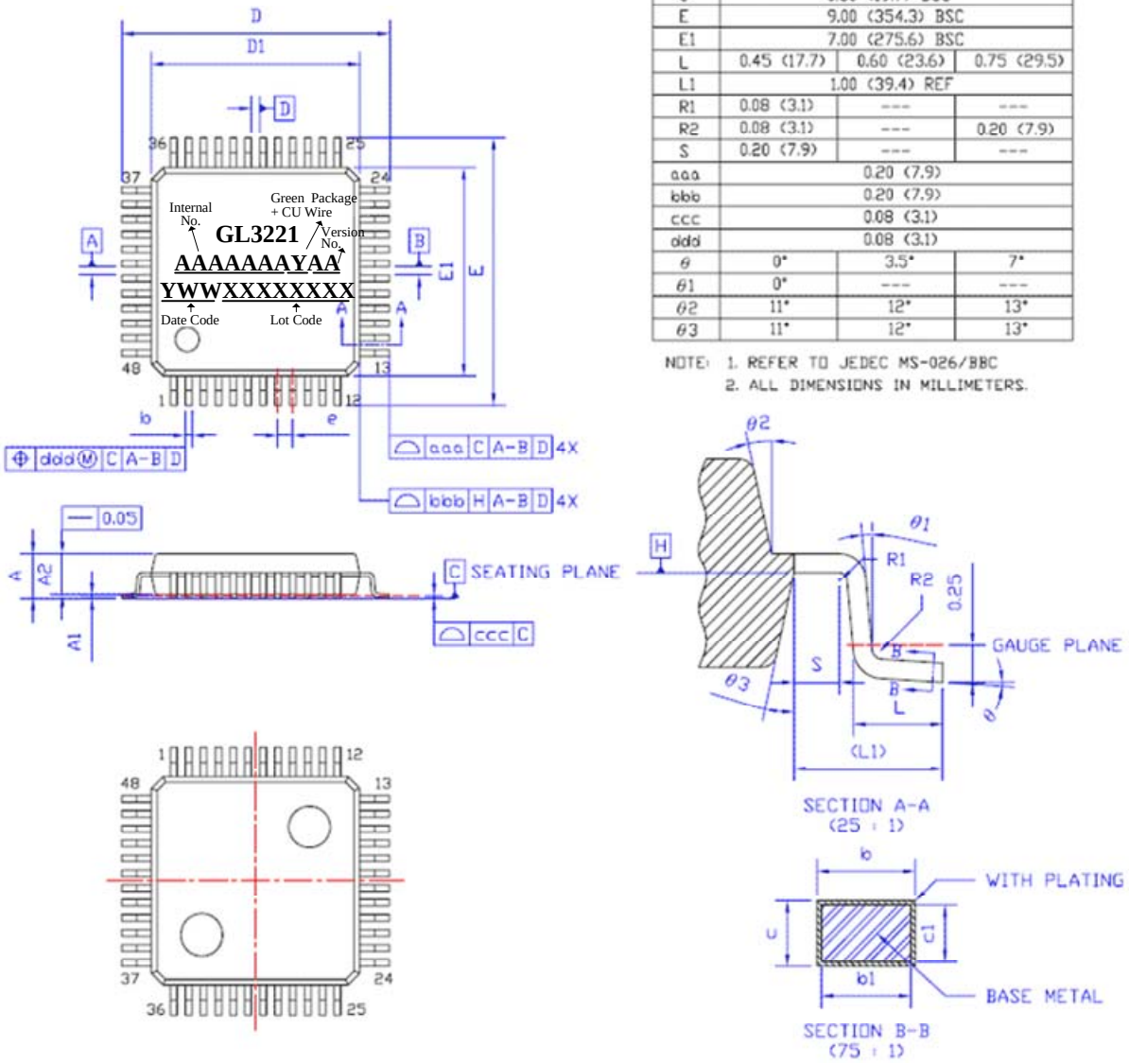


Figure 6.2 - LQFP 48 Pin Package

CHAPTER 8 ORDERING INFORMATION

Table 7.1 - Ordering Information

Part Number	Package	Green/Wire Material	Version	Status
GL3221-ONGXX	QFN 48	Green Package + AU Wire	XX	Available
GL3221-MNYXX	LQFP 48	Green Package + CU Wire	XX	Available