Genesys Logic, Inc.

GL3223

USB 3.0 Multi-LUN
Memory Card Reader Controller

Datasheet

Revision 1.03
Aug. 29, 2014

Copyright

Ownership and Title

Genesys Logic, Inc. owns and retains of its right, title and interest in and to all materials provided herein. Genesys Logic, Inc. reserves all rights, including, but not limited to, all patent rights, trademarks, copyrights and any other propriety rights. No license is granted hereunder.

Disclaimer

All Materials are provided "as is". Genesys Logic, Inc. makes no warranties, express, implied or otherwise, regarding their accuracy, merchantability, fitness for any particular purpose, and non-infringement of intellectual property. In no event shall Genesys Logic, Inc. be liable for any damages, including, without limitation, any direct, indirect, consequential, or incidental damages. The materials may contain errors or omissions. Genesys Logic, Inc. may make changes to the materials or to the products described herein at anytime without notice.

Genesys Logic, Inc.
12F., No. 205, Sec. 3, Beixin Rd., Xindian Dist. 231,
New Taipei City, Taiwan
Tel : (886-2) 8913-1888
Fax : (886-2) 6629-6168
http ://www.genesyslogic.com

Revision History

Revision	Date	Description
1.00	10/21/2013	First formal release
1.01	12/02/2013	1. Adding USB-IF logo TID, p7. 2. Adding WHCK/WHQL submission ID, p7, 8.
1.02	06/18/2014	1. Modify eMMC spec in Ch2, p7. 2. Update SPI FLASH MEMORY SUPPORT LIST in Ch6, p19.
1.03	08/29/2014	Add OCCS (On-Chip Clock Source) feature in p6, 7, 10

Table of Contents

CHAPTER 1 GENERAL DESCRIPTION 6

CHAPTER 2 FEATURES 7

CHAPTER 3 PIN ASSIGNMENT 9

3.1 LQFP 128 Pinout 9

3.2 Pin Description 10

CHAPTER 4 BLOCK DIAGRAM 14

4.1 Super Speed and HS/FS PHY 14

4.2 USB Controller 14

4.3 EPFIFO 14

4.4 MCU 15

4.5 MHE (Media Hardware Engine) 15

4.6 Regulator 15

CHAPTER 5 ELECTRICAL CHARACTERISTICS 16

5.1 Temperature Conditions 16

5.2 Operating Conditions 16

5.3 DC Characteristics 16

5.4 AC Characteristics of Reset Timing 17

5.4.1 Reset Timing 17

5.4.2 SD/MMC Card Clock Frequency 18

5.4.3 *e*•MMC Clock Frequency 18

5.4.4 MS Card Clock Frequency 18

CHAPTER 6 SPI FLASH MEMORY SUPPORT LIST 19

CHAPTER 7 PACKAGE DIMENSION 20

CHAPTER 8 ORDERING INFORMATION 21

List of Figures

Figure 3.1 - LQFP 128 Pinout Diagram 9
Figure 4.1 - Functional Block Diagram 14
Figure 5.1 - Timing Diagram of Reset Width 17
Figure 5.2 - Timing Diagram of Power Good to USB Command Receive Ready 17
Figure 7.1 - LQFP 128 Pin Package 20

List of Tables

Table 3.1 - Pin Description 10
Table 5.1 - Absolute Maximum Ratings 16
Table 5.2 - Operating Conditions 16
Table 5.3 - DC Characteristics 16
Table 5.4 - Reset Timing 18
Table 5.5 - SD/MMC Card Clock Frequency 18
Table 5.6 - *e*•MMC Clock Frequency 18
Table 5.7 - MS Card Clock Frequency 18
Table 6.1 - SPI Flash Memory Support List 19
Table 8.1 - Ordering Information 21

CHAPTER 1 GENERAL DESCRIPTION

The GL3223 is a crystal-less USB 3.0 Multi-LUN card reader controller, it provides 5 LUNs (Logic Unit Number) which can support various types of memory cards, such as CompactFlash™, Micro Drive, Secure Digital™(SD), SDHC, miniSD, microSD (T-Flash), MultiMediaCard™ (MMC), RS-MMC, MMCmicro, MMCmobile, Memory Stick™ (MS), Memory Stick Duo™ (MS Duo), High Speed Memory Stick™ (HS MS), Memory Stick PRO™ (MS PRO), Memory Stick PRO™ Duo (MS PRO Duo), Memory Stick PRO-HG™ (MS PRO-HG), MS PRO Micro and xD-picture card in one chip. It also supports SDXC and Memory Stick XC high density memory cards (capacity up to 2TB) and SD3.0 UHS-I memory cards.

The GL3223 integrates a high speed 8051 microprocessor and a high efficiency hardware engine for the best data transfer performance between USB and various memory card interfaces. It supports Serial Peripheral Interface (SPI) for firmware upgrade to SPI Flash Memory via USB port. It also integrates 5V to 3.3V and 3.3V to 1.2V regulators and power MOSFETs which can reduce system BOM cost.

CHAPTER 2 FEATURES

- USB specification compliance
  - Comply with Universal Serial Bus 3.0 Specification rev. 1.0 (USB 3.0)
  - Comply with Universal Serial Bus Specification rev. 2.0 (USB 2.0)
  - Comply with USB Mass Storage Class Specification rev. 1.0
  - Support USB Mass Storage Class Bulk-Only Transport (BOT)
  - Support 1 device address and up to 3 endpoints: Control (0) / Bulk Data Read In (1) / Bulk Data Write Out (2)
  - Support 5 Gbps SuperSpeed, 480 Mbps high-speed, and 12 Mbps full-speed transfer rates
- Integrated USB building blocks
  - USB2.0 transceiver macrocell (UTM), Serial Interface Engine (SIE), embedded Power-On Reset (POR)
- Embedded high speed 8051 micro-controller
- High efficient DMA hardware engine improves transfer rate between USB and flash card interfaces
- Support CompactFlash™ v6.0 with PIO mode 6 / Ultra DMA mode 7 and LBA48 (capacity up to 144PB)
- Support Ssecure Digital™ v1.0/ v1.1/ v2.0/ SDHC/ SDXC (Capacity up to 2TB)
- Support Secure Digital™ v3.01 UHS-I (Ultra High Speed): SDR12/ SDR25/ SDR50/ DDR50/ SDR104
- Support MultiMediaCard™ (MMC)
  - MMC specification v3.x/ v4.0/ v4.1/ v4.2
  - x1/ x4/ x8 bit data bus
- Support Embedded MultiMediaCard ™ (*e*•MMC)
  - *e*•MMC specification v4.3/ v4.4/ v4.5/ v5.0
  - High Speed SDR/ High Speed DDR/ HS200
- Support Memory Stick™/ Memory Stick PRO™/ Memory Stick PRO Duo™/ Memory Stick PRO Duo Mark2™/ Memory Stick Micro™ (M2)/ Memory Stick PRO-HG™/ Memory Stick PRO-HG Duo™/ Memory Stick PRO-HG Duo HX™
  - Compliant with Memory Stick Series Specification: MS v1.43, MS PRO v1.05, MS Micro v1.04 (MS HG Micro v1.00), MS PRO-HG Duo 1.03, MS XC Duo v1.00, MS XC-HG Duo v1.00, MS XC Micro v1.00 and MS XC-HG Micro v1.00
  - Support Read/Write quad data access (512Bytex4) for MS PRO-HG to enhance the transmission rate
- Support xD-Picture™ v1.2C Type M/H
- Support Serial Peripheral Interface (SPI) for firmware upgrade to SPI Flash Memory via USB interface
- Support operation by either MASK ROM or external FW in SPI Flash Memory
- On-chip power MOSFETs for all flash media cards power source
- On-chip 5V to 3.3V and 3.3V to 1.2V regulator
- On board 25 MHz Crystal driver circuit (optional)
- Support OCCS (On-Chip Clock Source) to eliminate external 25MHz crystal to save BOM cost
- Support USB2.0 LPM (Link Power Management)
- Support USB3.0 LTM (Latency Tolerance Messaging)
- Support USB3.0 U1/U2/U3 low power link state
- Pass the USB-IF Test Procedure for SuperSpeed product (TID: 340890025)
- Pass WHCK (Windows Hardware Certification Kit) test for Windows 8.1 (Submission ID: 1620543)

- Pass WHCK (Windows Hardware Certification Kit) test for Windows 8 (Submission ID: 1620537)
- Pass WHQL (Windows Hardware Quality Lab) test for Windows 7 (Submission ID: 1620861)
- Support two SD3.0 interfaces with UHS-I: SDR12/ SDR25/ SDR50/ DDR50/ SDR104 bus mode
- Support programmable disable MMC interface
- Support programmable various LUN (Logic Unit Number): 5, 4, 3, 2 LUNs and 1 LUN
- Support programmable SSC (Spread Spectrum Clocking), clock rate for SD, MS memory card interface
- Support programmable LED behavior, Read Only option for specific application
- Support power-saving mode to disconnect USB bus by card remove for better power management
- Support selective-suspend for entering suspend mode when data transfer pending after several seconds.
- Support Over-Current protection mechanism
- Available in LQFP128 pin package (14x14mm) for 5 LUNs: CF, SD, MS, xD and microSD/M2

CHAPTER 3 PIN ASSIGNMENT

3.1 LQFP 128 Pinout

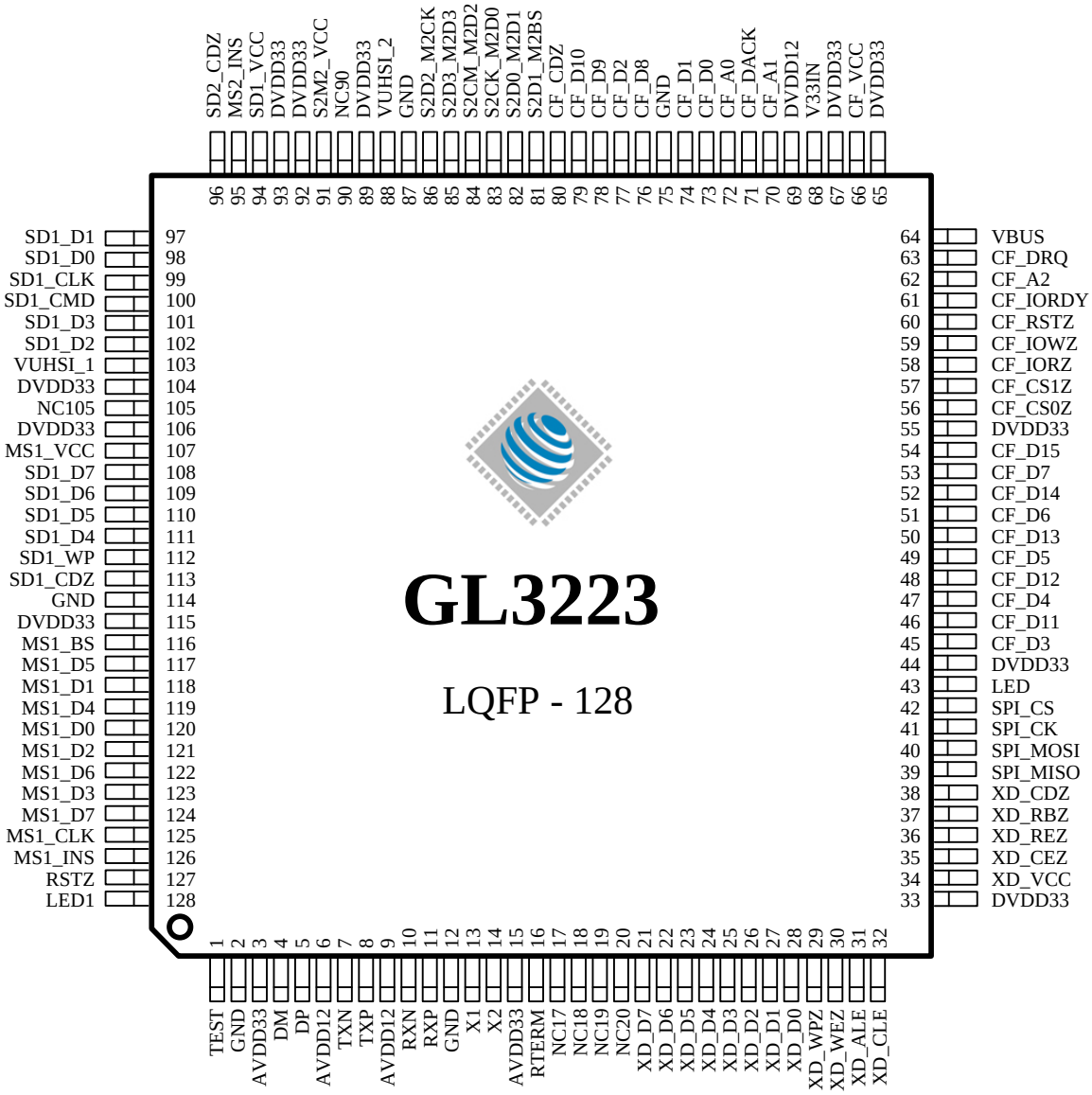


Figure 3.1 - LQFP 128 Pinout Diagram

3.2 Pin Description

Table 3.1 - Pin Description

Pin Name	LQFP 128	Type	Description
Power/Ground			
AVDD12	6, 9,	P	Analog 1.2V power
AVDD33	3, 15,	P	Analog 3.3V power
DVDD12	69,	P	Digital 1.2V power
DVDD33	33, 44, 55, 65, 67, 89, 92, 93, 104, 106, 115	P	Digital 3.3V power
VBUS	64	P	5V power source
V33IN	68	P	3.3V to 1.2V regulator power
VUHSI_1	103	P	SD 3.0 IO PAD Power, the power source of this pin comes from the internal regulator of GL3223 and no need of external power input
VUHSI_2	88	P	SD 3.0 IO PAD Power, the power source of this pin comes from the internal regulator of GL3223 and no need of external power input
SD1_VCC	94	P	SD card power (capacity: 800mA)
CF_VCC	66	P	CF card power (capacity: 500mA)
XD_VCC	34	P	xD card power (capacity: 200mA)
MS1_VCC	107	P	MS card power (capacity: 500mA)
S2M2_VCC	91	P	microSD/M2 card power (capacity: 800mA)
GND	2, 12, 75, 87, 114	P	Ground
USB PHY Interface			
DP	5	A	USB 2.0 D+
DM	4	A	USB 2.0 D-
TXN	7	A	USB 3.0 TX-
TXP	8	A	USB 3.0 TX+
RXN	10	A	USB 3.0 RX-
RXP	11	A	USB 3.0 RX+
RTERM	16	A	USB reference resistor. This pin is used to control the level of USB signal. A 680ohm, 1% resistor is recommended to be laid between RTERM and GND
X1	13	I	25MHz x'TAL input. It can be connected to external 25MHz clock input(Optional)
X2	14	B	25MHz x'TAL output(Optional)
Memory Card Interface			
CF_CDZ	80	I, pu	CF card detect 0: Card insert 1: No card

CF_D[15:0]	54, 52, 50, 48, 46,79, 78, 76, 53, 51,49, 47, 45, 77, 74,73	B	CF data pins
CF_CS0Z	56	O	CF chip select 0
CF_CS1Z	57	O	CF chip select 1
CF_IORZ	58	O	CF IO read
CF_IOWZ	59	O	CF IO write
CF_RSTZ	60	O	CF reset
CF_IORDY	61	I, pd	CF IO ready
CF_DRQ	63	I, pd	CF DMA request
CF_DACK	71	O	CF DMA acknowledge
CF_A[2:0]	62, 70, 72	O	CF address
XD_D[7:0]	21~28	B	xD data pins
XD_WPZ	29	O	xD write protect
XD_WEZ	30	O	xD write enable
XD_ALE	31	O	xD_ALE
XD_CLE	32	O	xD command latch enable
XD_CEZ	35	O	xD card enable
XD_REZ	36	O	xD read enable
XD_RBZ	37	I, pu	xD read/busy
XD_CDZ	38	I, pu	xD card detect 0: Card insert 1: No card
SD1_WP	112	I, pu	SD write protect 0: write enable 1: write protection
SD1_CDZ	113	I, pu	SD card detect 0: Card insert 1: No card
SD1_D[7:0]	108, 109, 110, 111,101, 102, 97, 98	B	SD data pins
SD1_CLK	99	O	SD clock
SD1_CMD	100	B,pu	SD command/response
MS1_BS	116	O	MS/MSP bus state

MS1_INS	126	I, pu	MS insertion detect 0: Card insert 1: No card
MS1_D[7:0]	124, 122, 117, 119,123, 121, 118, 120	B	MS/MSP data signal
MS1_CLK	125	O	MS clock
SD2_CDZ	96	I, pu	SD card detect 0: Card insert 1: No card
MS2_INS	95	I, pu	MS insertion detect 0: Card insert 1: No card
S2D1_M2BS	81	B	SD data pin
		O	MS/MSP bus state
S2D0_M2D1	82	B	SD data pin
		B	MS/MSP data signal
S2CK_M2D0	83	O	SD clock
		B	MS/MSP data signal
S2CM_M2D2	84	B,pu	SD command/response
		B	MS/MSP data signal
S2D3_M2D3	85	B	SD data pin
		B	MS/MSP data signal
S2D2_M2CK	86	B	SD data pin
		O	MS clock
Others			
RSTZ	127	I, pu	Chip reset, active low
LED	43	O	Memory card access LED
LED1	128	O	Power LED
NC	17, 18, 19, 20, 90,105		Not Connected
SPI_CS	42	O	SPI interface: chip select
SPI_CK	41	O	SPI interface: clock
SPI_MISO	39	I	SPI interface: connect to SPI flash data output
SPI_MOSI	40	O	SPI interface: connect to SPI flash data input

TEST	1	I, pd	Test mode

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	pu	internal pull-up when input
	pd	internal pull-down when input
	P	Power / Ground
	A	Analog

CHAPTER 4 BLOCK DIAGRAM

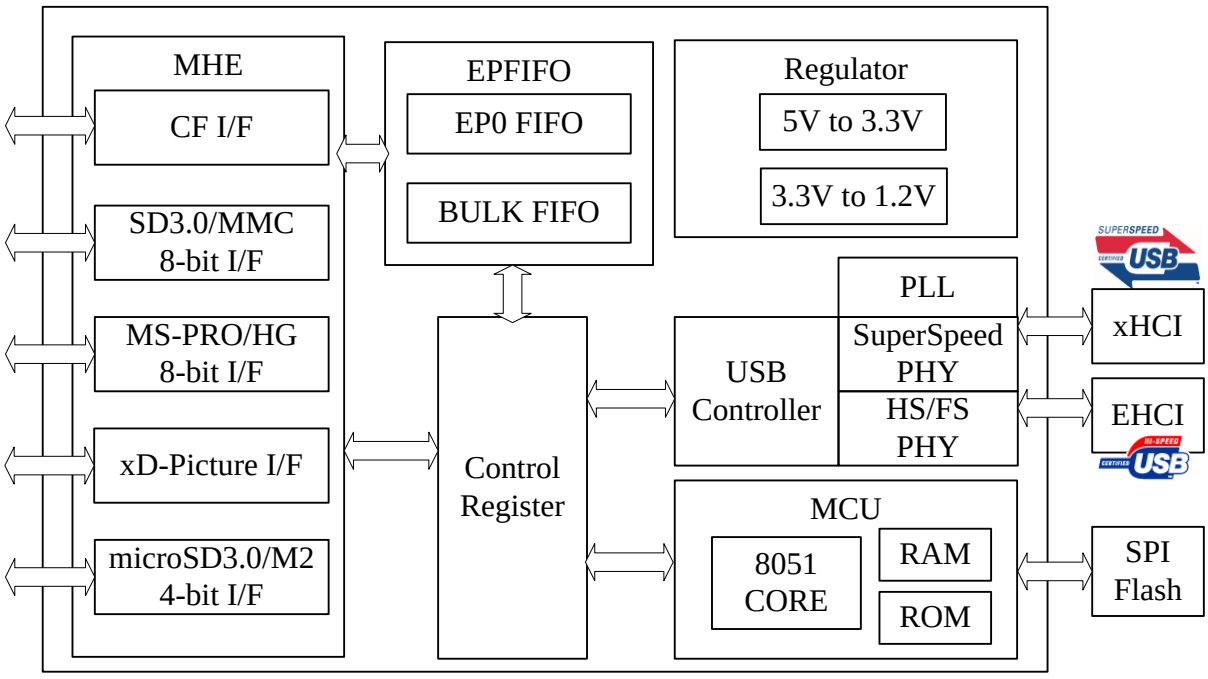


Figure 4.1 - Functional Block Diagram

4.1 Super Speed and HS/FS PHY

The transceiver macro cell is the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB to one that is compatible with the general logic.

4.2 USB Controller

The USB Controller, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

4.3 EPFIFO

Endpoint FIFO includes Control FIFO (FIFO0), Interrupt FIFO (FIFO3), Bulk In/Out FIFO

- **EP0 FIFO** FIFO of control endpoint 0. It is 512-byte FIFO and used for endpoint 0 data transfer.
- **Bulk In/Out FIFO** It can be in the TX mode or RX mode:
  1. It can be transmit/receive 512-byte data of USB 2.0 and 1K-byte data of USB 3.0 continuously.
  2. It can be directly accessed by micro-controller

4.4 MCU

8051 micro-controller inside.

- **8051 Core** Compliant with Intel 8051 high speed micro-controller
- **ROM** Firmware code on ROM
- **SRAM** Internal RAM area for MCU access

4.5 MHE (Media Hardware Engine)

Media Interface: CF/xD/SD/MMC/MS/MS PRO/MS PRO-HG

4.6 Regulator

- **5V to 3.3V** 3.3V Power Source
- **3.3V to 1.2V** 1.2V Power Source

CHAPTER 5 ELECTRICAL CHARACTERISTICS

5.1 Temperature Conditions

Table 5.1 - Absolute Maximum Ratings

Parameter	Value
Storage Temperature	-65°C to +150 °C
Operating Temperature	0°C to +70 °C

5.2 Operating Conditions

Table 5.2 - Operating Conditions

Parameter	Value
Supply Voltage	+4.75V to +5.25V
Ground Voltage	0V
F_{OSC} (Oscillator or Crystal Frequency)	25 MHz ± 0.03%

5.3 DC Characteristics

Table 5.3 - DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.4	V
I_I	Input Leakage Current	$0 < V_{IN} <$ DVDD	-10		10	μA
V_{OH}	Output High Voltage	DVDD = 3.3V	2.8			V
V_{OL}	Output Low Voltage				0.4	V
I_{OH}	Output Current High			8		mA
I_{OL}	Output Current Low			8		mA
C_{IN}	Input Pin Capacitance			5		pF
I_{NORMAL}	HS mode			43		mA
	SS mode	U0 state		120		mA
		U1 state		27		mA
		U2 state		13		mA
I_{ACTIVE}	HS mode			65		mA
	SS mode	U0 state		147		mA
I_{RESET}				40		mA

I_{SUS}	HS Suspend current	1.5K pull-up included		1.58		mA
	SS Suspend current	U3 state		1.45		mA
R_{pu}	Reset Pad pull-up			46		KΩ
	SD_CDZ, SD_WP, MS_INS, GPIO Pad pull-up			46		KΩ
	SD_CMD pull-up			15		KΩ
	SD_CLK, D[3:0] Pad pull-up			15		KΩ
R_{pd}	SD_CMD pull-down			15		KΩ
	SD_CLK, D[3:0] Pad pull-down			15		KΩ
R_{IMP}	SD_CMD, SD_CLK, D[3:0] impedances			50		Ω

5.4 AC Characteristics of Reset Timing

5.4.1 Reset Timing

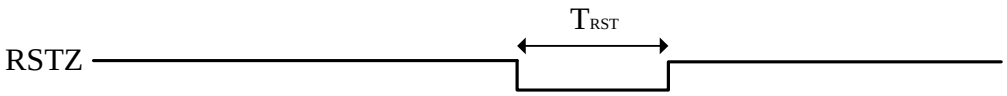


Figure 5.1 - Timing Diagram of Reset Width

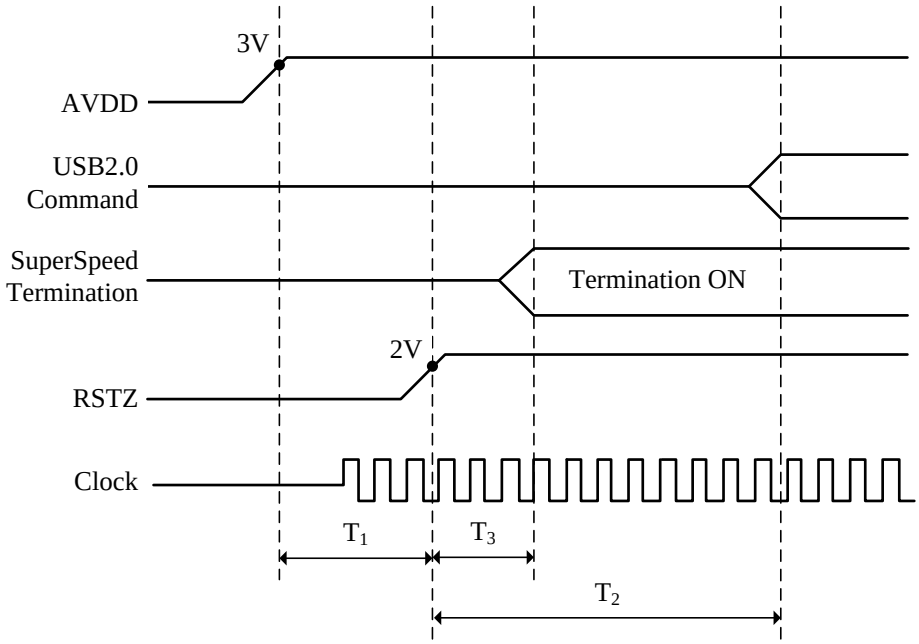


Figure 5.2 - Timing Diagram of Power Good to USB Command Receive Ready

Table 5.4 - Reset Timing

Parameter	Description	Min.	Unit
T_{RST}	Chip reset sense timing width	2	us
T1	AVDD power up to reset de-assert	500	us
T2	Reset de-assert to respond USB command ready	95	ms
T3	Reset de-assert to SuperSpeed termination on	12	ms

5.4.2 SD/MMC Card Clock Frequency

Table 5.5 - SD/MMC Card Clock Frequency

Parameter	Description	Max.	Unit
F_{ID}	Clock frequency Identification Mode	400	KHz
F_{DS}	Clock frequency Default Speed Mode	25	MHz
F_{HS}	SD Clock frequency High Speed Mode	50	MHz
F_{HS}	MMC Clock frequency High Speed Mode	52	MHz
F_{SDR25}	Clock frequency Ultra High Speed Mode: SDR25	50	MHz
F_{DDR50}	Clock frequency Ultra High Speed Mode: DDR50	50	MHz
F_{SDR50}	Clock frequency Ultra High Speed Mode: SDR50	100	MHz
F_{SDR104}	Clock frequency Ultra High Speed Mode: SDR104	208	MHz

5.4.3 *e*•MMC Clock Frequency

Table 5.6 - *e*•MMC Clock Frequency

Parameter	Description	Max.	Unit
F_{ID}	Clock frequency Identification Mode	400	KHz
F_{SDR}	Clock frequency High Speed SDR	52	MHz
F_{DDR}	Clock frequency High Speed DDR	52	MHz
F_{HS200}	Clock frequency HS200	200	MHz

5.4.4 MS Card Clock Frequency

Table 5.7 - MS Card Clock Frequency

Parameter	Description	Max.	Unit
F_{DS}	Clock frequency Default Speed Mode	20	MHz
F_{MSP}	Clock frequency MS PRO 4bit Mode	40	MHz
F_{MSPHG}	Clock frequency MS PRO HG 8bit Mode	60	MHz

CHAPTER 6 SPI FLASH MEMORY SUPPORT LIST

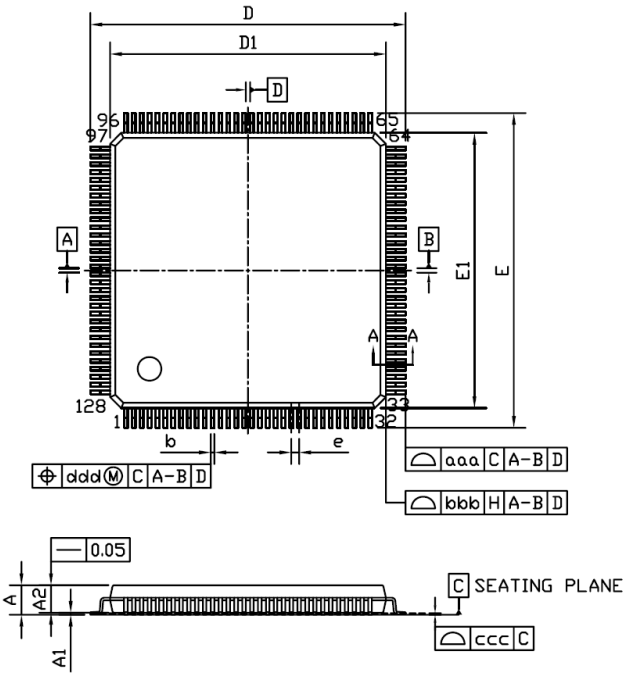
Table 6.1 - SPI Flash Memory Support List

Vendor	Model
GigaDevice	GD25Q512
	GD25Q010
	GD25Q040
PMC	PM25LD512C
	PM25LD010
	PM25LD010C
	PM25LD020
	PM25LD020C
WINBON	W25X05CL
	W25X10CL
	W25X10BV
	W25X20CL
	W25X20BV
EON	EN25Q40
MXIC	MX25L1006E
ESMT	F25L01PA-86PG
	F25L01PA-100PG
Giantec	GT25F512

Note :

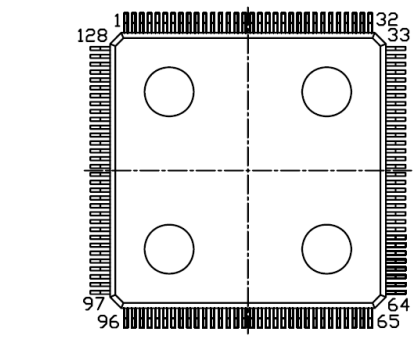
- GL3223 support Page-Program SPI Flash Memory only, does not support Byte-program SPI Flash Memory
- The density of SPI Flash Memory shall be larger than or equal to 512Kbit.
- Firmware file (xxxx.bin) which Genesys Logic provided is only used for Genesys Logic's Multi-Tool and MP Tool ISP (In System Programming via USB interface) purpose. If you would like to provide FW to SPI Flash vendor for pre-loading or Flash ROM writer usage, please contact to GL technical support team.

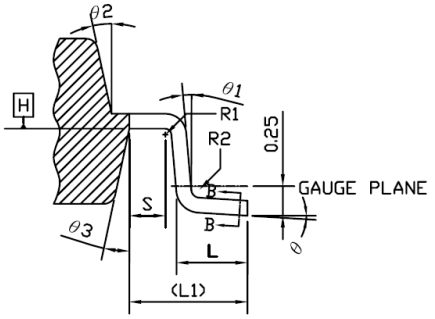
CHAPTER 7 PACKAGE DIMENSION



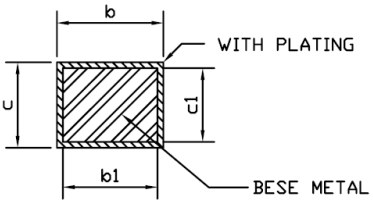
SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	---	---	1.60 (63.0)
A1	0.05 (2.0)	---	0.15 (5.9)
A2	1.35 (53.1)	1.40 (55.1)	1.45 (57.1)
b	0.13 (5.1)	0.18 (7.1)	0.23 (9.1)
b1	0.13 (5.1)	0.16 (6.3)	0.19 (7.5)
c	0.09 (3.5)	---	0.20 (7.9)
c1	0.09 (3.5)	---	0.16 (6.3)
D	16.00 (629.9) BSC		
D1	14.00 (551.) BSC		
e	0.40 (15.7) BSC		
E	16.00 (629.9) BSC		
E1	14.00 (551.) BSC		
L	0.45 (17.7)	0.60 (23.6)	0.75 (29.5)
L1	1.00 (39.4) REF		
R1	0.08 (3.1)	---	---
R2	0.08 (3.1)	---	0.20 (7.9)
S	0.20 (7.9)	---	---
aaa	0.20 (7.9)		
bbb	0.20 (7.9)		
ccc	0.08 (3.1)		
ddd	0.07 (2.8)		
θ	0°	3.5°	7°
θ1	0°	---	---
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTE: 1. REFER TO JEDEC MS-026/BEE
2. ALL DIMENSIONS IN MILLIMETERS.





SECTION A-A
(18 : 1)



SECTION B-B
(90 : 1)

Figure 7.1 - LQFP 128 Pi

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Green/Wire Material	Version	Status
GL3223-MXYXX	LQFP 128	Green Package + CU Wire	XX	Available