Genesys Logic, Inc.

GL3321G

USB 3.0 to SATA 6Gb/s Bridge Controller

Datasheet

Revision 1.40
Feb. 21, 2013

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Revision History

Revision	Date	Description
1.00	03/14/2012	First formal release
1.01	03/21/2012	Modify Chapter 2 Pin assignment
1.10	08/10/2012	Modify Block diagram
1.20	08/17/2012	Modify Feature list
1.30	01/25/2013	Remove windows to go feature Remove BYP pin
1.40	02/21/2013	Remove UASP

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CHAPTER 1 FEATURES

- USB specification compliance
  - Comply with Universal Serial Bus 3.0 Specification rev. 1.0 (USB 3.0)
  - Comply with Universal Serial Bus Specification rev. 2.0 (USB 2.0)
  - Comply with USB Mass Storage Class Specification rev. 1.0
  - Support USB Mass Storage Class Bulk-Only Transport (BOT)
  - Support 1 device address and up to 6 endpoints: Control (0) / Bulk Data Write Out (1) / Bulk Data Read In (2) / Interrupt In (3) / CMD Out (4) / Status In (5)
  - Support 5 Gbps SuperSpeed, 480 Mbps high-speed, and 12 Mbps full-speed transfer rates
- SATA specification features
  - Comply with Serial ATA Revision 3.0 Specification Gold Revision
  - Support SATA power saving, including partial and slumber modes
  - Support SATA Hot Plug
  - Support Native Command Queuing up to 32 commands
  - Support SATA host/device initiated power management
  - Support SATA BIST host/device initiated eye pattern test
  - Support 6.0 Gbps, 3.0 Gbps and 1.5 Gbps transfer rates
  - Support SATA Device Sleep function (DevSlp)
- Embedded 8051 micro-controller
  - Embedded 64 Kbytes Mask ROM
  - Embedded 16 Kbytes Code SRAM for Cache and 2 Kbytes Data SRAM
- Embedded internal regulators
  - 5 V to 3.3V linear drop-out regulator for whole chip power supply
  - Inductor-type DC-DC for core power, input range from 2.97 V to 3.63 V
- Single clock source, supporting 30 MHz
- Available in 48-pin QFN (6 x 6 mm^2)
- Operating System support
  - Windows 8/Windows 7 32&64/Vista32&64/XP/2000/Me/98/98SE, Mac OS 9.X/10.X, Linux Kernel 2.4.X/2.6.X
- Other Features
  - Support write Protect Function, Password Security (virtual CD ROM), Backup Management
  - Support Trim Command for SSD
  - Support ODD (BD, DVD, CD)
  - Spread Spectrum Clocking (SSC) for EMI reduction
  - On-chip watchdog timer for automatic error recovery
  - SPI interface for firmware update.
  - PWM interfaces for fan control and LED control (2 GPIOs).
  - UART interface for debugging

CHAPTER 2 PIN ASSIGNMENT

2.1 GL3321G Pinout

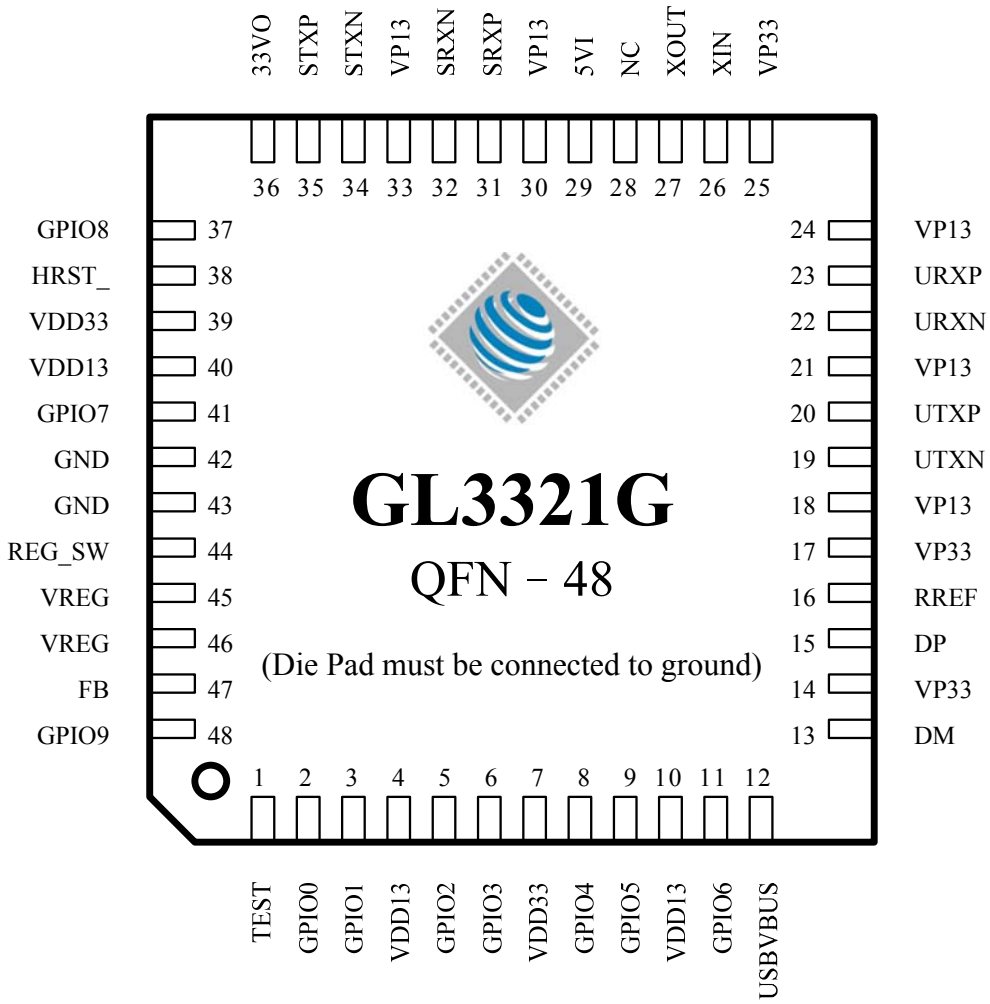


Figure 2.1 － GL3321G 48-pin QFN Pinout Diagram

2.2 GL3321G Pin List

Table 2.1 – GL3321G 48-pin QFN Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	TEST	I	13	DM	B	25	VP33	P	37	GPIO8	B
2	GPIO0	B	14	VP33	P	26	XIN	I	38	HRST_	I
3	GPIO1	B	15	DP	B	27	XOUT	O	39	VDD33	P
4	VDD13	P	16	RREF	A	28	NC	A	40	VDD13	P
5	GPIO2	B	17	VP33	P	29	5VI	P	41	GPIO7	B
6	GPIO3	B	18	VP13	P	30	VP13	P	42	GND	P
7	VDD33	P	19	UTXN	O	31	SRXP	I	43	GND	P
8	GPIO4	B	20	UTXP	O	32	SRXN	I	44	REG_SW	P
9	GPIO5	B	21	VP13	P	33	VP13	P	45	VREG	P
10	VDD13	P	22	URXN	I	34	STXN	O	46	VREG	P
11	GPIO6	B	23	URXP	I	35	STXP	O	47	FB	A
12	USBVBUS	P	24	VP13	P	36	33VO	P	48	GPIO9	B

2.3 Pin Descriptions

Table 2.2 – 48-pin QFN Pin Descriptions by Functionality

Name	QFN 48	Type	Description
USB 3.0			
UTXN	19	O	USB 3.0 differential transmit TX-
UTXP	20	O	USB 3.0 differential transmit TX+
URXN	22	I	USB 3.0 differential receive RX-
URXP	23	I	USB 3.0 differential receive RX+
USB 2.0			
DM	13	B	USB D-
DP	15	B	USB D+
USBVBUS	12	P	USB VBUS detect
SATA 6Gb/s, 3Gb/s, and 1.5Gb/s			
SRXP	31	I	SATA differential receive RX+
SRXN	32	I	SATA differential receive RX-
STXN	34	O	SATA differential transmit TX-

STXP	35	O	SATA differential transmit TX+
Clock Source			
XIN	26	I	Crystal input
XOUT	27	O	Crystal output
RREF	16	A	Reference resistor
Control and IOs			
TEST	1	I (pd)	0: Normal operation. 1: Chip will be put in test mode
HRST_	38	I (pu)	Hardware reset (Low active)
GPIO0	2	B (pu)	Programmable I/O with pull-up resistor
GPIO1	3	B (pu)	Programmable I/O with pull-up resistor
GPIO2	5	B (pu)	Programmable I/O with pull-up resistor
GPIO3	6	B (pu)	Programmable I/O with pull-up resistor
GPIO4	8	B (pu)	Programmable I/O with pull-up resistor
GPIO5	9	B (pu)	Programmable I/O with pull-up resistor
GPIO6	11	B (pu)	Programmable I/O with pull-up resistor
GPIO7	41	B (pu)	Programmable I/O with pull-up resistor
GPIO8	37	B (pu)	Programmable I/O with pull-up resistor
GPIO9	48	B (pu)	Programmable I/O with pull-up resistor
5V to 3.3V LDO Regulator			
5VI	29	P	Power is supplied to this device from this pin which is required an input filter capacitor. In general, the input capacitor in the range of 1μF to 10μF is sufficient.
33VO	36	P	The output supplies power to loads. The output capacitor is required to prevent output voltage unstable. The GL3321G is stable with an output capacitor 1μF or greater. The larger output capacitor will be required for application with large transit load to limit peak voltage transits, besides could reduce output noise, improve stability, PSRR.
Power / Ground			
REG_SW	44	P	Switching Regulator 1.3V output
VREG	45	P	3.3V Switching Regulator Input
VREG	46	P	3.3V Switching Regulator Input
FB	47	A	1.3V voltage feedback and output
VDD13	4	P	1.3V Digital power
VDD13	10	P	1.3V Digital power
VDD13	40	P	1.3V Digital power
VP13	18	P	1.3V Analog power
VP13	21	P	1.3V Analog power

VP13	24	P	1.3V Analog power
VP13	30	P	1.3V Analog power
VP13	33	P	1.3V Analog power
VDD33	7	P	3.3V I/O power
VDD33	39	P	3.3V I/O power
VP33	14	P	3.3V Analog I/O power
VP33	17	P	3.3V Analog I/O power
VP33	25	P	3.3V Analog I/O power
GND	42	P	Ground
GND	43	P	Ground

Type Notation (in chip reset status)			
A	Analog	**P**	Power / Ground
B	Bi-direction	**f**	Floating
I	Input mode	**pd**	Internal pull-down
O	Output mode	**pu**	Internal pull-up
OSC	Oscillator		

CHAPTER 3 BLOCK DIAGRAM

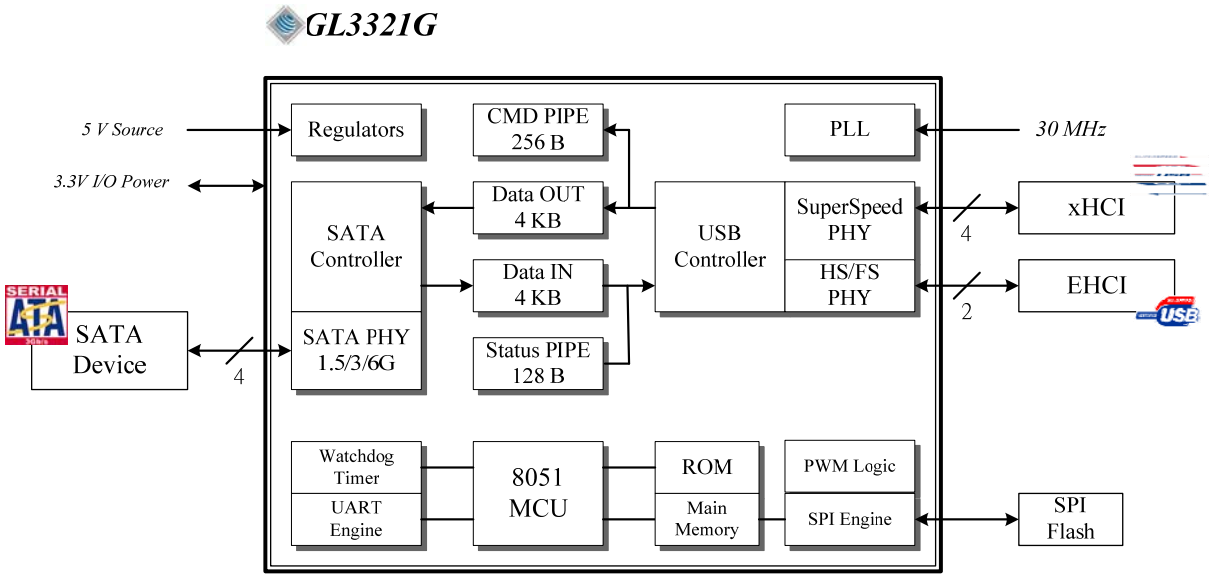


Figure 3.1 – GL3321G Block Diagram

CHAPTER 4 FUNCTION BLOCK DESCRIPTION

4.1 HS / FS PHY (UTM)

The USB 2.0 Transceiver Macrocell (UTM) is the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to the one compatible with the general logic.

4.2 SuperSpeed PHY

SuperSpeed PHY has elastic buffer and supports receiver detection, data serialization and de-serialization. Besides, it has PIPE interface with SuperSpeed Link Layer. The bandwidth is 32-bit wide, 125 MHz.

4.3 USB Controller

The USB Controller includes SIE for HS/FS and Link/Protocol Layer for SuperSpeed. The Serial Interface Engine, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions. The Link Layer transmits and receives Packets and Link commands. It also responses to change link power state. The Protocol Layer constructs Packet Information Structures for transmission and decomposes received Packet Information Structure.

4.4 EP0 / EP3 Buffer

Endpoint 0/3 Buffer: The Endpoint 0 (Control) FIFO is composed by 512-byte FIFO, and the Endpoint 3 (Interrupt) FIFO is composed by 32-byte FIFO.

4.5 CMD / Status / Data Buffer

CMD Buffer: It is composed by 256-byte FIFO, and it is used for command transfer between host and device.

Status Buffer: It is composed by 128-byte FIFO, and it is used for status transfer between host and device .

Data Buffer: It is composed by DATA IN and DATA out Bulk Buffer. These two 4K-byte data buffers which are used to store data transferred between USB host and SATA device.

4.6 SATA Controller

The SATA Controller includes Link, Transport, and Application Layer. The Link layer transmits and receives frames, transmits primitives based on control signals from the Transport layer, and receives primitives from the PHY layer which are converted to control signals to the Transport layer. The Transport layer constructs Frame Information Structures for transmission and decomposes received Frame Information Structure. The Application Layer translates the SATA operation onto internal protocols. The bandwidth is 32-bit wide, 37.5 MHz at SATA 1.5Gb/s, 75 MHz at SATA 3Gb/s, and 150 MHz at SATA 6Gb/s.

4.7 SATA PHY 1.5G / 3G / 6G

SATA PHY has elastic buffer and supports receiver detection, data serialization and de-serialization. It has SAPIS interface with SATA Link Layer.

4.8 8051 / MCU

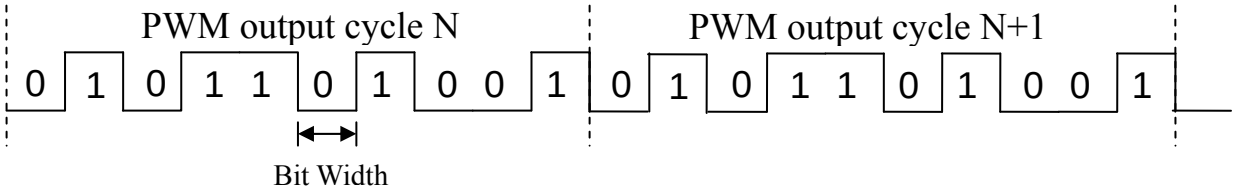
The 8051/MCU is a super fast microprocessor used for USB 3.0 application. It includes 64K-byte ROM, 16K-byte main memory SRAM for Cache, watchdog timer, and UART engine. The frequency is 30 MHz or 15MHz.

4.9 PWMs

Two PWMs are for FAN and LED controls, which are programmable for different frequency outputs. The PWM rate is from 12 MHz to 0.02 Hz.

Each output cycle of the PWM engine is defined 10 bits, and the value to be sent is set to PWMOP register. The output sequence of PWMOP is from bit 9 to bit 0, and then period cyclically repeats from bit 9. For example, the following figure shows while PWMOP set 169H.

Figure 4.1 – The PWM Output Waveform



The bit width in output cycle can set {WHE[4:0], WHH[7:0], WHM[7:0], WHL[7:0]} (offset 44h - 47h) to modulate and base on PWMCLK 1T (30MHz). Bit Width = 1T * 0x{WHE[4:0], WHH[7:0], WHM[7:0], WHL[7:0]}.

4.10 SPI Engines

SPI engine is to move code from external flash to the internal RAM

4.11 General Purpose IO Description

GL3321G provides multiple IO pins for various functions and strapping settings (as described in Table 4.1). The states of GPIOs are input mode before reset state, and then they are controlled by firmware after reset.

Table 4.1 – GPIO Descriptions

Pin Name	Pin Description	Type	Functionality	
			Input	Output
GPIO0	GPIO0 / SPI-MISO	I/O	SPI_MISO	
GPIO1	GPIO1 / SPI-SCK	I/O		SPI_CLK
GPIO2	GPIO2 / SPI-MOSI	I/O		SPI_MOSI
GPIO3	GPIO3 / SPI-SS0	I/O		SPI_SS0
GPIO4	GPIO4	I/O		
GPIO5	GPIO5 / SPI-SS1	I/O		SPI_SS1
GPIO6	GPIO6	I/O		
GPIO7	GPIO7	I/O		
GPIO8	GPIO8 / UART TX / ACTLED	I/O		UART TX output (debug) / LED1 (ACTIVITY)
GPIO9	GPIO9 / UART RX	I/O	UART RX (debug)	

CHAPTER 5 ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Table 5.1 – Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IO}	Digital I/O pad power supply voltage	2.97	3.3	3.63	V
Vcore	Digital power supply voltage	1.27	1.3	1.32	V
V_{AUSB2}	Analog power supply voltage for USB 2.0 PHY*	3.0	3.3	3.6	V
V_{AUSB3}	Analog power supply voltage for USB 3.0 PHY	1.27	1.3	1.32	V
V_{ASATA}	Analog power supply voltage for SATA PHY	1.27	1.3	1.32	V
V_{5VI}	USB VBus voltage	4.40		5.25	V
V_{reg}	Inductor type switching regulator input voltage	2.97	3.3	3.63	V
V_{ESD}	Static discharge voltage	4000			V
T_A	Ambient Temperature	0		70	℃
T_j	Junction Temperature	-40		125	℃

5.2 Temperature Conditions

Table 5.2 – Temperature Conditions

Item	Value
Storage Temperature	-65℃ ~ 150 ℃
Operating Temperature	0 ℃ ~ 70 ℃

5.3 DC Characteristics

5.3.1 I/O Type Digital Pins

Table 5.3 – I/O Type Digital Pins

Parameter	Min.	Typ.	Max.	Unit
I_{OL} Low Level Output Current @ 0.4V*	5.4	10.69	22.6	mA
I_{OH} High Level Output Current @ V_{IO} -0.2V*	3.2		13.0	mA
I_{OH} High Level Output Current @ V_{IO} -0.6V*	8.1		33.5	mA
V_{T+} Schmitt trigger low to high threshold point	-	1.29	-	V
V_{T-} Schmitt trigger high to low threshold point	-	0.81	-	V
R_{PU} Pad internal pull up resister @ (0V)*	16K	33K	48K	Ohms

R_{PD} Pad internal pull down resister @ (1.0* V_{IO})*	26K	51K	76K	Ohms
V_{IL} Input Low Voltage	-0.3	-	0.32 X V_{IO}	V
V_{IH} Input High Voltage	0.67 X V_{IO}	-		V
V_{OL} Output Low Voltage	-	-	0.3	V
V_{OH} Output High Voltage	2.2	-	-	V
30MHz clock rise time (20%-80% V_{IO})@10pF load*	0.47		1.77	ns
30MHz clock fall time (80%-20% V_{IO})@10pF load*	0.54		2.00	ns
I_{OZ} Tristate Output Leakage Current	-	-	1	uA

5.3.2 Reference Clock Input Requirement

Table 5.4 – Reference Clock Input Requirement

Parameter	Min.	Typ.	Max.	Unit
XIN crystal frequency		30 ± 60ppm		MHz
XIN cycle time*		33.33		ns

5.3.3 Reference Resistor Requirement

Table 5.5 – Reference Resistor Requirement

Parameter	Min.	Typ.	Max.	Unit
Reference Resistor		680(1%)		Ohms

5.3.4 XOUT Clock Output DC Characteristics

Table 5.6 – X2 Clock Output DC Characteristics

Parameter	Min.	Typ.	Max.	Unit
XOUT clock frequency		30 ± 60ppm		MHz
XOUT cycle time		33.33		ns

5.3.5 USB 2.0 Interface DC Characteristics

The GL3321G conforms to DC characteristics for Universal Serial Bus specification rev. 2.0. Please refer to this specification for more information.

5.3.6 USB 3.0 Interface DC Characteristics

The GL3321G conforms to DC characteristics for Universal Serial Bus specification rev. 3.0. Please refer to this specification for more information.

5.3.7 SATA Interface DC Characteristics

The GL3321G conforms to DC characteristics for Serial ATA specification rev. 3.0. Please refer to this specification for more information.

CHAPTER 6 POWER ON SEQUENCE

The power on reset of GL3321G can be triggered by external reset or internal power good reset. The internal power good reset is used to avoid whole chip power and clock unstable during power on. The period of external reset is necessary longer than internal power good reset. After external reset, GL3321G will start to work. The timing of power on reset is illustrated in the following figure.

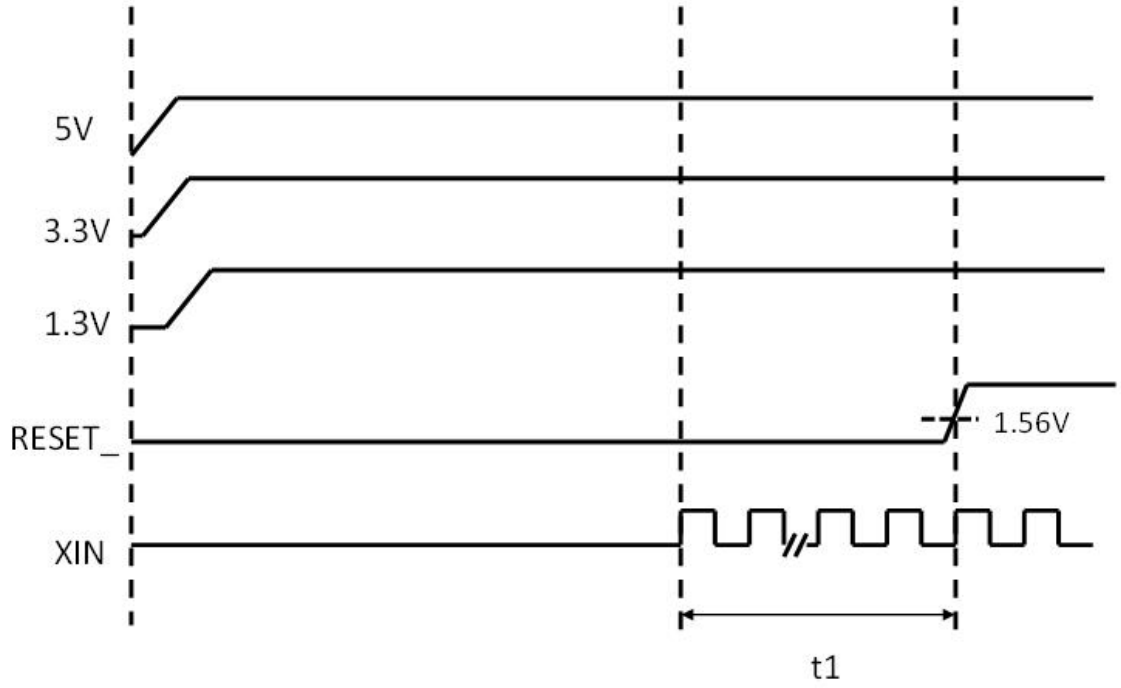
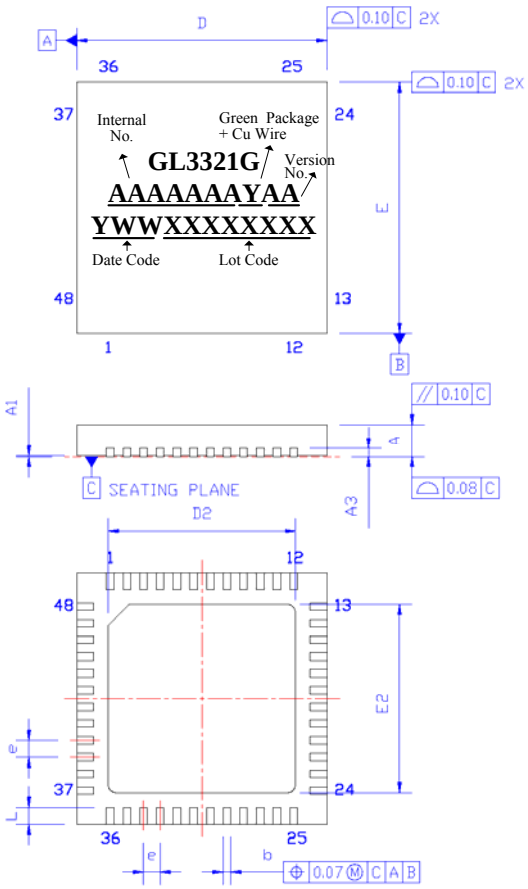


Figure 6.1 – GL3321G Power on sequence

Table 6.1 – Power On Sequence Timing Parameter

Parameter	Min.	Typ.	Max.	Unit
t1	1	-	-	Ms

CHAPTER 7 PACKAGE OUTLINE



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.13 (5.1)	0.18 (7.1)	0.25 (9.8)
D	6.00 (236.2) BSC		
D2	4.40 (173.2)	4.50 (177.2)	4.60 (181.1)
E	6.00 (236.2) BSC		
E2	4.40 (173.2)	4.50 (177.2)	4.60 (181.1)
e	0.40 (15.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

GL3321G 48-pin QFN Package

CHAPTER 8 ORDERING INFROMATION

Table 8.1 – Ordering Information

Part Number	Package	Green/Wire Material	Version	Status
GL3321G-ONYXX	QFN 48	Green Package + CU Wire	XX	Available