Genesys Logic, Inc.

GL3510-52

USB 3.1 Gen 1 Hub Controller

Datasheet

Revision 1.00
Jun. 03, 2021

Copyright

Ownership and Title

Genesys Logic, Inc. owns and retains of its right, title and interest in and to all materials provided herein. Genesys Logic, Inc. reserves all rights, including, but not limited to, all patent rights, trademarks, copyrights and any other propriety rights. No license is granted hereunder.

Disclaimer

All Materials are provided “as is”. Genesys Logic, Inc. makes no warranties, express, implied or otherwise, regarding their accuracy, merchantability, fitness for any particular purpose, and non-infringement of intellectual property. In no event shall Genesys Logic, Inc. be liable for any damages, including, without limitation, any direct, indirect, consequential, or incidental damages. The materials may contain errors or omissions. Genesys Logic, Inc. may make changes to the materials or to the products described herein at anytime without notice.

Genesys Logic, Inc.
13F., No. 205, Sec. 3, Beixin Rd., Xindian Dist. 231,
New Taipei City, Taiwan
Tel : (886-2) 8913-1888
Fax : (886-2) 6629-6168
http://www.genesyslogic.com

Revision History

Revision	Date	Description
1.00	06/03/2021	Formal release

Table of Contents

List of Figures

List of Tables

CHAPTER 1 GENERAL DESCRIPTION

Genesys GL3510 is a 4-port/2-port, low-power, and configurable hub controller. It is compliant with the USB 3.1 specification. GL3510 integrates Genesys Logic self-developed USB 3.1 Gen 1 Super Speed transmitter/receiver physical layer (PHY) and USB 2.0 High-Speed PHY. It supports Super Speed, Hi-Speed, and Full-Speed USB connections and is fully backward compatible to all USB 2.0 and USB 1.1 hosts. GL3510 has built-in 5V to 3.3V and 5V to 1.2V regulators, which saves customers' BOM cost, and eases for PCB design.

GL3510 features the native fast-charging and complies with USB-IF battery charging specification rev1.2, it could fast-charge Apple, Samsung Galaxy devices, and any device complaint with BC1.2/1.1. It also allows portable devices to draw up to 1.5A from GL3510 charging downstream ports (CDP[1]) or dedicated charging port (DCP[2]). It can enable systems to fast charge handheld devices even during "Sleep" and "Power-off" modes.

All available packages for GL3510 are listed as the following tables.

Product Series	Package Type	Number of DFPs	Power Mgmt.	LED Support
GL3510	QFN 64	4	Gang Mode	PGANG LED
GL3510	QFN 48	2	Gang Mode	PGANG LED

*Note: TT (transaction translator) implements the control logic defined in Section 11.14 ~ 11.22 of USB specification revision 2.0. TT basically handles the unbalanced traffic speed between the USPORT (operating in HS) and DSPORTS (operating in FS/LS) of hub.

[1] CDP, charging downstream port, the Battery Charging Rev.1.2-compliant USB port that does data communication and charges device up to 1.5A.

[2] DCP, dedicated charging port, the Battery Charging Rev.1.2-compliant USB port that only charges devices up to 1.5A, similar to wall chargers.

CHAPTER 2 FEATURES

- Compliant with USB 3.1 Gen 1 Specification
  - Upstream port supports SuperSpeed (SS), HighSpeed (HS) and FullSpeed (FS) traffic
  - Downstream ports support SS, HS, FS, and LowSpeed (LS) traffic
  - 1 control pipe and 1 interrupt pipe
  - Backward compatible to USB specification Revision 2.0/1.1
- Featuring fast-charging on all downstream ports and upstream port
  - Compliant with USB Battery Charging Revision v1.2, supporting CDP, DCP, and ACA-Dock
  - Downstream ports can be turned from a Standard Downstream Port (SDP) into Charging Downstream Port (CDP) or Dedicated Charging Port (DCP)
  - Downstream devices can be charged while upstream VBUS is not present, which can be applied on wall charger applications
  - Upstream port is capable of charging and data communicating simultaneously for portable devices supporting ACA-Dock or proprietary charging protocols
  - Supporting Apple 1A/2.1A/2.4A and Samsung Galaxy devices fast-charging
- On-chip 8-bit micro-processor
  - RISC-like architecture
  - USB optimized instruction set
  - 1 cycle instruction execution (maximum)
  - Performance: 12 MIPS @ 12.5MHz (maximum)
  - With 256-byte RAM, 20K-byte internal ROM, and 24K-byte SRAM
- Single Transaction Translator (TT) architecture
- Advanced power management and low power consumption
  - Supporting USB 3.1 U0/U1/U2/U3 power management states
  - Supporting USB Link Power Management (LPM) L0/L1/L2
  - Supporting low active power switch
- Configurable settings
  - Configurable charging port
  - Supporting compound-device (non-removable setting on downstream ports)
- Flexible design
  - Supporting Poly-fuse/Power-switch
  - Automatic switching between self-powered and bus-powered modes
  - Supporting electrical tuning for each specific port
  - Allow downstream ports to connect up to 8 devices, 4 x USB3.1 non-removable devices with 4 x USB2.0 non-removable devices or exposed ports
- Low BOM cost
  - Single external 25 MHz crystal / Oscillator clock input
  - Built-in upstream port 1.5KΩ pull-up and downstream port 15KΩ pull-down resistors
  - Built-in 5 to 3.3V and 5 to 1.2V regulator
- Applications
  - Standalone USB hub/Docking station
  - USB wall charger

CHAPTER 3 PIN ASSIGNMENT

3.1 Pin-out Diagram

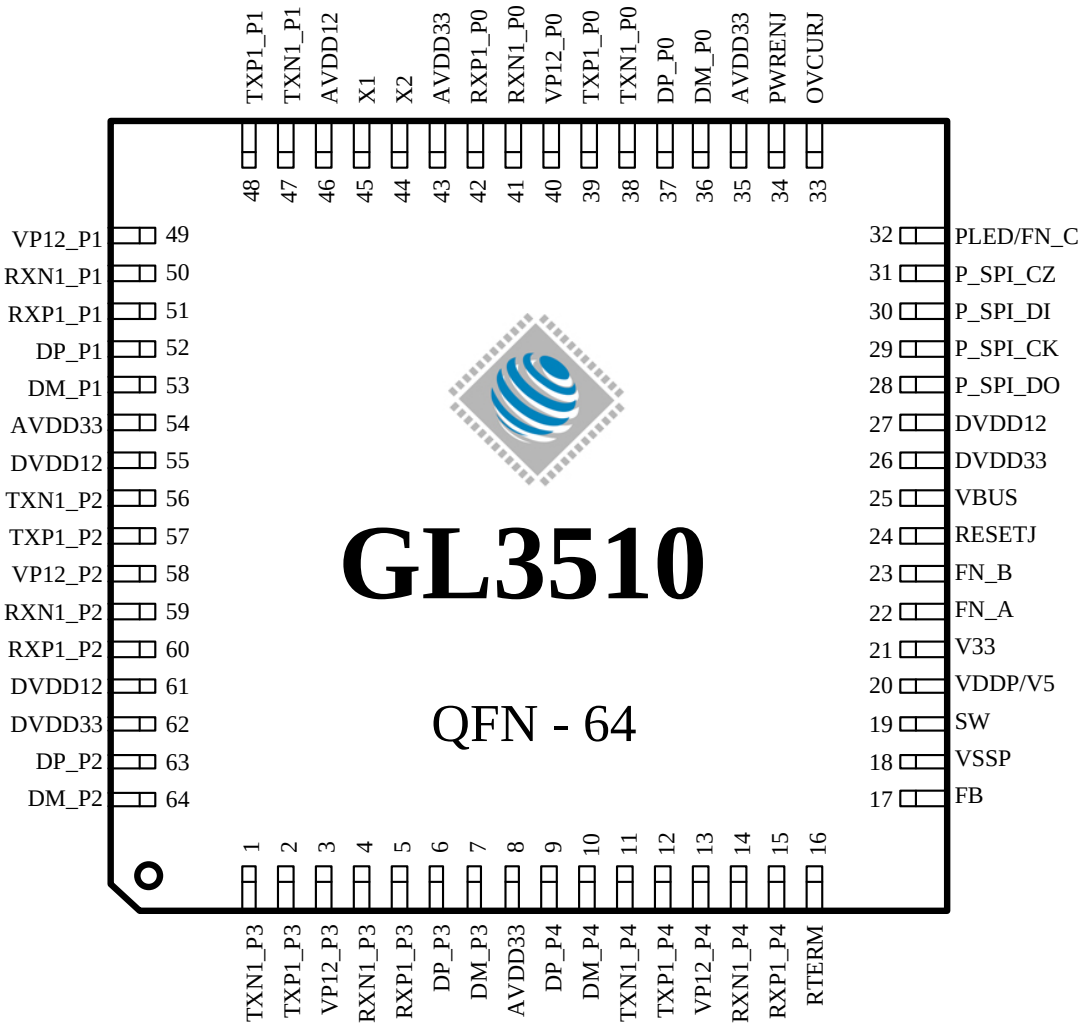


Figure 3.1 - QFN 64 (4-DFP) Pin-out Diagram

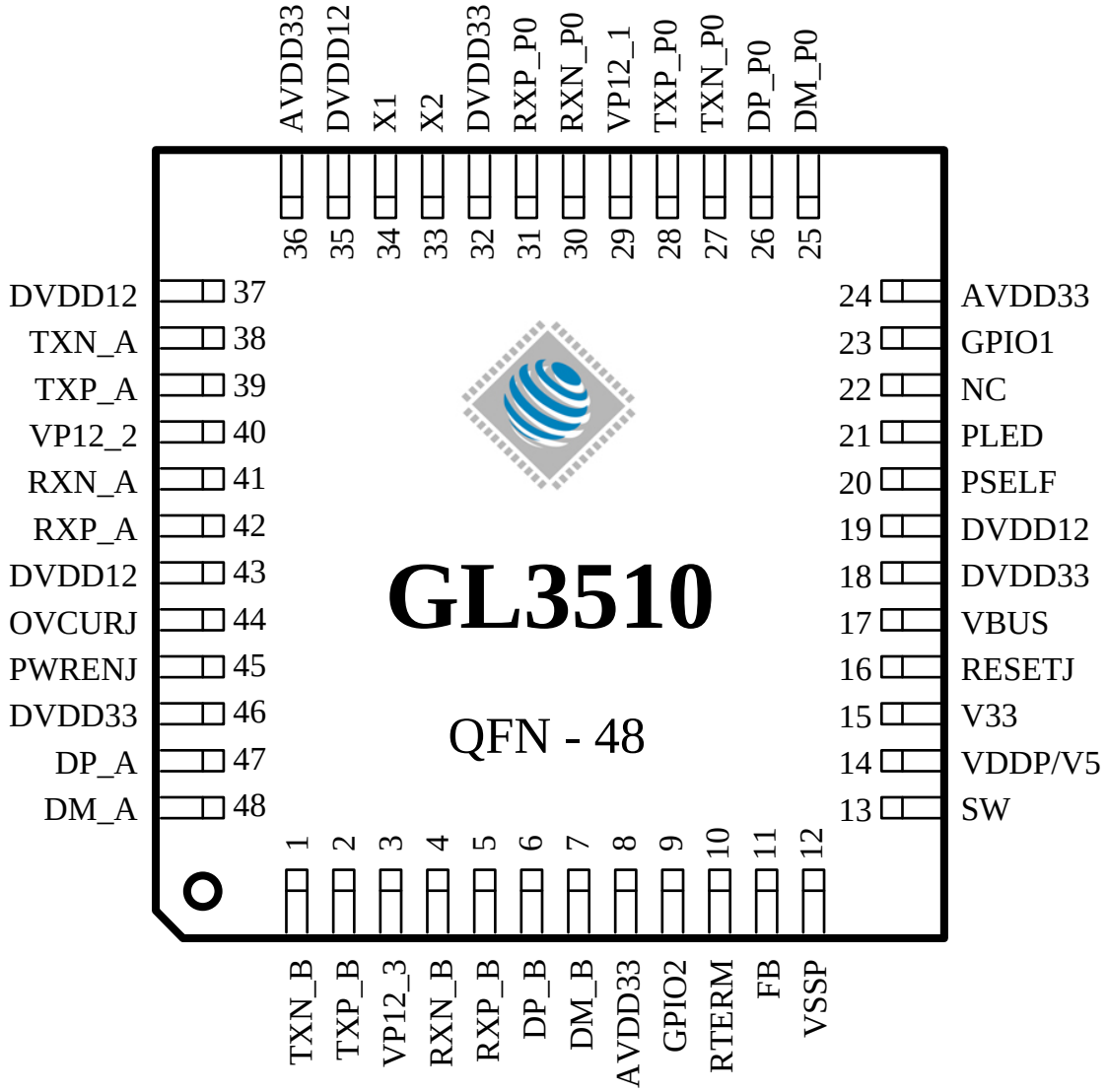


Figure 3.2 - QFN 48 (2-DFP) Pin-out Diagram

3.2 Pin Descriptions

USB Interface			
Pin Name	**QFN64**	**Type**	**Description**
TXN1_P0 TXP1_P0	38 39	O	USB3.1 Gen 1 Differential Data Transmitter TX-/TX+ of USPORT
RXN1_P0 RXP1_P0	41 42	I	USB3.1 Gen 1 Differential Data Receiver RX-/RX+ of USPORT
TXN1_P1 TXP1_P1	47 48	O	USB3.1 Gen 1 Differential Data Transmitter TX-/TX+ of DSPORT1
RXN1_P1 RXP1_P1	50 51	I	USB3.1 Gen 1 Differential Data Receiver RX-/RX+ of DSPORT1
TXN1_P2 TXP1_P2	56 57	O	USB3.1 Gen 1 Differential Data Transmitter TX-/TX+ of DSPORT2
RXN1_P2 RXP1_P2	59 60	I	USB3.1 Gen 1 Differential Data Receiver RX-/RX+ of DSPORT2
TXN1_P3 TXP1_P3	1 2	O	USB3.1 Gen 1 Differential Data Transmitter TX-/TX+ of DSPORT3
RXN1_P3 RXP1_P3	4 5	I	USB3.1 Gen 1 Differential Data Receiver RX-/RX+ of DSPORT3
TXN1_P4 TXP1_P4	11 12	O	USB3.1 Gen 1 Differential Data Transmitter TX-/TX+ of DSPORT4
RXN1_P4 RXP1_P4	14 15	I	USB3.1 Gen 1 Differential Data Receiver RX-/RX+ of DSPORT4
DM_P0 DP_P0	36 37	B	USB 2.0 DM/DP for USPORT
DM_P1 DP_P1	53 52	B	USB 2.0 DM/DP for DSPORT1
DM_P2 DP_P2	64 63	B	USB 2.0 DM/DP for DSPORT2
DM_P3 DP_P3	7 6	B	USB 2.0 DM/DP for DSPORT3
DM_P4 DP_P4	10 9	B	USB 2.0 DM/DP for DSPORT4

USB Interface			
Pin Name	**QFN48**	**Type**	**Description**
TXN_P0 TXP_P0	27 28	O	USB3.1 Gen 1 Differential Data Transmitter TX-/TX+ of USPORT
RXN_P0 RXP_P0	30 31	I	USB3.1 Gen 1 Differential Data Receiver RX-/RX+ of USPORT
TXN_A TXP_A	38 39	O	USB3.1 Gen 1 Differential Data Transmitter TX-/TX+ of DSPORT2
RXN_A RXP_A	41 42	I	USB3.1 Gen 1 Differential Data Receiver RX-/RX+ of DSPORT2
TXN_B TXP_B	1 2	O	USB3.1 Gen 1 Differential Data Transmitter TX-/TX+ of DSPORT3

RXN_B RXP_B	4 5	I	USB3.1 Gen 1 Differential Data Receiver RX-/RX+ of DSPORT3
DM_P0 DP_P0	25 26	B	USB 2.0 DM/DP for USPORT
DM_A DP_A	48 47	B	USB 2.0 DM/DP for DSPORT2
DM_B DP_B	7 6	B	USB 2.0 DM/DP for DSPORT3

Hub Interface				
Pin Name	**QFN64**	**QFN48**	**Type**	**Description**
PWRENJ	34	45	B	1. PWRENJ is the only power-enable output for GANG mode. 2. Strapping for Power Switch or PolyFuse ▪ Pull high to support low-active power switch ▪ Floating to support poly-fuse ▪ Pull down to support high-active power switch
OVCURJ	33	44	I (pu)	OVCURJ is the only over current flag for GANG mode.
FN_A	22	-	B	Strapping for Port 3 Configuration ▪ Floating to set downstream port 3 as non-removable port ▪ Pull high to be over current indicator for downstream port 3
FN_B	23	-	B	Strapping for Port 4 Configuration ▪ Pull down to disable downstream port 4 ▪ Floating to set downstream port 4 as non-removable port ▪ Pull high to be over current indicator for downstream port 4
GPIO1		23	B	General purpose I/O reserved. Pull High : BC1.2 Enable Pull Low : BC1.2 Disable Floating : BC1.2 Disable
GPIO2		9	B	General purpose I/O reserved. Pull High : No Strapping Pull Low : Port Disabled for Port_B Floating : Set Port_B as Non_Removable
PSELF		20	B	0: Self power mode 1: Bus power mode.
PLED/FN_C	32	21	B	1. PGANG LED 2. Strapping for Charger (not applied to QFN48). ▪ Pull down to disable charging on all downstream ports ▪ Pull high to enable charging on all downstream ports

Clock and Reset Interface				
Pin Name	**QFN64**	**QFN48**	**Type**	**Description**
X1	45	34	I	Crystal / OSC clock input
X2	44	33	O	Crystal clock output.
RESETJ	24	16	I (pd)	Active low. External reset input, default pull high 10KΩ. When RESET# = low, whole chip is reset to the initial state.

SPI Interface				
Pin Name	**QFN64**	**QFN48**	**Type**	**Description**
P_SPI_CK	29	-	B	For SPI data clock
P_SPI_CZ	31	-	B	For SPI data chip enable
P_SPI_DO	28	-	B	For SPI data Input
P_SPI_DI	30	-	B	For SPI data Output

Power/Ground Interface			
Pin Name	**QFN64**	**Type**	**Description**
VP12_P0~P4	40,49,583,13	P	Analog 1.2V power input for Analog circuit
AVDD12	46	P	Analog 1.2V power input for Analog PLL circuit
DVDD12	27,55,61	P	1.2V digital power input for digital circuits
DVDD33	26,62	P	3.3V digital power input for digital circuits
AVDD33	8,35, 43,54	P	Analog 3.3V power input
VBUS	25	I	VBUS valid input
V33	21	P	5V-to-3.3V regulator Vout & 3.3 input
V5	20	P	5V Power input. If using external regulator, V5 pin should be connected with 3.3V.

Power/Ground Interface			
Pin Name	**QFN48**	**Type**	**Description**
VP12_1~3	29,40,3	P	Analog 1.2V power input for Analog circuit
AVDD12	-	P	Analog 1.2V power input for Analog PLL circuit
DVDD12	19,35, 37,43	P	1.2V digital power input for digital circuits
DVDD33	18,32, 46	P	3.3V digital power input for digital circuits
AVDD33	8,24,36	P	Analog 3.3V power input
VBUS	17	I	VBUS valid input
V33	15	P	5V-to-3.3V regulator Vout & 3.3 input
V5	14	P	5V Power input. If using external regulator, V5 pin should be connected with 3.3V.

Switching Regulator (5V to 1.2V)				
Pin Name	**QFN64**	**QFN48**	**Type**	**Description**
FB	17	11	A	Switcher Feedback Voltage. This pin is the inverting input of the error amplifier. VOUT senses the switcher output through an external resistor divider network. For the fixed voltage version, connect this pin to the output voltage.

SW	19	13	A	Internal Switches Output. Connect this pin to the output inductor.
VDDP	20	14	P	Dedicated 5V power input for embedded switching regulator
VSSP	18	12	P	Dedicated Ground for embedded switching regulator

Miscellaneous Interface				
Name	**QFN64**	**QFN48**	**Type**	**Description**
RTERM	16	10	A	A 20Kohm resister must be connected between RTERM and Ground

Note: Analog circuits are quite sensitive to power and ground noise, so please take care the power routing and the ground plane for PCB design. For detailed information, please refer to **USB3.1 Hub Design Guide**.

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	P	Power / Ground
	A	Analog
	pu	Internal pull up
	pd	Internal pull down

CHAPTER 4 FUNCTION DESCRIPTION

4.1 Functional Block

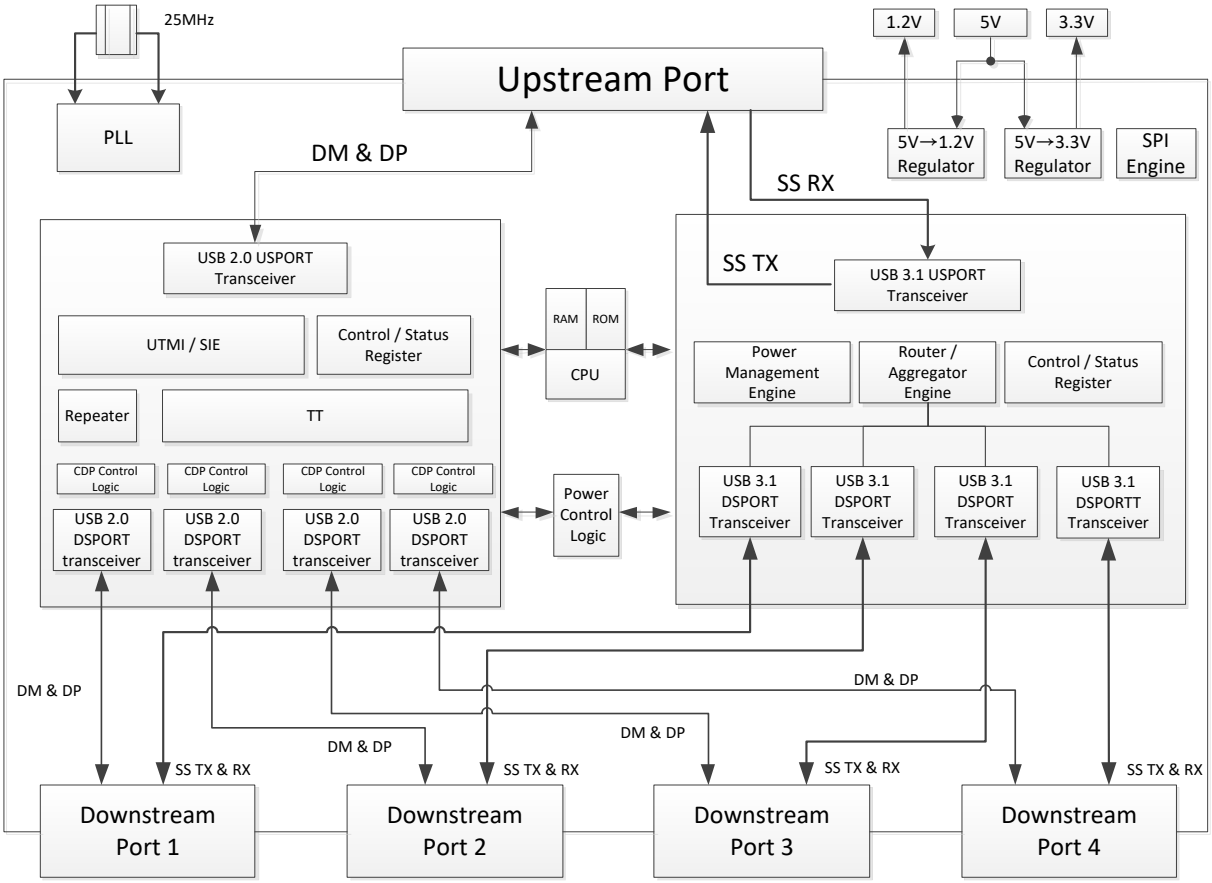


Figure 4.1 – Architecture Diagram

4.2 General Description

4.2.1 USB 2.0 USPORT Transceiver

USB 2.0 USPORT (upstream port) transceiver is the analog circuit that supports both full-speed and high-speed electrical characteristics defined in Chapter 7 of USB specification revision 2.0. USPORT transceiver will operate in full-speed electrical signaling when GL3510 is plugged into a 1.1 host/hub. USPORT transceiver will operate in high-speed electrical signaling when GL3510 is plugged into a 2.0 host/hub.

4.2.2 USB 3.1 Gen 1 USPORT Transceiver

USB3.1 Gen 1 USPORT (upstream port) transceiver is the analog circuit that has elastic buffer and supports receiver detection, data serialization and de-serialization. Besides, it has PIPE interface with SuperSpeed Link Layer

4.2.3 PLL (Phase Lock Loop)

PLL generates the clock sources for the whole chip. The generated clocks are proven quite accurate that help in generating high speed signal without jitter.

4.2.4 Regulator

GL3510 build in internal regulators convert 5V input to 3.3V/1.2V output.

4.2.5 RAM/ROM/CPU

The micro-processor unit of GL3510 is an 8-bit RISC processor with 20K-byte ROM and 256-bytes RAM. It operates at 12MIPS of 12 MHz clock(maximum) to decode the USB command issued from host and then prepares the data to respond to the host.

4.2.6 UTMI (USB 2.0 Transceiver Microcell Interface)

UTMI handles the low level USB protocol and signaling. It's designed based on the Intel's UTMI specification 1.01. The major functions of UTMI logic are to handle the data and clock recovery, NRZI encoding/decoding, Bit stuffing /de-stuffing, supporting USB 2.0 test modes, and serial/parallel conversion.

4.2.7 SIE (Serial Interface Engine)

SIE handles the USB protocol defined in Chapter 8 of USB specification revision 2.0. It co-works with μC to play the role of the hub kernel. The main functions of SIE include the state machine of USB protocol flow, CRC check, PID error check, and timeout check. Unlike USB 1.1, bit stuffing/de-stuffing is implemented in UTMI, not in SIE.

4.2.8 Control/Status Register

Control/Status register is the interface register between hardware and firmware. This register contains the information necessary to control endpoint0 and endpoint1 pipelines. Through the firmware based architecture, GL3510 possesses higher flexibility to control the USB protocol easily and correctly.

4.2.9 Power Management Engine

The power management of GL3510 is compliant with USB3.1 Gen 1 specification. When operating in SuperSpeed mode, GL3510 supports U0, U1, U2, and U3 power states. U0 is the functional state. U1 and U2 are lower power states compared to U0. U1 is a low power state with fast exit to U0; U2 is a low power state which saves more power than U1 with slower exit to U0. U3 is suspend state, which is the most power-saving state, with tens of milliseconds exit to U0. Unlike USB 2.0, SuperSpeed packet traffic is unicast rather than broadcast. Packet only travels the direct path in-between host and the target device. SuperSpeed traffic will not reach an unrelated device. When enabled for U1/U2 entry, and there is no pending traffic within comparable exit latency, GL3510 will initiate U1/U2 entry to save the power. On the other hand, the link partner of GL3510 may also initiate U1/U2 entry. In this case, GL3510 will accept or

reject low power state entry according to its internal condition.

4.2.10 Router/Aggregator Engine

Router/Aggregator Engine implements the control logic defined in Chapter10 of USB 3.1 specification. Router/Aggregator Engine uses smart method for route packet to device or aggregate packet to host.

4.2.11 REPEATER

Repeater logic implements the control logic defined in Section 11.4 and Section 11.7 of USB specification revision 2.0. REPEATER controls the traffic flow when upstream port and downstream port are signaling in the same speed. In addition, REPEATER will generate internal resume signal whenever a wakeup event is issued under the situation that hub is globally suspended.

4.2.12 TT

TT implements the control logic defined in section 11.14 ~ 11.22 of *USB specification Revision 2.0*. TT basically handles the unbalanced traffic speed between the USPORT (operating in HS) and DSPORTS (operating in FS/LS) of hub. GL3510 adopts the single TT architecture to provide the most cost effective solution. Single TT shares the same buffer control module for each downstream port.

4.2.12.1 Connected to 1.1 Host/Hub

If an USB 2.0 hub is connected to the downstream port of an USB 1.1 host/hub, it will operate in USB 1.1 mode. For an USB 1.1 hub, both upstream direction traffic and downstream direction traffic are passing through REPEATER. That is, the REPEATER/TT routing logic will route the traffic channel to the REPEATER.

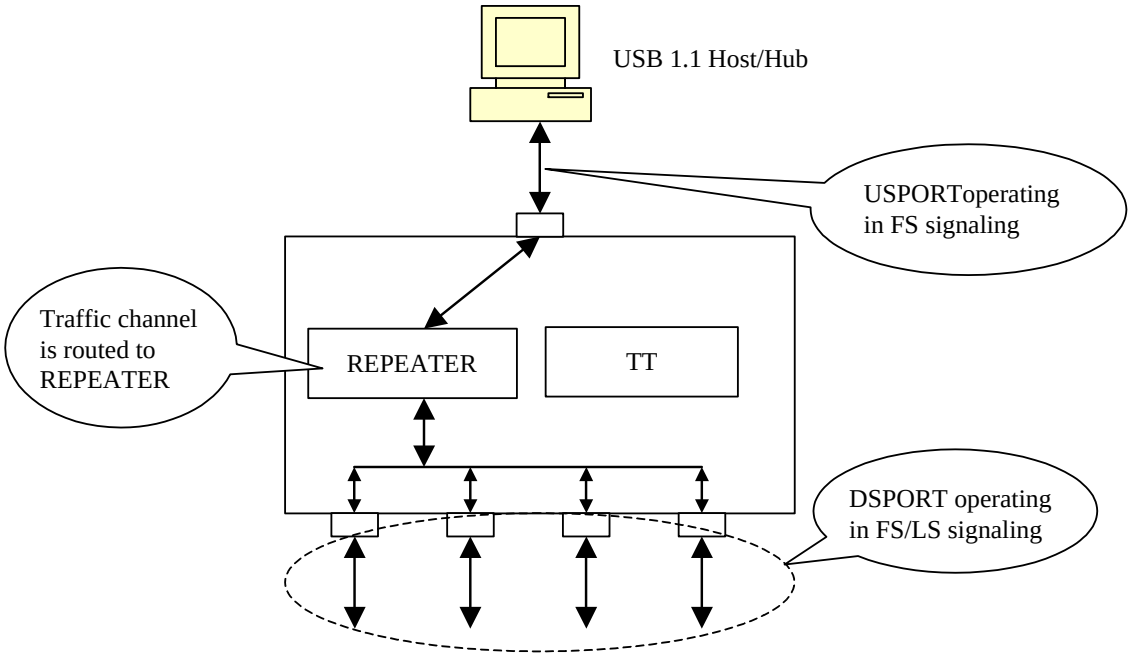


Figure 4.2 - Operating in USB 1.1 Schemes

4.2.12.2 Connected to USB 2.0 Host/Hub

If an USB 2.0 hub is connected to an USB 2.0 host/hub, it will operate in USB 2.0 mode. The upstream port signaling is in high speed with bandwidth of 480 Mbps under this environment. The traffic channel will then be routed to the REPEATER when the device connected to the downstream port is signaling also in high speed. On the other hand, the traffic channel will then be routed to TT when the device connected to

the downstream port is signaling in full/low speed.

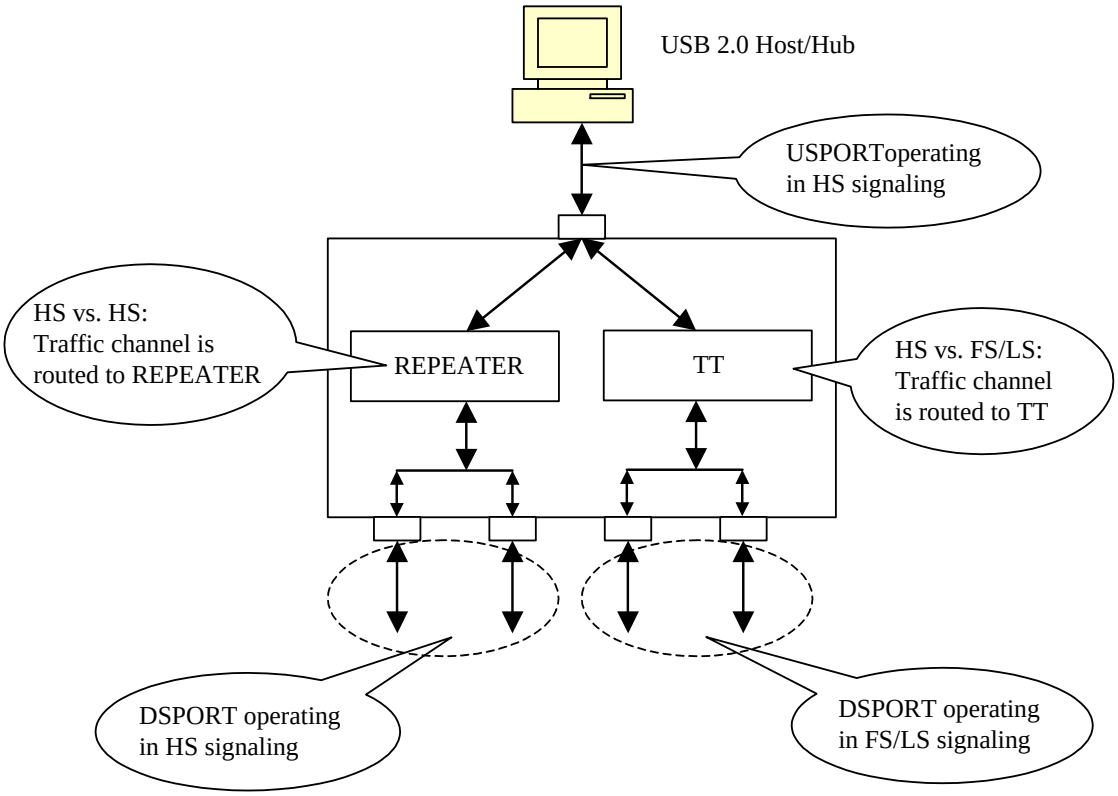


Figure 4.3 - Operating in USB 2.0 Schemes

4.2.13 CDP Control Logic

CDP (charging downstream port) control logic implements the logic defined in USB Battery charging specification revision 1.2. The major function of it is to control DSPORT Transceiver to make handshake with a portable device which is compliant with USB Battery charging spec rev1.2 as well. After recognizing charging detection each other, portable device will draw up to 1.5A from VBUS to fast charge its battery.

4.2.14 USB 3.1 Gen 1/USB 2.0 DSPORT Transceiver

DSPORT transceiver is the analog circuit that supports high-speed, full-speed, and low-speed electrical characteristics. In addition, each DSPORT transceiver accurately controls its own squelch level to detect the detachment and attachment of devices.

4.3 Configuration and I/O Settings

4.3.1 RESET Setting

GL3510's power on reset can either be triggered by external reset or internal power good reset circuit. The external reset pin, RESETJ, is connected to upstream port Vbus (5V) to sense the USB plug / unplug or 5V voltage drop. The reset trigger voltage can be set by adjusting the value of resistor R1 and R2 (Suggested value refers to schematics) GL3510's internal reset is designed to monitor silicon's internal core power (1.2V) and initiate reset when unstable power event occurs. The power on sequence will start after the power good voltage has been met, and the reset will be released after approximately 40 μS after power good. GL3510's reset circuit as depicted in the picture.

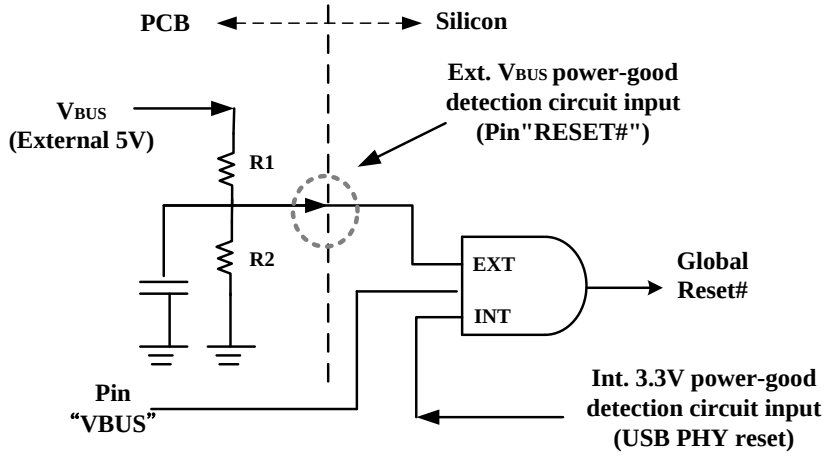


Figure 4.4 - Power on Reset Diagram

To fully control the reset process of GL3510, we suggest the reset time applied in the external reset circuit should longer than that of the internal reset circuit. Timing of POR is illustrated as below figure.

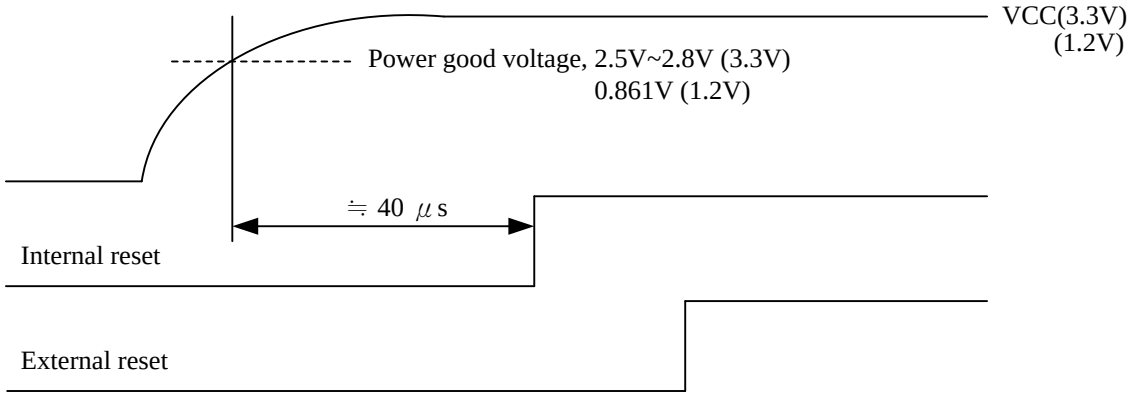


Figure 4.5 - Power on Sequence of GL3510

4.3.2 SELF/BUS Power Setting

By setting PSELF, GL3510 can be configured as a bus-power or a self-power hub.

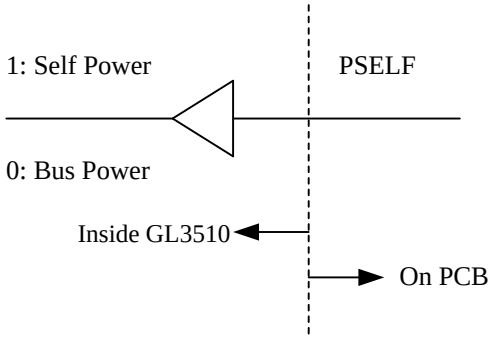


Figure 4.6 - SELF/BUS Power Setting

4.3.3 LED Connections

GL3510 uses PLED pin to indicate the suspend flag. GL3510 outputs the suspend flag once it is globally suspended. In figure 4.7, we depict the suspend LED indicator schematics. It should be noticed that the polarity of LED must be followed, otherwise the suspend current will be over spec limitation (2.5mA).

GL3510 controls the LED lighting according to the flow defined in Section 11.5.3 of Universal Serial Bus Specification Revision2.0. Both manual mode and Automatic mode are supported in GL3510. When GL3510 is globally suspended, GL3510 will turn off the LED to save power.

4.3.4 Power Switch Enable Polarity

Both low/high-enabled power switches are supported. It is determined by jumper setting.
The power switch polarity will be configured by the state of pin PWREN pin, as the following table.

Table 4.1 - Configuration by Power Switch Type

PWRENJ	Power Switch Enable Polarity
0	High-active
1	Low-active

4.3.5 Port Configuration

Downstream port 4 can be disabled by pin strapping, which extends the flexibility for PCB design and more applications. Please refer to GL3510 schematic for more details.

4.3.6 Non-removable Port Setting

For compound applications or embedded systems, downstream ports that always connect inside the system can be set as non-removable by firmware configuration and pin strapping. Please refer to **Genesys USB3.1 Hub FW ISP Tool User Guide** for the detailed setting information.

CHAPTER 5 FAST CHARGING SUPPORT

5.1 Introduction to Battery Charging Specification Rev.1.2

The USB ports on personal computers are convenient places for portable devices to draw current for charging their batteries. This convenience has led to the creation of dedicated chargers that simply expose a USB standard-A receptacle. This allows portable devices to use the same USB cable to charge from either a PC or from a dedicated charger.

If a portable device is attached to a USB host or hub, then the USB 2.0 specification requires that after connecting, a portable device must draw less than:

- 2.5 mA average if the bus is suspended
- 100 mA maximum if bus is not suspended and not configured
- 500 mA maximum if bus is not suspended and configured for 500 mA

If a portable device is attached to a charging host or hub, it is allowed to draw a current up to 1.5A, regardless of suspend. In order for a portable device to determine how much current it is allowed to draw from an upstream USB port, the USB-IF Battery Charging specification defines the mechanisms that allow the portable device to distinguish between a USB standard host, hub or a USB charging host. Since portable devices can be attached to USB charging ports from various manufactures, it is important that all USB charging ports behave the same way. This specification also defines the requirements for a USB chargers and charging downstream ports.

5.2 Standard Downstream Port (SDP)

GL3510 complies with Battery Charging Specification rev1.2, which defines three charging ports: SDP, CDP and DCP. The SDP is a standard USB port which can transfer data and provide maximum 500mA current.

5.3 Charging Downstream Port (CDP)

GL3510 supports battery charging detection, turning its downstream port from a standard downstream port (SDP) into charging downstream port (CDP). GL3510 will make physical layer handshaking when a portable device that complies with BC rev1.2 attaches to its downstream port. After physical layer handshaking, a portable device is allowed to draw more current up to 1.5A.

Once the charging downstream port of GL3510 is enabled, it will monitor the V_{DP_SRC} on D+ line anytime. When a portable device, which is compliant with BC rev1.2, is attached to the downstream port, it will drive V_{DP_SRC} on D+ line to initiate the handshake with charging downstream port. GL3510 will response on its D- line by V_{DM_SRC} and keep in a certain period of time and voltage level. The portable device will accept this handshaking on its D- line in correct timing period and voltage level, and then turns off its V_{DP_SRC} on D+ line. GL3510 will recognize that charging negotiation is finished by counting time between the portable device turning on and off its V_{DP_SRC}. After that, the portable device can start to draw more current from VBUS to charge its battery more rapidly. It can draw current up to 1.5A.

If there is no response from D- line, the portable device will recognize that it is attached to a standard downstream port, not a charging port.

5.4 Dedicated Charging Port (DCP)

GL3510 also supports dedicated charging port, which is a downstream port on a device that outputs power through a USB connector, but it is not capable of enumerating a downstream device. With the adequate system circuit design, GL3510 will turn its downstream port from a standard downstream port (SDP) into dedicated charging port (DCP), i.e short the D+ line to the D- line, to let the portable device draws current up to 1.5A. Please refer to the **USB3.1 Hub Design Guide** document for the detailed information.

5.5 ACA-Dock

An ACA-Dock is a docking station that has one upstream port, and zero or more downstream ports. The upstream port can be attached to a portable device (PD), and is capable of sourcing ICDP to the PD, which means that the upstream port can charge and have data communication with the PD at the same time. Please refer to Battery Charging Spec v1.2 for more details.

5.6 Apple and Samsung Devices

GL3510 Hub not only supports BC1.2, but also supports fast-charging for Apple 1A/2.4A and Samsung Galaxy devices.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Maximum Ratings

Table 6.1 - Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_5	5V Power Supply	-0.5	+6.0	V
V_{DD}	3.3V Power Supply	-0.5	+3.6	V
VDDcore	1.2VPower Supply	-0.5	+1.32	V
V_{IN}	3.3V Input Voltage for digital I/O(EE_DO) pins*	-0.5	+5	V
Vincore	1.2V	-0.5	+1.32	V
V_{INUSB}	Input Voltage for USB signal (DP, DM) pins	-0.5	+3.6	V
T_S	Storage Temperature under bias	-60	+100	ºC
F_{OSC}	Frequency	25 MHz ± 0.03%		

*Please refer to the reference design schematic.

6.2 Operating Ranges

Table 6.2 - Operating Ranges

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_5	5V Power Supply	4.75	5.0	5.25	V
V_{DD}	3.3V Power Supply	3.0	3.3	3.6	V
VDDcore	1.2V Power Supply	1.15	1.2	1.32	V
V_{IND}	Input Voltage for digital I/O pins	-0.5	3.3	3.6	V
V_{INUSB}	Input Voltage for USB signal (DP, DM) pins	0.5	3.3	3.6	V
T_A	Ambient Temperature	0	-	70	ºC
T_J	Absolute maximum junction temperature	0	-	125	ºC

6.3 DC Characteristics

6.3.1 DC Characteristics except USB Signals

Table 6.3 - DC Characteristics except USB Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	3	3.3	3.6	V
V_{IL}	LOW level input voltage	-	-	1	V
V_{IH}	HIGH level input voltage	1.4	-	-	V
V_{TLH}	Schmitt trigger PAD*-LOW to HIGH threshold voltage	1.7	-	-	V
V_{THL}	Schmitt trigger PAD*- HIGH to LOW threshold voltage	-	-	0.7	V
V_{OL}	LOW level output voltage when I_{OL}=8mA	-	-	0.4	V
V_{OH}	HIGH level output voltage when I_{OH}=8mA	2.4	-	-	V
I_{OLK}	Leakage current for pads with internal pull up or pull down resistor	-	-	30	μA
R_{DN}	Pad internal pull down resister	232	378	647	KΩ
R_{UP}	Pad internal pull up resister	276	435	718	KΩ

* Schmitt trigger pads are VBUS, RESET

6.3.2 USB 2.0 Interface DC Characteristics

GL3510 conforms to DC characteristics for Universal Serial Bus specification rev. 2.0. Please refer to the specification for more information.

6.3.3 USB 3.1 Gen 1 Interface DC Characteristics

GL3510 conforms to DC characteristics for Universal Serial Bus 3.1 specification. Please refer to the specification for more information.

6.4 Power Consumption

GL3510 integrates 5V-to-3.3V and 5V-to-1.2V regulators. If supplying 5V power, internal regulators convert 5V to 3.3V and 1.2 V, and power consumed in 5V domain in the following table already includes 1.2V and 3.V power consumption and conversion loss. In other words, if using 5V as input power, 1.2V and 3.3V power can be ignored; if using external 1.2V and 3.3V power as input sources, the total power consumption will be the sum of 1.2V and 3.3V.

Number of Active USB 3.1 Ports	Using 5V power input		Using 1.2V and 3.3V power input				Unit
	5V		1.2V		3.3V		
	Config.	Read/ Write	Config.	Read/ Write	Config.	Read/ Write	
Reset	6		1.6		2		mW
Suspend	12.5		6		3.3		mW
0	140	-	16	-	80	-	mW
1	455	455	285	286	80	80	mW
2	590	592	389	391	80	80	mW
3	760	789	494	500	80	80	mW
4	920	935	600	605	80	80	mW

Number of Active USB 2.0 Ports	Using 5V power input		Using 1.2V and 3.3V power input				Unit
	5V		1.2V		3.3V		
	Config.	Read/ Write	Config.	Read/ Write	Config.	Read/ Write	
Reset	6		1.6		2		mW
Suspend	12.5		6		3.3		mW
0	140	-	16	-	79	-	mW
1	170	212	16	16	98	125	mW
2	199	273	16	16	117	164	mW
3	228	310	16	16	138	188	mW
4	259	342	16	16	158	210	mW

Note:

Test result represents silicon level operating current without considering additional power consumption contributed by external over-current protection circuit. The power consumption could be different depending on configurations.

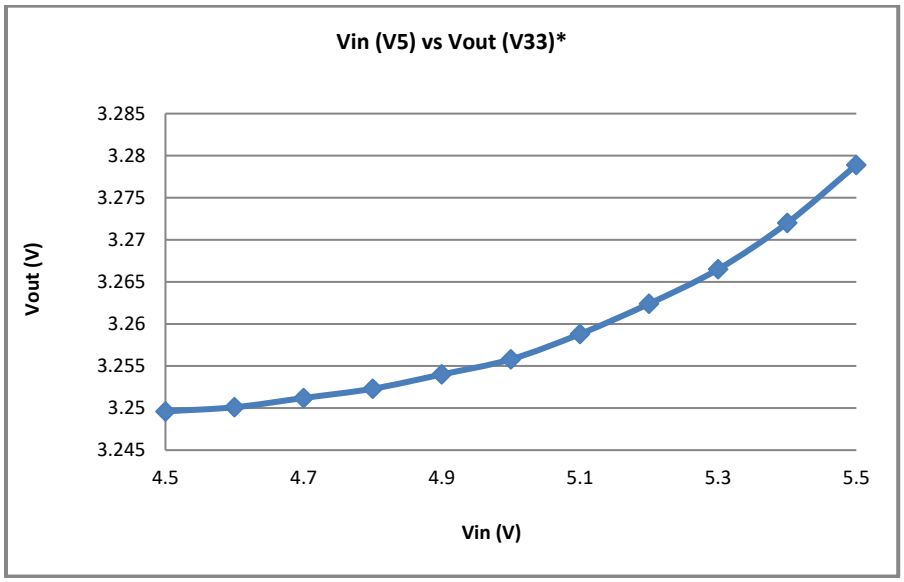
6.5 On-Chip Power Regulator

GL3510 requires 3.3V and 1.2V source power for normal operation of internal core logic and USB physical layer (PHY). There are two kinds of regulators integrated in GL3510; one is low-drop power regulator converts 5V power input from USB cable (Vbus) to 3.3V voltage for silicon power source; another one is DC-DC switching regulator converts 5V to 1.2 V. The 3.3V and 1.2V power output are guaranteed by internal voltage reference circuits to prevent unstable 5V power compromise USB data integrity. The regulators' maximum currents loading are 250mA (5-3.3V) and 0.8A (5-1.2V), which provide enough tolerance for normal GL3510 operation (below 100mA).

6.5.1 5V to 3.3V Regulator

5V to 3.3V On-chip Power Regulator features are described as follows.

- 5V to 3.3V low-drop power regulator
- 250mA maximum output driving capability
- Provide stable 3.3V output when Vin = 4.5V~5.5V
- 125uA maximum quiescent current (typical 80uA).



*Note: Measured environment: Ambient temperature = 25℃,
Current Loading = 250mA

Figure 6.1 - Vin(V5) vs Vout(V33)*

6.5.2 5V to 1.2V Regulator

5V to 1.2V DC-DC Switching Regulator features are described as follows.

- 5V to 1.2V DC-DC switching regulator
- 0.8A maximum output driving capability

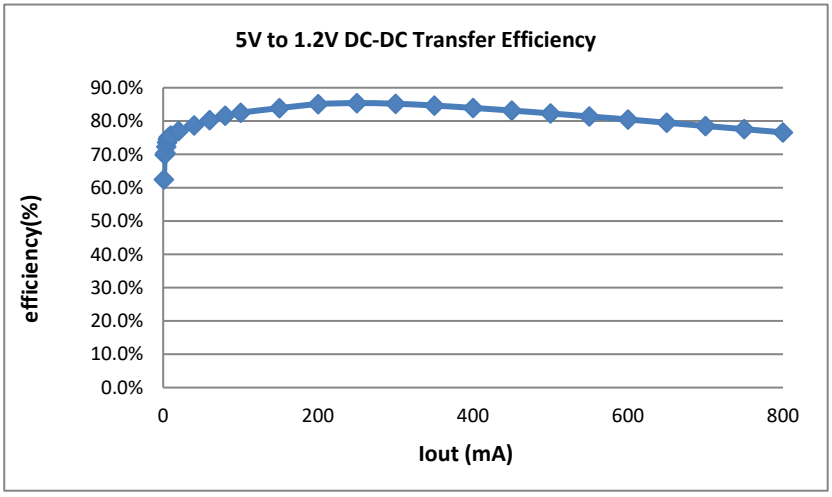
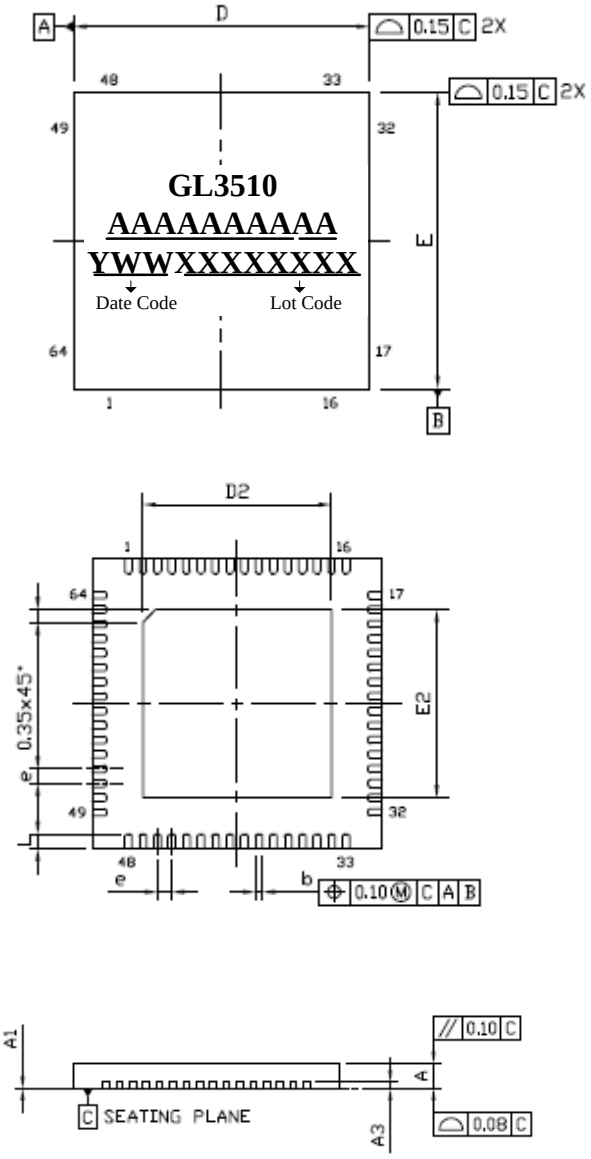


Figure 6.2 - Vin (V5) vs. Vout (V1.2)

6.6 External Clock

XOUT: 25MHz crystal oscillator output. It should be left open if an external clock source is used.
XIN: 25MHz crystal oscillator input. If an external 3.3V clock source is used, its frequency has to be 25MHz +/-300ppm with a peak-to-peak jitter less than 50ps..

CHAPTER 7 PACKAGE DIMENSION



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.15 (5.9)	0.20 (7.9)	0.25 (9.8)
D	8.00 (315.0) BSC		
D2	4.10 (161.4)	5.35 (210.6)	6.60 (259.8)
E	8.00 (315.0) BSC		
E2	4.10 (161.4)	5.35 (210.6)	6.60 (259.8)
e	0.40 (15.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

Figure 7.1 - QFN64 Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Material	Version	Status
GL3510-OSY52	QFN 64 (4-DFP)	Green Package	52	Available