GL520SM Microprocessor System Hardware Monitor

General Descriptionn

The GL520SM is a low-cost and highly integrated circuit designed in CMOS technology which serves as a hardware monitor of any microprocessor based system. The GL520SM can be used to monitor temperatures, power supply voltages and fan speeds in a PC system. By connecting to an external thermistor for remote sensing applications, the GL520SM allows more flexibility in location of the sensor. The GL520SM will generate interrupts and drive different square-like wave which allows the speaker to sound the alarm when it detects the abnormal situation. Through the SMBus interface, the host can program the temperature trip points and query the GL520SM about the interrupt status, current temperature, voltage and fan speed.

Features

- Remote temperature sensing scheme
- 2 external thermistors for remote sensing
- Wide temperature detection range: 0°C to +110°C
- Programmable hysteresis and temperature set point
- 4 positive voltage monitored
- 2 fan speed monitored
- 5 VID inputs
- 4 types of speaker-driven signal output
- SMBus serial interface
- Readback capability of all monitored temperature, voltage and fan speed
- 24-pin SO plastic package

Key Specifications

• Supply Voltage	5V
• Temperature Accuracy (0°C to +110°C)	±3°C (max)
• Voltage Accuracy (at VIN1, VIN2 and VIN3)	±60mV(max)
(at AVDD)	±75mV(max)

Note: the measuring accuracy is based on neglecting the errors of external thermistors, linearizing and scaling resistors.

Pinning Diagram

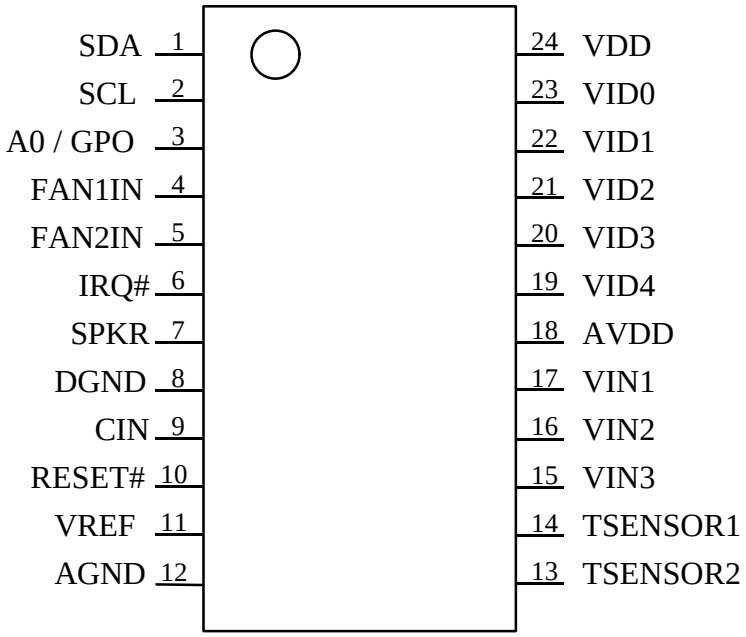


Figure 1. GL520SM pinning diagram

Pin Description

PIN	MNEMONIC	TYPE	FUNCTION
1	SDA	Digital I/O	SMBus data input/output (open drain)
2	SCL	Digital Input	SMBus clock input
3	A0 / GPO	Digital I/O	A general purpose output set/reset by bit 3 of register 0Fh. This pin serves as input for user-set SMBus address A0 during chip reset.
4	FAN1IN	Digital Input	Fan 1 tachometer input with amplitude 0 to VDD.
5	FAN2IN	Digital Input	Fan 2 tachometer input with amplitude 0 to VDD.
6	IRQ#	Digital Output	An active low output to indicate abnormal situation (open drain)
7	SPKR	Digital I/O	Output one of 4 types speaker-driven signal dependent on detected abnormal situation caused by temperature, voltage input and fan speed.
8	DGND	—	Digital Ground.
9	CIN	Analog Input	Connected to an external capacitor.
10	RESET#	Analog Input	An active low input to reset GL520SM.

11	VREF	Analog I/O	Voltage reference for external thermistor
12	AGND	—	Analog ground
13	TSENSOR2	Analog I/O	Connected to an external sensor 2 circuit.
14	TSENSOR1	Analog I/O	Connected to an external sensor 1 circuit.
15	VIN3	Analog Input	Analog voltage input to be monitored.
16	VIN2	Analog Input	Analog voltage input to be monitored.
17	VIN1	Analog Input	Analog voltage input to be monitored.
18	AVDD	—	+5.0V analog power, bypass with a 0.1µF capacitor to AGND. This voltage is also monitored internally.
19	VID4	Digital Input	Voltage supply readouts from the processor. This value is read in the VID Status Register.
20	VID3	Digital Input	Voltage supply readouts from the processor. This value is read in the VID Status Register.
21	VID2	Digital Input	Voltage supply readouts from the processor. This value is read in the VID Status Register.
22	VID1	Digital Input	Voltage supply readouts from the processor. This value is read in the VID Status Register.
23	VID0	Digital Input	Voltage supply readouts from the processor. This value is read in the VID Status Register.
24	VDD	—	+5.0V digital power, bypass with a 0.1µF capacitor to DGND.

Absolute Maximum Ratings

Positive Supply Voltage (VDD)	6.5V
Voltage on Any Input or Output Pin (except analog inputs)	-0.3V to (VDD+0.3V)
Ground Difference (DGND-AGND)	±300mV
Input Current at Any Pin	±5mA
Package Input Current	± 20mA
Maximum Junction Temperature	150°C
ESD Human Body Model	2 kV

Operating Ratings

Operating Temperature Range	-40°C to +125°C
Supply Voltage (VDD)	+4.25V to +5.75V
Ground Difference (DGND-AGND)	±100mV
V_{IN} Voltage Range	-0.05V to (VDD+0.05V)

DC Electrical Characteristics

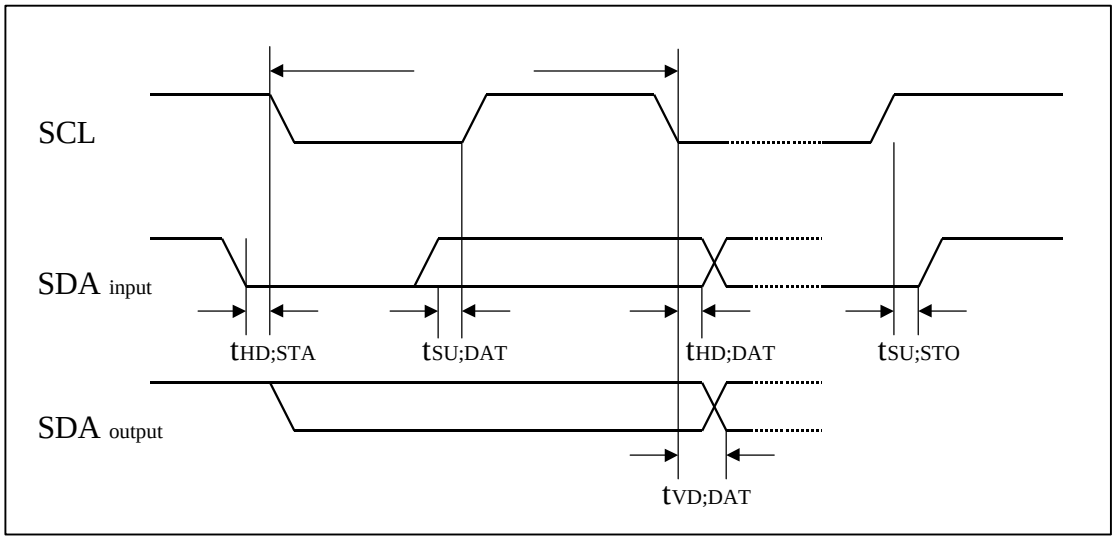
Symbol	Parameter	Conditions	Typical	Limits	Units
Power Supply Characteristics					
Icc	Supply Current		2.4	3.0	mA(max)
Analog-to-Digital Converter Characteristics					
TUE	Total Unadjusted Error			±1	%(max)
t_C	Total Monitoring Cycle Time		1.024		sec
Fan RPM-to-Digital Converter Characteristics (based on 2 pulses per revolution of the fan tachometer output)					
	Full-scale Count			255	(max)
	FAN1 and FAN2 Nominal Input RPM	Divisor =1, Fan Count = 60	8000		RPM
		Divisor = 2, Fan Count = 60	4000		RPM
		Divisor = 4, Fan Count = 60	2000		RPM

		Divisor = 8, Fan Count = 60	1000		RPM
Oscillator Frequency (CIN)					
f_{CIN}		-10°C < TA < +110°C	32		kHz
Digital Outputs (A0/GPO, SPKR)					
$V_{OUT(H)}$	Logical '1' Output Voltage	I_{OUT} = ±5.0 mA		2.4	V(min)
$V_{OUT(L)}$	Logical '0' Output Voltage	I_{OUT} = ±5.0 mA		0.4	V(max)
Open Drain Digital Outputs (SDA, IRQ#)					
$V_{OUT(L)}$	Logical '0' Output Voltage	I_{OUT} = -5.0 mA		0.4	V(min)
$I_{OUT(H)}$	High Level Output Current	V_{OUT} = +5.0V	0.1	100	µA(max)
Digital Inputs (FAN1IN, FAN2IN)					
$V_{IN(H)}$	Logical '1' Input Voltage			2.5	V(min)
$V_{IN(L)}$	Logical '0' Input Voltage			0.8	V(max)
Digital Inputs (VID4-VID0)					
$V_{IN(H)}$	Logical '1' Input Voltage			2.0	V(min)
$V_{IN(L)}$	Logical '0' Input Voltage			0.8	V(max)
Serial Bus Digital Inputs (SCL, SDA) and RESET#					
$V_{IN(H)}$	Logical '1' Input Voltage			2.3	V(min)
$V_{IN(L)}$	Logical '0' Input Voltage			0.6	V(max)

AC Electrical Characteristics

PARAMETER	SYMBOL	MIN.	MAX.	UIITS
SCL clock frequency	$1/f_{SCL}$	10	100	kHz
Data in set-up time	$t_{SU;DAT}$	100	—	ns
Data in hold time	$t_{HD;DAT}$	0	—	ns
SCL low to data out valid	$t_{VD;DAT}$	100	—	ns
Start condition hold time	$t_{HD;STA}$	100	—	ns
Stop condition set-up time	$t_{SU;STO}$	100	—	ns

Figure 2. SMBus Timing Diagram



Functional Description

1. SMBus interface

The GL520SM is a slave device on the SMBus interface with a 7-bit slave address. The six most significant bits of the slave address are “010110”, hard wired inside the chip. The LSB A0 of the address is set by pulling the pin3 high for a one, or pulling down for a zero during power on reset.

2. Analog voltage inputs

The monitored power supplies should be arranged from 0 to 4.0V except AVDD (+5V). In other words, the voltage 0 to 4.0V can be directly connected to the voltage input, whereas the voltage above 4.0V, such as +12V, should be attenuated below 4.0V before connected to the chip. The AVDD (5.0V) of GL520SM is self-monitored after attenuated to 2.0V within the chip. The input voltage drift range is programmable individually. If the input voltage drifts beyond its desired value, GL520SM will send an interrupt request and drive square-like signal to indicate the bad power supply is detected.

While the voltage drift range (the upper and lower limit of VIN1, VIN2, VIN3 and AVDD) is programmed or voltage value register is read, the voltage is determined according to:

$$\text{Voltage Level (in V)} = \text{Register Value} \times \text{ADC Resolution (in V)},$$

where the “ADC Resolution” is 19 mV for VIN1, VIN2 and VIN3, but 23 mV for AVDD.

Note that the “Voltage Level” means the voltage level exactly at the pin VIN1, VIN2 or VIN3. If the power supply to be monitored is over 4.0V as mentioned, the “Voltage Level” will mean the attenuated voltage at input pins. Some examples about accessing the analog associated registers are shown below.

Example 1. How to get the actual voltage from the voltage value register?

If the value form the voltage register is A0h, it means the actual voltage is 3.04V.

Example 2. How to set the voltage limit register when the power supply is greater than 4.0V?

Assume the monitored voltage is 12V and attenuated to 3V before connected to VIN2. The voltage limit will be 2.85V~3.15V if ±5% drift range is presumed. Therefore the

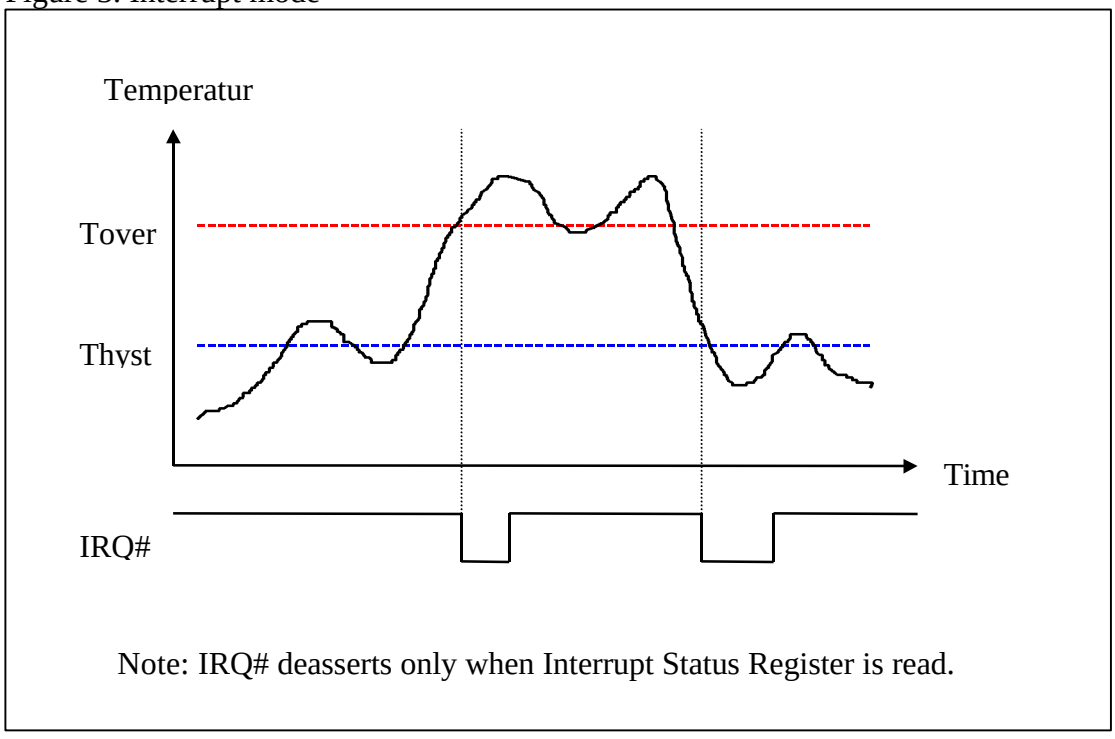
register Vin2_lmtl and Vin2_lmth should be 96h and A5h respectively.

Example 3. How to set the voltage limit register of AVDD(+5V)?
Assume the ±5% drift range of AVDD is set, the voltage limit will be 4.75V~5.25V. Therefore the register AVDD_lmtl and AVDD_lmth should be CEh and E4h respectively.

3. Temperature sensing scheme with an external thermistor
The temperature sensing scheme of GL520SM supports two interrupt modes, "Interrupt" and "Comparator" mode. The default is "Comparator" mode.

(1) "Interrupt" mode:
The temperature over Tover causes an interrupt that will not deassert until reset by reading Interrupt Status Register. Another interrupt will occur if the temperature goes below Thyst. Again it will remain active indefinitely until reset by reading Interrupt Status Register.

Figure 3. Interrupt mode

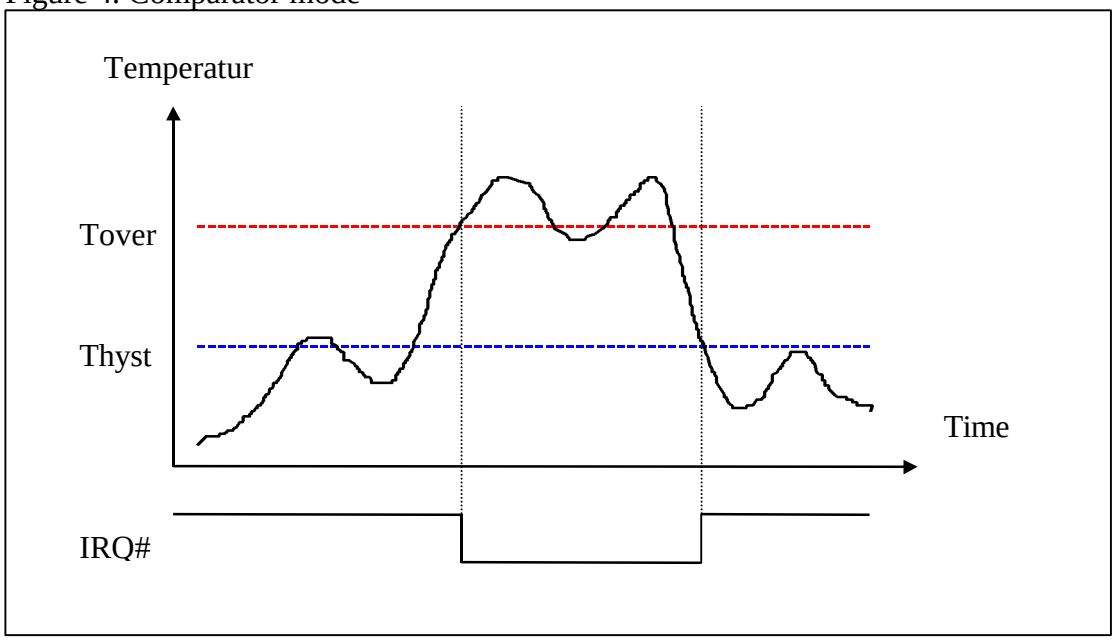


Note: IRQ# deasserts only when Interrupt Status Register is read.

(2) "Comparator" mode:
In this mode, the IRQ# signal behaves like a thermostat which goes low when temperature exceeds the Tover limit, and goes high when the temperature drops below Thyst limit. The interrupt will deassert after the Interrupt Status Register is read,

whereas the next detect will set the interrupt again until the temperature is below Thyst.

Figure 4. Comparator mode



4. Temperature Data Format

The temperature data is represented in an unsigned 8-bit number, which maps the measured temperature in °C by subtracting an offset. The data format applies to all the registers associated with temperature including “Temperature”, “Temp_Over” and “Temp_Hyst”. The actual temperature can be represented in the following equation:

Temperature (°C) = Register Value - Offset,

where the Offset in decimal is 130 for temperature associated registers.

5. General Outputs

The GL520SM provides a general purpose output which is set or reset by programming bit 3 of register 0Fh.

6. Fan Inputs

The Fan Inputs are sampled by an internal 16 KHz clock. The maximum count for one period of the fan input is 255. The default divisor is set to 8 and the default count limit is 64h for both monitored fans. For a fan with 2 pulses per revolution, the default setting provides a lower speed limit of 600 rpm. The fan speed is determined according to:

RPM = 960000 / (Count * Divisor * p),

where p is the pulse number per revolution for the monitored fan.

7. Speaker-driven output SPKR

The pin SPKR sends square-like wave to drive PC speaker in different tone if the abnormal situation of system is detected. There are 4 sounds to differentiate the abnormal situation including user-defined event, power alarm, temperature alarm and cooling fan alarm.

8. Register Access

The data registers in GL520SM are selected by the Pointer register which resets to 00h after power on and stores whatever the last contents it was set to. Writing to the GL520SM will always consist of the SMBus address byte, the Pointer byte and then the data byte.

Reading the GL520SM may take place in two cases:

i. If the Pointer register needs unchanged, the read can simply consist of an address byte, followed by the data byte sent from the GL520SM.
ii. If the Pointer register needs to be set, then the read will proceed by first writing to the GL520SM with the address byte, followed by the Pointer byte. Then a repeated start, followed by the data byte sent form the GL520SM will accomplish the read.

If a two-byte register is to be accessed, the first data byte is always the most significant byte and the second, the least significant byte. Figure 4 and Figure 5 show the data transfer sequence of GL520SM by SMBus interface.

Figure 5. Timing Diagram of SMBus Write for GL520SM

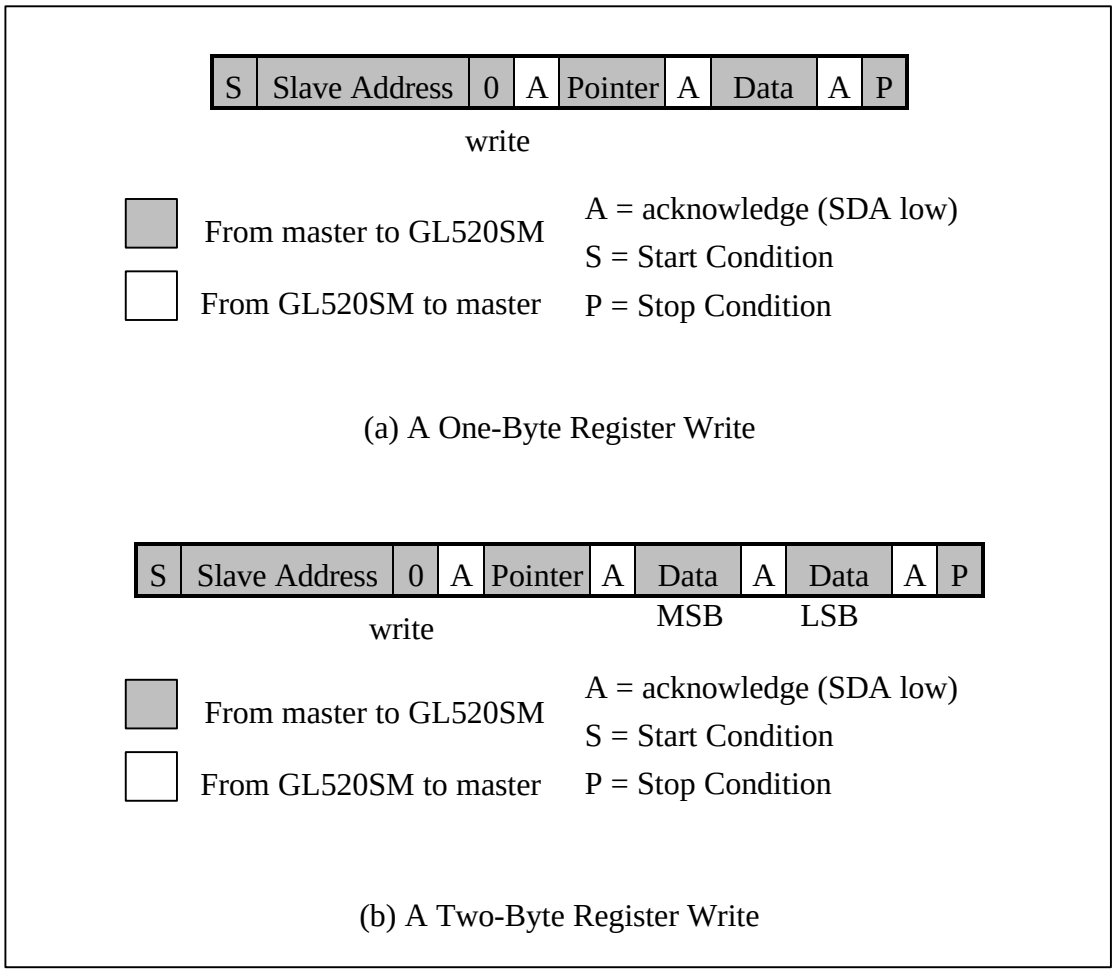
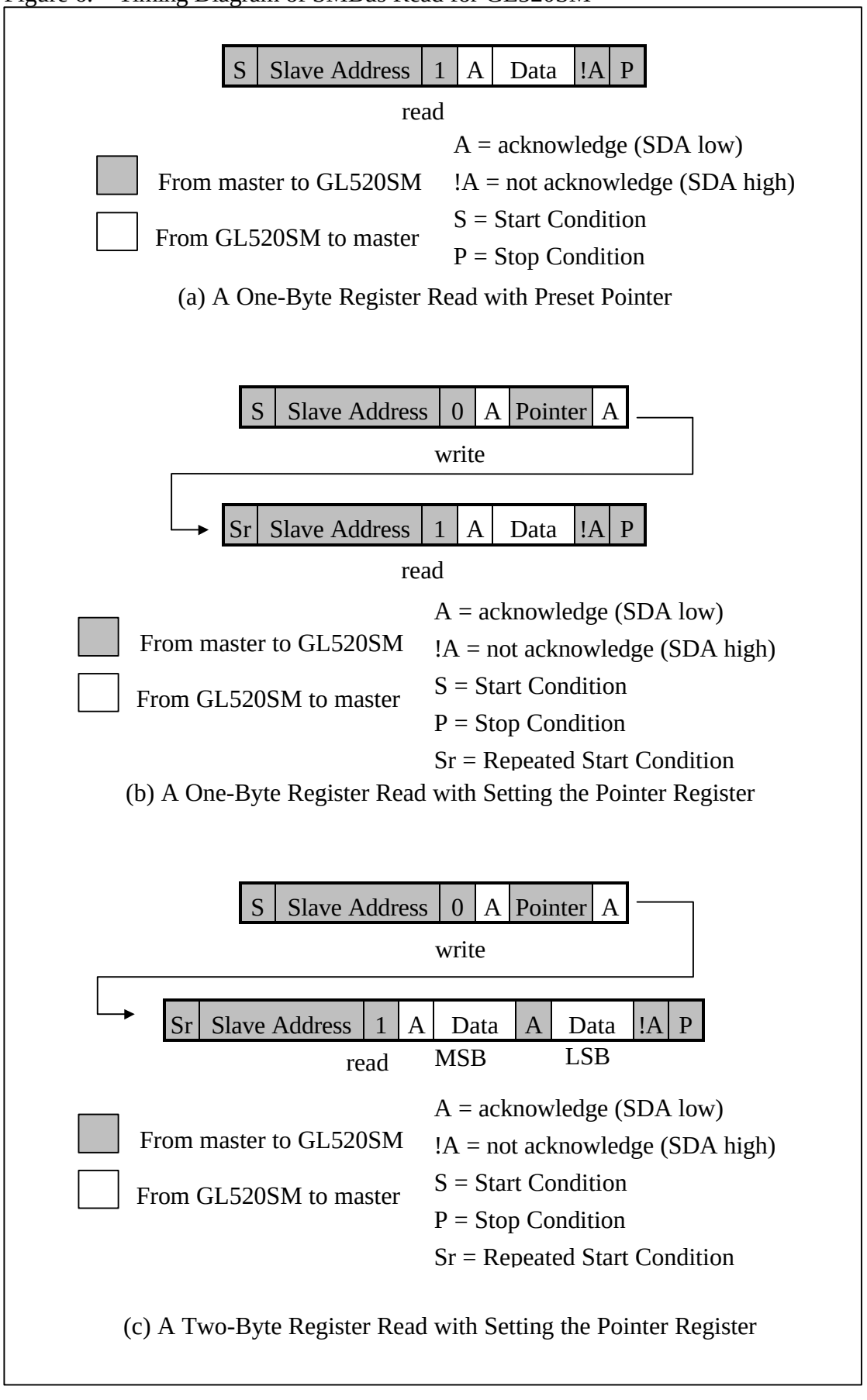


Figure 6. Timing Diagram of SMBus Read for GL520SM



9. NAND Tree Tests

A NAND tree is built in the GL520SM for Automated Test Equipment board level connectivity testing. The NAND tree test mode is entered by pulling down the IRQ# pin while chip reset. In this mode, all pins except VDD, AVDD, GND, AGND, RESET# and SPKR are high impedant which can be forced to 0 or 5V to accomplish NAND tree tests. The toggled output of the NAND tree is monitored on the SPKR pin.

Registers

1. POINTER REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved			Regsel4	Regsel3	Regsel2	Regsel1	Regsel0

D[7:5]: Must be zero while accessed.

D[4:0]: Regsel[4:0] selects which register to be accessed. The pointers 10010b -- 11110b are undefined.

Regsel[4:0]					Register	Byte	Attribute
0	0	0	0	0	ChipID	1	Read Only
0	0	0	0	1	Revision	1	Read Only
0	0	0	1	0	VID	1	Read Only
0	0	0	1	1	Configuration	1	R/W
0	0	1	0	0	Temp1	1	Read Only
0	0	1	0	1	Temp1_Over	1	R/W
0	0	1	1	0	Temp1_Hyst	1	R/W
0	0	1	1	1	Fan1_Count Fan2_Count	2	Read Only
0	1	0	0	0	Fan1_Limit Fan2_Limit	2	R/W
0	1	0	0	1	Vin1_lmth Vin1_lmtl	2	R/W
0	1	0	1	0	Vin2_lmth Vin2_lmtl	2	R/W
0	1	0	1	1	Vin3_lmth Vin3_lmtl	2	R/W
0	1	1	0	0	VDD_lmth VDD_lmtl	2	R/W
0	1	1	0	1	Vin3meter	1	Read Only
0	1	1	1	0	Temp2	1	Read Only
0	1	1	1	1	Misc	1	R/W
1	0	0	0	0	Alarm	1	R/W
1	0	0	0	1	Mask	1	R/W
1	0	0	1	0	Interrupt Status	1	Read Only
1	0	0	1	1	Vin2meter	1	Read Only
1	0	1	0	0	Vin1meter	1	Read Only
1	0	1	0	1	VDDmeter	1	Read Only

1	0	1	1	1	Temp2_Over	1	R/W
1	1	0	0	0	Temp2_Hyst	1	R/W
1	1	1	1	1	Test	1	R/W

Index 00h: CHIPID REGISTER (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
ChipID7	ChipID6	ChipID5	ChipID4	ChipID3	ChipID2	ChipID1	ChipID0

D[7:0]: The identification code, 20h, of GL520SM, read only.

Index 01h: REVISION REGISTER (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
Rev7	Rev6	Rev5	Rev4	Rev3	Rev2	Rev1	Rev0

D[7:0]: The revision of GL520SM, read only.

Index 02h: VID STATUS REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	VID4	VID3	VID2	VID1	VID0

D[7:5]: Rserved.

D[4:0]: VID[4:0], The voltage supply readouts from the processors.

Index 03h: CONFIGURATION REGISTER (default 04h)

D7	D6	D5	D4	D3	D2	D1	D0
Init	Start	Irqen	Mode	Tint	Intclr	Autozero	Notmout

D7: Init, setting a one to this bit restores power on default value to all registers. This bit also clears itself since its default value is zero.

D6: Start, a one enables start of monitoring; a zero puts GL520SM in standby mode immediately. All high and low limits of monitored sources should be set prior to setting this bit high.

D5: Irqen, a one enables the IRQ# output; a zero disables the IRQ# output.

D4: Mode, application mode select: a zero selects mode 1; a one selects mode 2. The GL520SM supports two application modes which are explained in the application note.

D3: Tint, a one selects the temperature interrupt mode; a zero selects the temperature comparator mode.

D2: Intclr, a one clears IRQ# output and remains the contents of Interrupt Status Register unchanged.

D1: Autozero, Setting one/zero enables/disables the auto-zeroing of the internal ADC.

D0: Notmout, Setting one/zero disables/enables the slave timeout function of SMBus

interface.

Note: The GL520SM monitoring function is started by setting Start (Bit6) high and Intclr (Bit2) low.

Index 04h: TEMPERATURE 1 REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
TS1D7	TS1D6	TS1D5	TS1D4	TS1D3	TS1D2	TS1D1	TS1D0

D[7:0]: TS1D[7:0], an unsigned integer mapping current temperature with 1°C resolution. The reported temperature is detected by the external thermistor 1.

Index 05h: Temp1_Over REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
T1over7	T1over6	T1over5	T1over4	T1over3	T1over2	T1over1	T1over0

D[7:0]: T1over[7:0], over-temperature threshold of the temperature detected by the thermistor 1.

Index 06h: Temp1_Hyst REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
T1hyst7	T1hyst6	T1hyst5	T1hyst4	T1hyst3	T1hyst2	T1hyst1	T1hyst0

D[7:0]: T1hyst[7:0], hysterisis threshold of temperature detected by the thermistor 1.

Index 07h: Fan_Count REGISTER (default 0000h)

D15	D14	D13	D12	D11	D10	D9	D8
Fan1cnt7	Fan1cnt6	Fan1cnt5	Fan1cnt4	Fan1cnt3	Fan1cnt2	Fan1cnt1	Fan1cnt0

D7	D6	D5	D4	D3	D2	D1	D0
Fan2cnt7	Fan2cnt6	Fan2cnt5	Fan2cnt4	Fan2cnt3	Fan2cnt2	Fan2cnt1	Fan2cnt0

D[15:8]: Fan1cnt[7:0], an unsigned integer mapping the fan 1 speed. A higher fan speed causes a lower count.

D[7:0]: Fan2cnt[7:0], an unsigned integer mapping the fan 2 speed. A higher fan speed causes a lower count.

Index 08h: Fan_Limit REGISTER (default 0000h)

D15	D14	D13	D12	D11	D10	D9	D8
Fan1lmt7	Fan1lmt6	Fan1lmt5	Fan1lmt4	Fan1lmt3	Fan1lmt2	Fan1lmt1	Fan1lmt0

D7	D6	D5	D4	D3	D2	D1	D0

Fan2lmt7	Fan2lmt6	Fan2lmt5	Fan2lmt4	Fan2lmt3	Fan2lmt2	Fan2lmt1	Fan2lmt0

D[15:8]: The lower speed limit to indicate a fan 1 failure.

D[7:0]: The lower speed limit to indicate a fan 2 failure.

Index 09h: Vin1_Limit REGISTER (default 0000h)

D15	D14	D13	D12	D11	D10	D9	D8
Vin1H7	Vin1H6	Vin1H5	Vin1H4	Vin1H3	Vin1H2	Vin1H1	Vin1H0

D7	D6	D5	D4	D3	D2	D1	D0
Vin1L7	Vin1L6	Vin1L5	Vin1L4	Vin1L3	Vin1L2	Vin1L1	Vin1L0

D[15:8]: The high limit of voltage from VIN1.

D[7:0]: The low limit of voltage from VIN1.

Index 0Ah: Vin2_Limit REGISTER (default 0000h)

D15	D14	D13	D12	D11	D10	D9	D8
Vin2H7	Vin2H6	Vin2H5	Vin2H4	Vin2H3	Vin2H2	Vin2H1	Vin2H0

D7	D6	D5	D4	D3	D2	D1	D0
Vin2L7	Vin2L6	Vin2L5	Vin2L4	Vin2L3	Vin2L2	Vin2L1	Vin2L0

D[15:8]: The high limit of voltage from VIN2.

D[7:0]: The low limit of voltage from VIN2.

Index 0Bh: Vin3_Limit REGISTER (default 0000h)

D15	D14	D13	D12	D11	D10	D9	D8
Vin3H7	Vin3H6	Vin3H5	Vin3H4	Vin3H3	Vin3H2	Vin3H1	Vin3H0

D7	D6	D5	D4	D3	D2	D1	D0
Vin3L7	Vin3L6	Vin3L5	Vin3L4	Vin3L3	Vin3L2	Vin3L1	Vin3L0

D[15:8]: The high limit of voltage from VIN3.

D[7:0]: The low limit of voltage from VIN3.

Index 0Ch: AVDD_Limit REGISTER (default 0000h)

D15	D14	D13	D12	D11	D10	D9	D8
AVDDH7	AVDDH6	AVDDH5	AVDDH4	AVDDH3	AVDDH2	AVDDH1	AVDDH0

D7	D6	D5	D4	D3	D2	D1	D0

AVDDL7	AVDDL6	AVDDL5	AVDDL4	AVDDL3	AVDDL2	AVDDL1	AVDDL0

D[15:8]: The high limit of voltage from AVDD.

D[7:0]: The low limit of voltage from AVDD.

Index 0Dh: VIN3 VOLTAGE REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
VIN3D7	VIN3D6	VIN3D5	VIN3D4	VIN3D3	VIN3D2	VIN3D1	VIN3D0

D[7:0]: VIN3D[7:0], a positive value of voltage at pin VIN3 with resolution 19 mV.

Index 0Eh: TEMPERATURE 2 REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
TS2D7	TS2D6	TS2D5	TS2D4	TS2D3	TS2D2	TS2D1	TS2D0

D[7:0]: TS2D[7:0], an unsigned integer mapping current temperature with 1°C resolution. The reported temperature is detected by the external thermistor 2.

Index 0Fh: MISC. REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
Fan1Div1	Fan1Div0	Fan2Div1	Fan2Div0	Reserved	SetGPO	Ualarm	VIDth

D[7:6]: Fan1Div[1:0], fan 1 divisor select.

D[5:4]: Fan2Div[1:0], fan 2 divisor select. The select table of fan1 and fan2 are both the same and shown below:

FanDiv1	FanDiv0	Divisor
0	0	1
0	1	2
1	0	4
1	1	8

D3: Reserved.

D2: SetGPO, a one forces pin A0/GPO to high; a zero resets the pin to low.

D1: Ualarm, a one enables SPKR to alarm by a user-defined event.

D0: VIDth, the option of VID input voltage threshold. A zero selects 1.4V; a one selects 0.75V.

Index 10h: ALARM REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
Temp2SPK	Fan2SPK	Fan1SPK	Temp1SPK	Vin3SPK	Vin2SPK	Vin1SPK	AVDDSPK

D7: Temp2SPK, a one enables SPKR output by temperature sensor 2 monitoring.

D6: Fan2SPK, a one enables SPKR output by Fan2 monitoring.

D5: Fan1SPK, a one enables SPKR output by Fan1 monitoring.

D4: Temp1SPK, a one enables SPKR output by temperature sensor 1 monitoring.

D3: Vin3SPK, a one enables SPKR output by voltage VIN3 monitoring.

D2: Vin2SPK, a one enables SPKR output by voltage VIN2 monitoring.

D1: Vin1SPK , a one enables SPKR output by voltage VIN1 monitoring.

D0: AVDDSPK, a one enables SPKR output by voltage AVDD monitoring.

Index 11h: MASK REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
Temp2EN	Fan2EN	Fan1EN	Temp1EN	Vin3EN	Vin2EN	Vin1EN	AVDDEN

D7: Temp2EN, a one enables interrupt output by temperature sensor 2 monitoring.

D6: Fan2EN, a one enables interrupt output by fan 2 monitoring.

D5: Fan1EN, a one enables interrupt output by fan 1 monitoring.

D4: Temp1EN, a one enables interrupt output by temperature sensor1 monitoring.

D3: Vin3EN, a one enables interrupt output by VIN3 monitoring.

D2: Vin2EN, a one enables interrupt output by VIN2 monitoring.

D1: Vin2EN, a one enables interrupt output by VIN1 monitoring.

D0: AVDDEN, a one enables interrupt output by AVDD monitoring.

Index 12h: INTERRUPT STATUS REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
Temp2ST	Fan2ST	Fan1ST	Temp1ST	Vin3ST	Vin2ST	Vin1ST	AVDDST

D7: Temp2ST, a one indicates the temperature detected by sensor 2 is above T2over or below T2hyst.

D6: Fan2ST, a one indicates the speed of fan 2 has exceeded its lower limit.

D5: Fan1ST, a one indicates the speed of fan 1 has exceeded its lower limit.

D4: Temp1ST, a one indicates the temperature detected by sensor 1 is above T1over or below T1hyst.

D3: Vin3ST, a one indicates the voltage from VIN3 has exceeded its error limit.

D2: Vin2ST, a one indicates the voltage from VIN2 has exceeded its error limit.

D1: Vin1ST, a one indicates the voltage from VIN1 has exceeded its error limit.

D0: AVDDST, a one indicates the voltage from AVDD has exceeded its error limit.

Index 13h: VIN2 VOLTAGE REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
VIN2D7	VIN2D6	VIN2D5	VIN2D4	VIN2D3	VIN2D2	VIN2D1	VIN2D0

D[7:0]: VIN2D[7:0], a positive value of voltage at pin VIN2 with resolution 19 mV.

Index 14h: VIN1 VOLTAGE REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
VIN1D7	VIN1D6	VIN1D5	VIN1D4	VIN1D3	VIN1D2	VIN1D1	VIN1D0

D[7:0]: VIN1D[7:0], a positive value of voltage at pin VIN1 with resolution 19 mV.

Index 15h: VIN0 VOLTAGE REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
VIN0D7	VIN0D6	VIN0D5	VIN0D4	VIN0D3	VIN0D2	VIN0D1	VIN0D0

D[7:0]: VIN0D[7:0], a positive value of voltage at pin AVDD with resolution 23 mV.

Index 17h: Temp2_Over REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
T2over7	T2over6	T2over5	T2over4	T2over3	T2over2	T2over1	T2over0

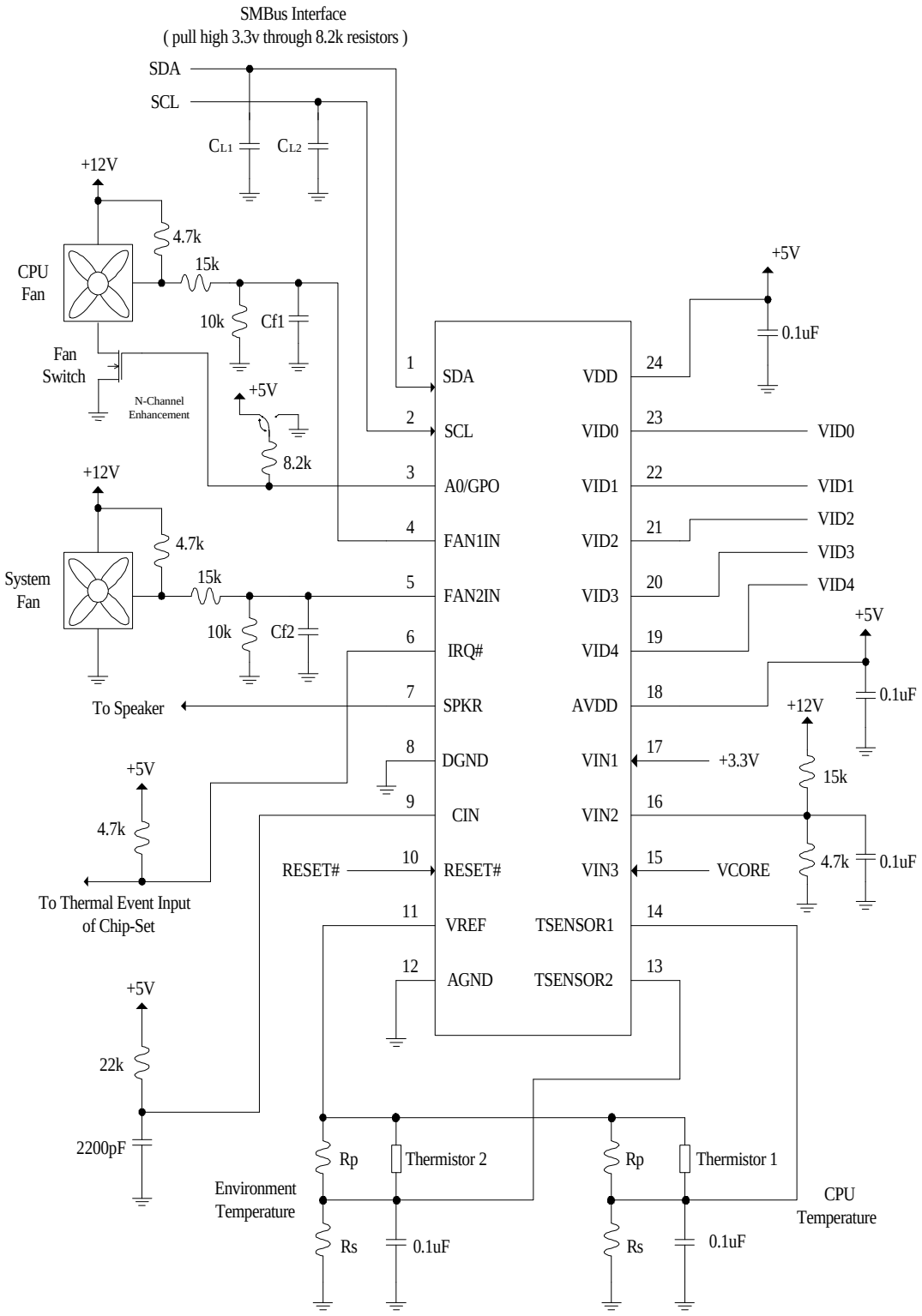
D[7:0]: T2over[7:0], over-temperature threshold of the temperature sensed by the external thermistor.

Index 18h: Temp2_Hyst REGISTER (default 00h)

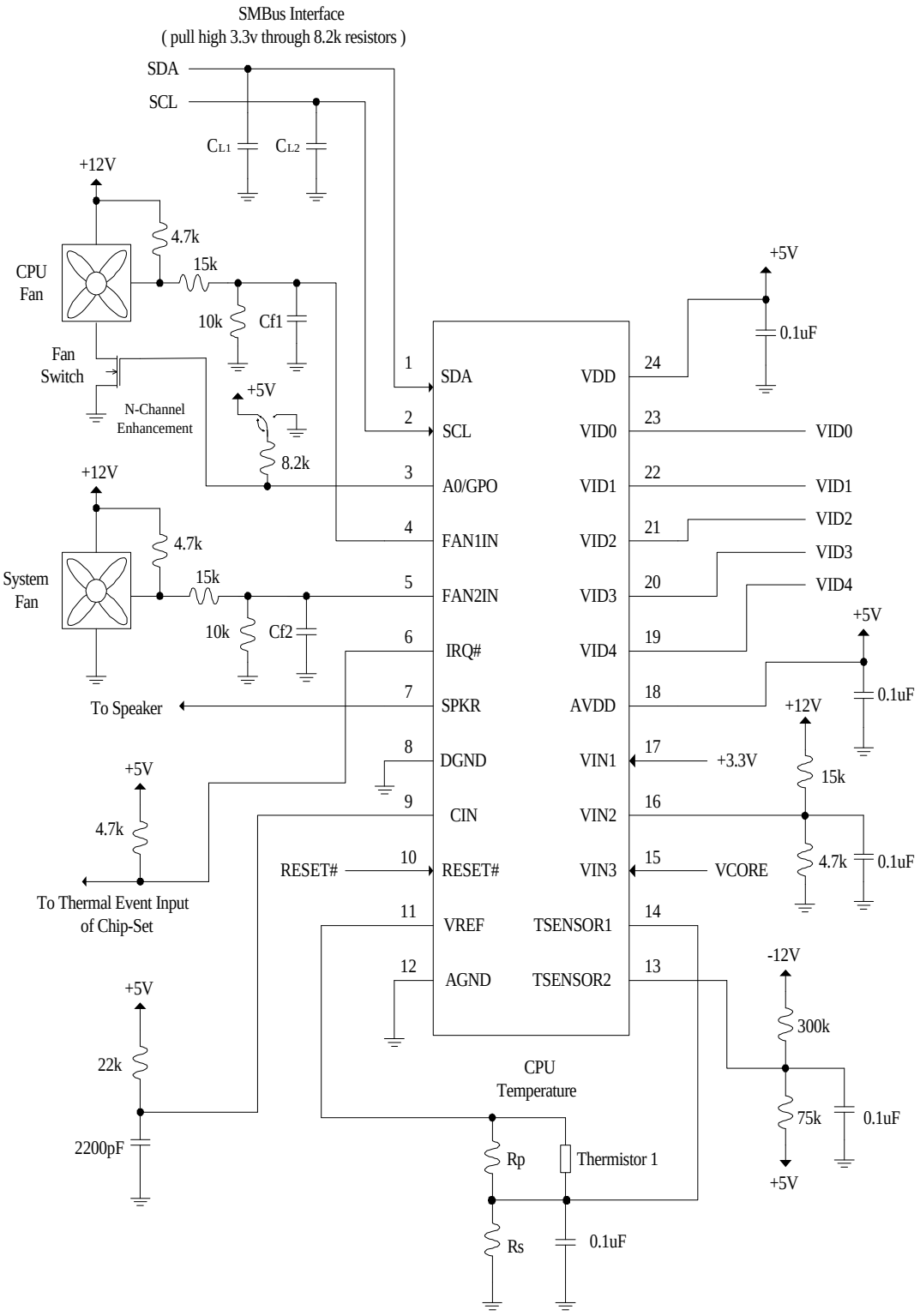
D7	D6	D5	D4	D3	D2	D1	D0
T2hyst7	T2hyst6	T2hyst5	T2hyst4	T2hyst3	T2hyst2	T2hyst1	T2hyst0

D[7:0]: T2hyst[7:0], hysterisis threshold of temperature sensed by the external thermistor.

TYPICAL APPLICATION OF MODE I



TYPICAL APPLICATION OF MODE II



Application Note

1. Application Mode:

   GL520SM is allowed to be configured into two application modes as shown in the above application circuits. The default application is mode 1.

   Mode 1: The chip monitors 2 temperature, 2 fans and 4 positive power supplies.

   Mode 2: The chip monitors 1 temperature, 2 fans, 4 positive power supplies and 1 negative power supply. For the –12V input, the scaling resistors should be ratioed such that a positive voltage below +2.4V appears at the pin TSENSOR2.

   The mode is selected by bit 4 of configuration register.

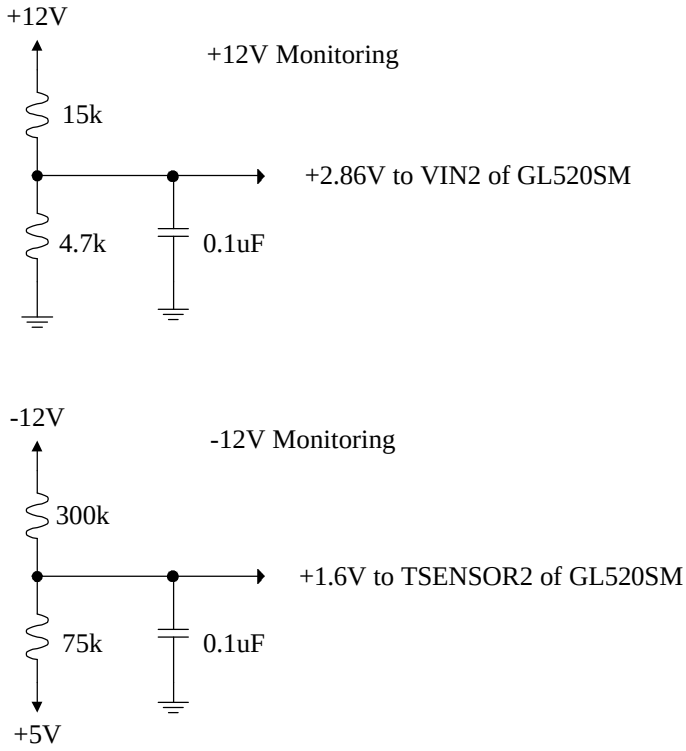
2. Thermistors:

   The recommended thermistor models and corresponding linearizing resistors are listed below. The values of resistors are computed on neglecting the ingenerate errors of resistors and thermistor. For an optimized temperature precision, the resistors, Rp and Rs, are recommended to offer within ±1% tolerance. The values of linearizing resistors need changed for other thermistor models not shown in the table.

Thermistor Model	Rp	Rs
FENWAL 135-103 LAG-J01	4.3k	4.7k
FENWAL 135-103 LAF-J01	4.3k	4.7k
SEMITEC 103 CT-4	8.2k	6.8k
SEMITEC 103 AT	6.8k	6.2k
YMEX 186-103 YMD-J	4.3k	4.7k
YMEX 186-103 YMD-JW	5.6k	5.6k
YMEX 186-103 YMC-H	6.8k	6.2k
YMEX 286-S103 CIG-H	5.6k	5.6k
YMEX 186-103 YMS-J	5.6k	5.6k

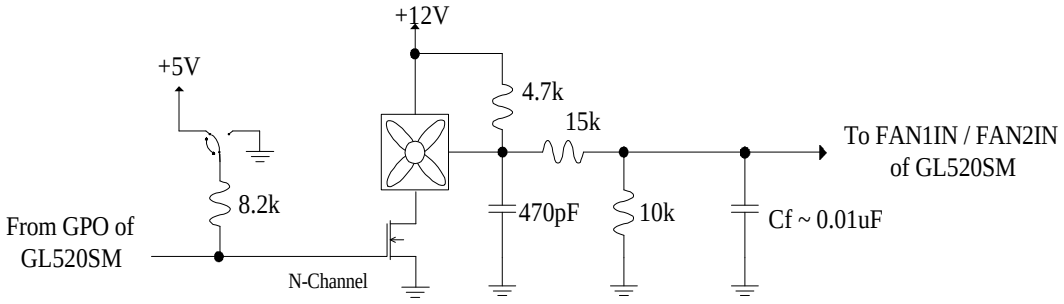
3. Voltage Scaling:

   The power supply to be monitored should be ranged from 0 to 4.0V. In other words, the voltage 0 to 4.0V can be directly connected to voltage input of GL520SM, whereas the voltage above 4.0V, such as 12V, should be attenuated below 4.0V before connected to this chip. The scaling resistor values for +12V and -12V input are recommended as below,



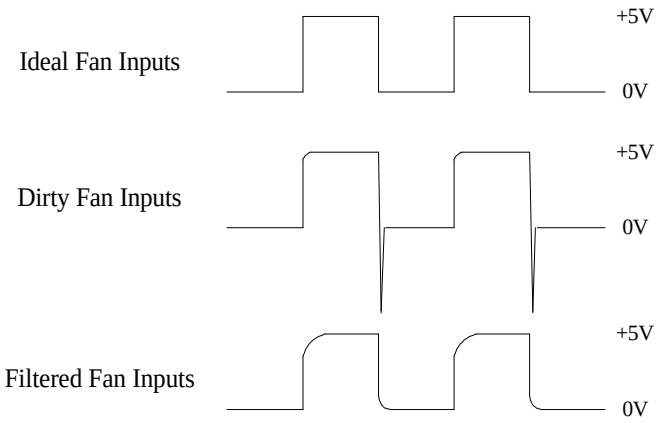
4. Fan Inputs and Fan ON/OFF Control:

   The fan inputs should be connected as illustrated below,



- If the fan inputs are directly pulled high to +5V through resistors in the above diagram, a +12V dc level voltage will appear at the fan inputs when the fans are turned off. This signal level may lead to damage to the chips.
- The LSB of GL520SM SMBus address is determined by pulling the 8.2k resistor high or low while power on reset. The slave address is 5Ah if this pin is pulled high, and 58h if low.
- The unused fan inputs should be terminated to ground using 10k resistors.
- The capacitor Cf are used to filter the undershoot of fan inputs if needed. The values depend on the undershoot and input threshold at pin FAN1IN/FAN2IN. Be sure the inputs meet the operating ratings, -0.3V ~

VDD+0.3V.



5. Chip Clock:
   The R and C external to pin CIN is adjustable while the internal circuit is oscillated at 32KHz ideally. Since the detected fan inputs are sampled by the chip clock, the error of clock rate will respond the error of computed fan speed.

6. Interrupt Output:
   The IRQ# can be programmed to generate only when the detected CPU temperature exceeds the over temperature limit. In temperature comparator mode, the GL520SM will automatically assert/deassert the IRQ# output depending on the detected temperature. By connecting the IRQ# to the Thermal Detect Input of chip-sets, the GL520SM can be used to start the Hardware Clock Throttle mode. The IRQ# pin of GL520SM is open-drain and should be pulled high externally to operate properly.

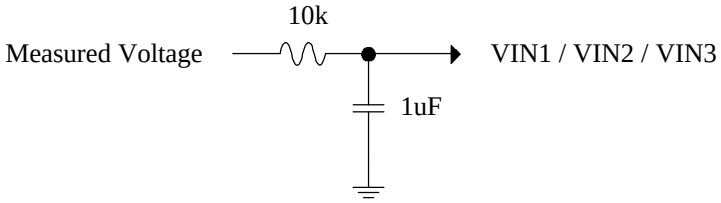
7. SMBus Loading:
   The bus loading should be considered since there are usually more than one SMBus-agent component in the system.
   - The components should be placed closely to each other on the board to minimize the bus loading effect.
   - The values of pull-high resistors are adjusted to meet the rise and fall time condition.
   - The small capacitors are added if the bus loading of these two siganl is severely unbalanced.

8. Bypass Capacitors:
   Bypass capacitors are needed at the pin VDD and AVDD and should be placed

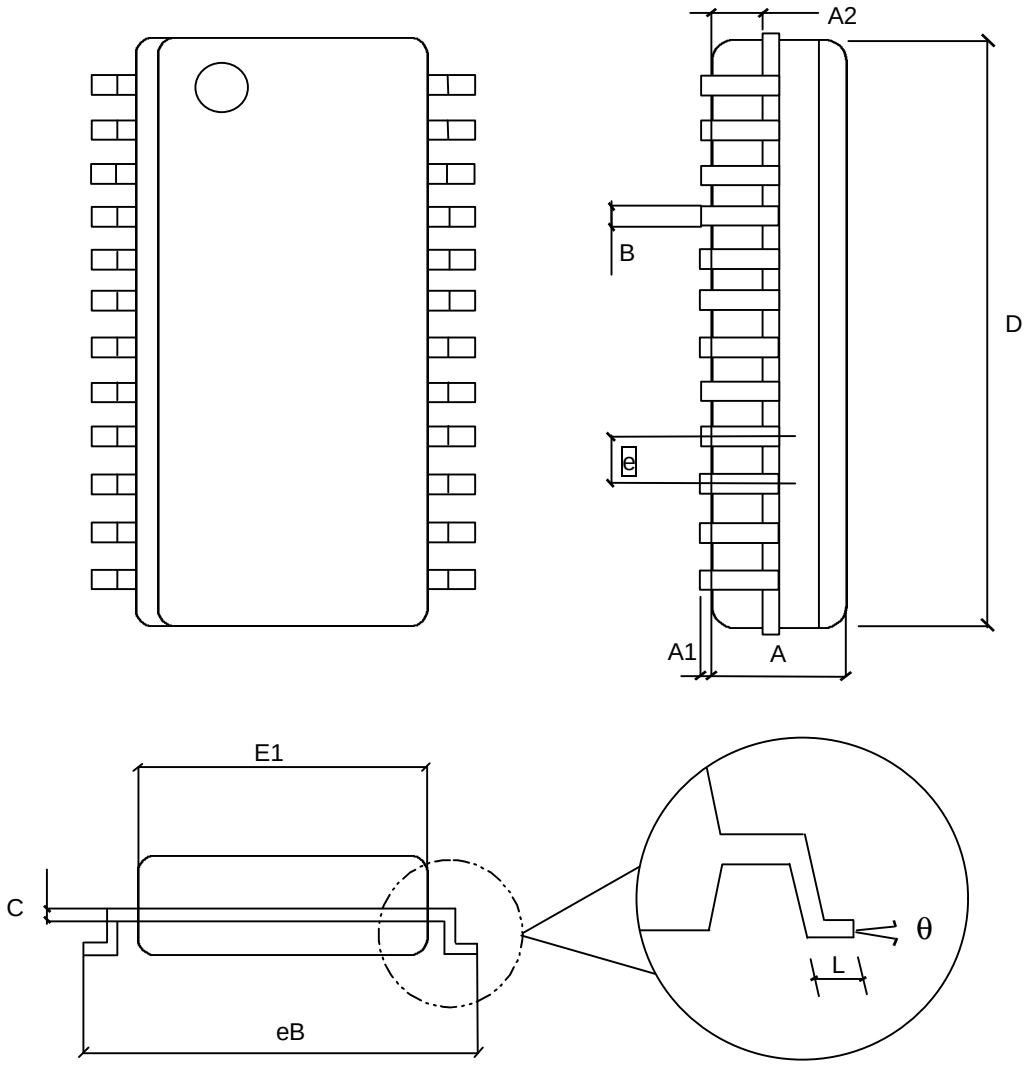
near the chip as closely as possible.

9. Anti-aliasing Filters:

An anti-aliasing filter is recommended to insert at pin VIN1, VIN2 and VIN3 for a noisy environment. The referenced circuit is as below where the values of R and C are selected so that $R \times C > 5 \times 10^{-4}$.



The Package Outline Dimension of GL520SM (SOP 24 Pins)



Symbol	Dimension in mils			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	98	100	102	2.489	2.540	2.591
A1	6	---	---	0.152	---	---
A2	39	41	43	0.991	1.041	1.092
B	---	16	---	---	0.406	---
C	---	10	---	---	0.254	---
D	598	600	602	15.189	15.240	15.291
E1	298	300	302	7.569	7.620	7.671
e	---	50	---	---	1.270	---
eB	406	410	414	10.312	10.414	10.516
L	30	32	34	0.762	0.813	0.864
θ	---	5°	---	---	5°	---