Navigation Receiver Module
GL8088s

Operations Manual

Version 1.1

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Summary

This document is designed for users of multi-channel navigation GLONASS/GPS/GALILEO receiving module GL8088s and contains the general description, specifications, application instructions, and rules of operation, transportation, and storage.

List of Used Abbreviations

The list of adopted abbreviations is set out below:

SS: Space Satellite
SC: Satellite Constellation
NT: Navigation Task
PC: Personal Computer
SW: Software
CT: Standard Accuracy = **ПТ-Code**: Reduced Accuracy (former designation)
NMEA: Full name **NMEA 0183**, text protocol used for marine (normally navigation) equipment intercommunications (**National Marine Electronics Association)**.

General Information

The exterior view of GL8088s navigation receiver module is shown in figure 1.

Fig. 1. The exterior view of the receiver module.

GL8088s receiving device of GLONASS/GPS/GALILEO multy-constellation Navigation System (hereinafter referred to as receiver or module) is designed for real-time calculation of current geographic coordinates and velocity of the target, generation of a time sinchronisation pulse called 1PPS and exchange with peripherals via RS232 serial ports. The operating principle of the receiver is based on parallel receiving and processing of signals from navigation GLONASS SC by 32 counting channels in frequency band L1 (CT or PT code), GPS on L1 frequency (C/A code) and GALILEO on E1 frequency. NT solution results are issued in NMEA messages format.

GL8088s navigation receiver is built on a state-of-the-art dedicated chipset STA8088F from the family of so-called "systems-on-a-chip" STA8088FG.

The receiver has high sensitivity, low power consumption and short cold/warm/hot start times.

The receiver is provided with two searching (capturing) channels and 32 channels for satellite signals tracking, which ensures simultaneous searching for satellite signals of GLONASS and GPS constellations.

The receiver makes it possible to use stellites almanac and ephemeris data stored in the receiver memory for initial search of satellite signals; this ensures reduction of cold start time and, which is more important, makes it possible to perform the cold start when the signals from satellites are weak. The mentioned datas can be prepared by external sources (and transferred to the receiver via data links), as well as by the receiver itself. In the latter case, no additional information from the external sources is required.

The right-orientation key (the mark of the first connection terminal) is a black dot against the white background; the key is located in the top left corner of the label beside NAVIA logo.

Fig. 2. View of the receiver board with the screen removed.

The receiver is provided with built-in 3-state jammer barrier feature, which allow the receiver to operate under high interference signaling environment.

The receiver operation control interface is performed with the use of special ST GNSS NMEA commands.

The Demo board is released for user evaluation of the receiver module operation. The description of the board is provided in document Demo board GL8088s TD v1_0.pdf. The board can be connected to PC or other equipment for the receiver module operation analysis.

Specifications

Parameter		Value
Number of tracking channels		32
Number of capturing channels		2
GPS frequency band, MHz		1,575.42 ±0.5
GLONASS frequency band, MHz		1,597.5…1,605.9
Coordinates calculation tolerance (at confidence probability level 0.67), maximum, m		2 in plan 4 by height
Plan velocity calculation tolerance (at confidence probability level 0.67), maximum, m/s		0.05
Tolerance of 1PPS distribution (at the gauss 70% distribution level) to time scales GPS, GLONASS, UTC, UTC (SU), average, ns		+-17
Mean time to the first position measurement, at signal level – 130 dBm, s		35 cold start 34 warm start 1 hot start 1 recapturing
Detection sensitivity, minimum, dBm		-145 cold start -145 warm start -155 hot start
Satellite ephemeris predicting,days		5 – stand alone 7 – external data source
Volume of statellites almanac and ephemeris data transmitted from the external source, KBytes		2
Tracking sensitivity, minimum, dBm		-162 in statics -159 in dynamics -155 in dynamics (tolerance 30 m maximum)
Jammer barrier system		3 level, built-in
Output data updating rate, Hz		0.1…1, 5
Dynamics, Maximum	Acceleration, g rate of acceleration change, g/s	3 1
Maximum velocity, m/s		515
Maximum height, m		18,000
Microprocessor core		ARM946
Communications interface		RS232 3.3 V LVTTL
1PPS signal	Level duration, ms	3.3 V LVTTL 500
Main supply voltage, V		3.0…3.6
Backup supply voltage, V		2.0…3.6
Useful current in 3.3 V circuit, standard, mA		searching 55 (GPS), 75 (GLONASS+GPS) tracking 35 (GPS), 55 (GLONASS+GPS)
Useful current in external backup battery circuit, standard, µA		50
Dimensions (length x width x height), mm³		35.5x33.2x3.8
Weight, maximum, g		10
Operating temperatures range, ºC		-40…+85

Receiver module Overall Dimensions

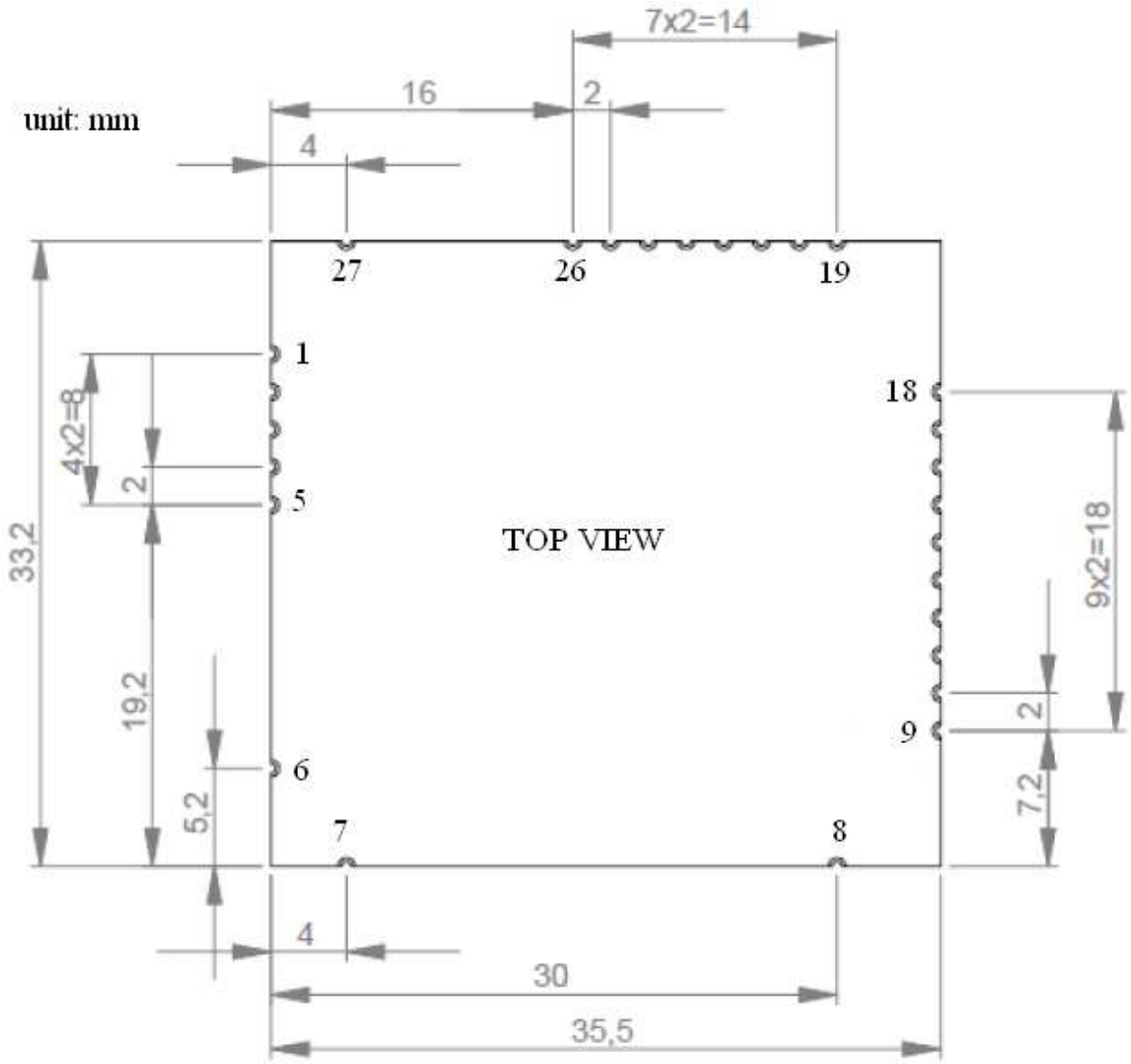

Fig. 3. Overall and Connection Dimensions of GL8088s Receiver.

Recommended Footprint for the Receiver module

The recommended footprint for GL8088s mounting on the user's PCB is shown in figure 4. All dimensions are in millimeters.

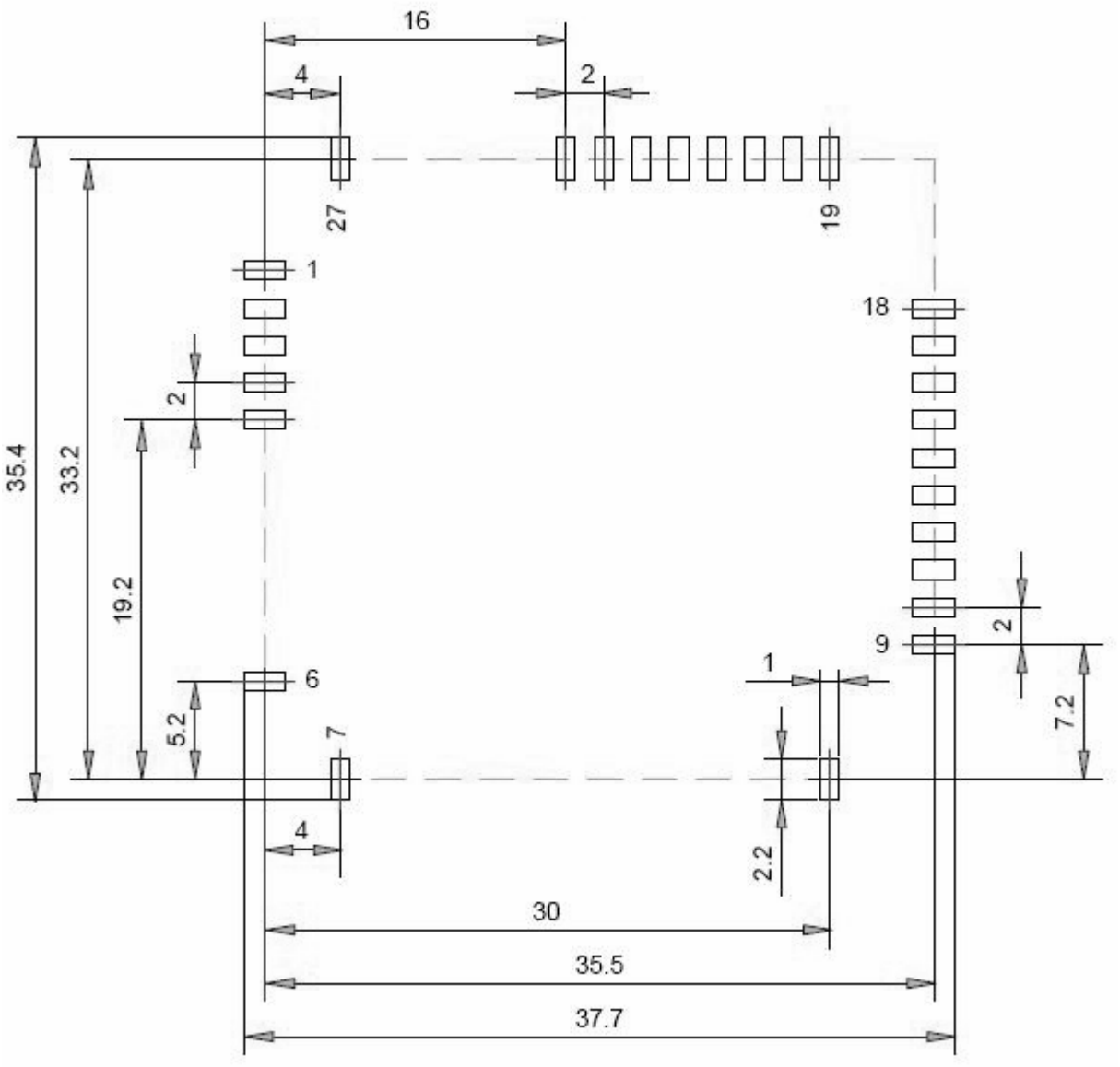

Fig. 4. Recommended mounting seat for GL8088s receiver.

No signal lines should be placed under the module. It is recommended that the free space under the module be filled with GND polygon.

Function of Connection Terminals

Signal description	Type	Terminal number	Designation
Ground of the high-frequency part	Power	1, 2, 4, 5, 6, 7, 27	AGND
Ground of the digital part	Power	8, 9, 18, 20, 22	GND
Antenna input	Analog	3	RFIN
Power supply +3.3 V	Power	10, 21	PWRIN
Backup battery circuit power supply	Power	17	VBAT
UART0 Output	In/**Out**	13	TXD0
UART0 Input	**In**/Out	12	RXD0
UART1 Output	In/**Out**	15	TXD1
UART1 Input	**In**/Out	14	RXD1
1PPS signal	In/**Ou**t	16	PPS1
Module On/Off Switching	In	11	ENA
Module hardware reset	In	19	$\overline{\text{RST}}$
Not connected	---	23, 24, 25, 26	NC

The states of bidirectional connection terminals in working mode of the receiver operation are shown in bold letters.

Typical Application Schematic

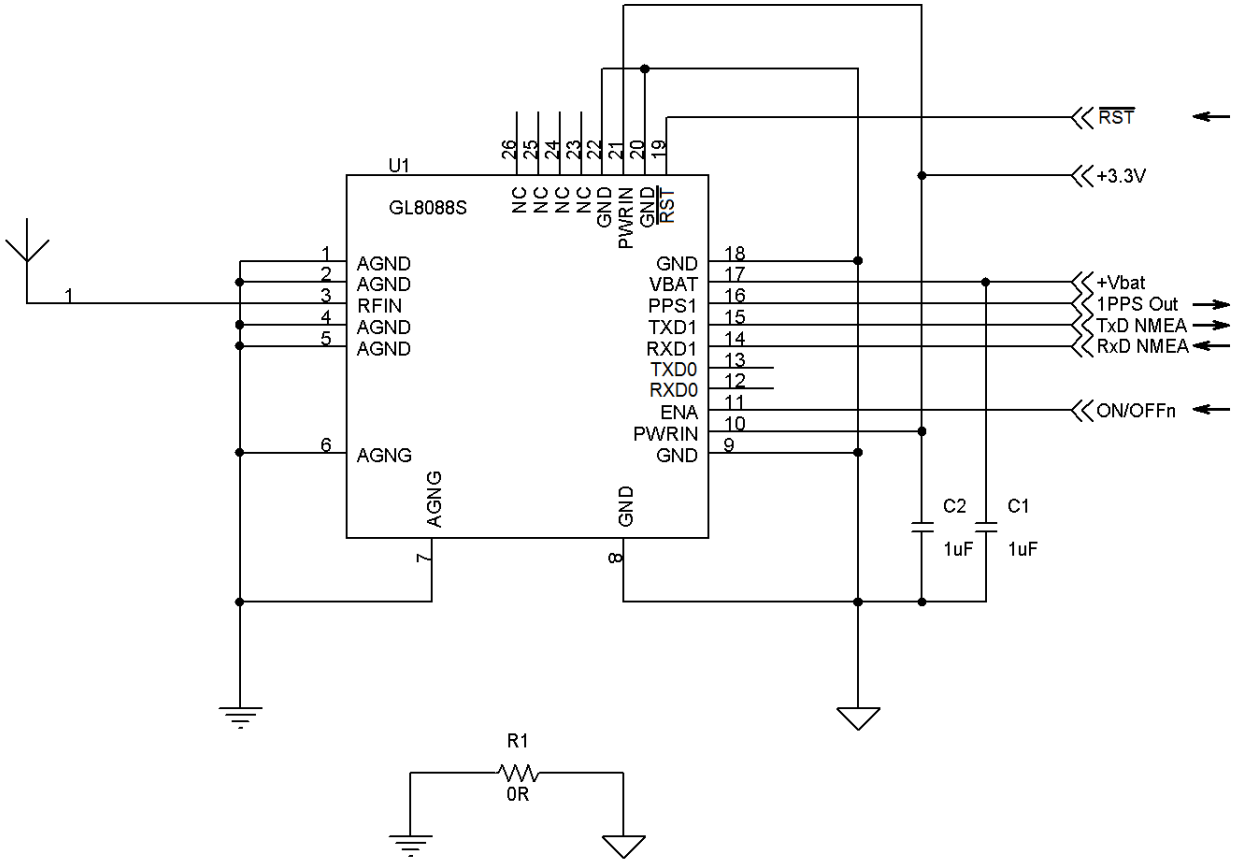

Fig. 5. GL8088s receiver standard connecting diagram.

Figure 5 shows the standard application circuit diagram of GL8088s receiver. The arrows designate the directions of signals propagation – input signals of the receiver are designated with arrows "to the receiver", output signals are designated with arrows "from the receiver".

The receiver supply voltage V_{dd} = 3.0…3.6 V is applied to termination pads 10 and/or 21 (PWRIN) integrated inside the module. In the connecting diagram, this circuit is designated as +3.3V.

Voltage from the backup battery within the range of V_{bat} = 2.0…3.6 V must be applied to termination pad 17 (VBAT). In the application circuit diagram, this circuit is designated as $+V_{bat}$. It is recommended that V_{bat} be constantly maintained for assurance of built-in RTC clock and module RAM memory. In addition, the backup battery voltage provides power for the module internal firmware (the module FW) activation attribute lautch storage register. Use of a backup battery whose voltage exceeds the module supply voltage is not recommended ($V_{bat} \leq V_{dd}$).

AT ONLY A FIRST TIME of the module supply voltage V_{dd} is "ON" following V_{bat} also "ON", be sure to send a low logic level pulse to terminal pad 19 ($\overline{RST}$ input). This is required for selection of operation mode for the integrated microcontroller of the module (operation or storing of the program in the built-in flash SQI memory), for activation of the module internal FW and saving of its activation attribute into the storage lautch register. The pulse duration must be at least 10 ms, the input voltage must not exceed 0.1 V, the source output capability must be at least 8 mA. At subsequent switching-on of V_{dd} supply voltage, sending of the pulse to $\overline{RST}$ input is non-mandatory, since sending of this signal causes eraising of current time information in RTC, which increases the time of satellites searching and capturing. The signal states and levels timing diagram at the module connection terminals at V_{bat} and V_{dd} switching-on is shown in figure 6.

It should be taken into account that the states and signals are described in reference to the external peripheral control system (e.g., external peripheral MCU). Therefore, the data at TxD0 output of the module is described in the figure as "Input data" (input data for the external peripheral system), while the data at RxD0 input of the module is described as "Output data" (output data from the peripheral system). High impedance Z state describes the connection terminals of the peripheral system (inputs and outputs) connected to the relevant connection terminals of the module.

The connection terminals of the peripheral control system must in no time be the power sources of the module (the so-called phantom power), i.e., voltages at connection terminals TxD0, RxD0, TxD1 and RxD1 must not exceed the module supply voltage at any time. Clearly, with V_{dd} switched-off, there must be no voltage on the said connection terminals; for example, if the connection terminals are switched to high-impedance Z state, input mode or into Logical 0 state, there must be no supply voltage "pull-up" on them.

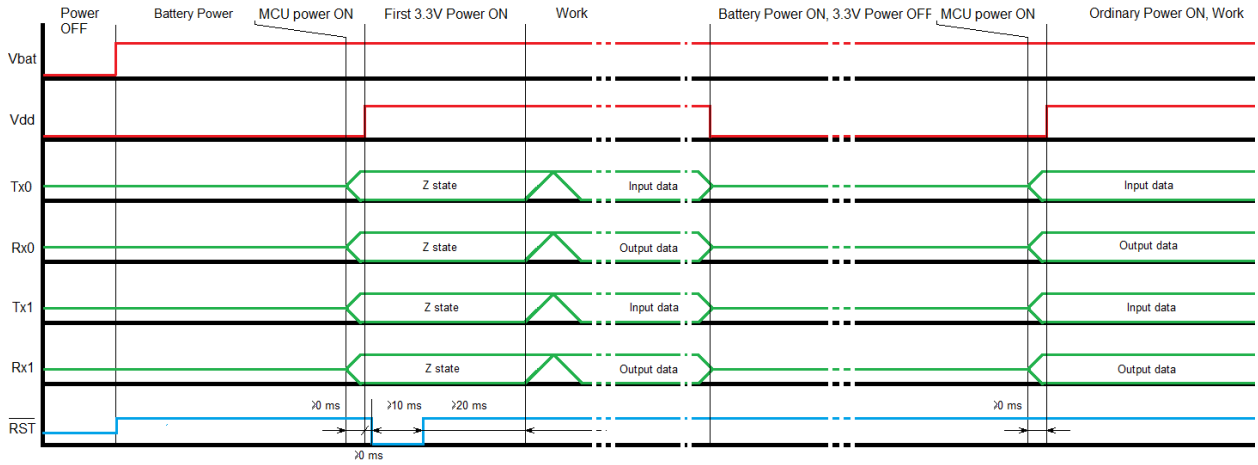

Fig. 6. The signal states and levels timing diagram at the module connection terminals at Vbat application.

The moment the pulse is sent to $\overline{RST}$ input (or, if this pulse is not generated but instead only the module supply voltage V_{dd} is applied without applying of $+V_{bat}$), be sure to provide for high-impedance state (Z state or Input state) of the circuits connected to TXD0 and TXD1 terminals. In doing so, be aware that there should be no leakages through protection circuits of connected connection terminals caused by overvoltage up to V_{dd} value. Failure to meet this requirement will render correct launching of the module internal software impossible. The said states should be maintained for at least 20 ms from the moment the sending of low level signal to $\overline{RST}$ input is over or from the moment V_{dd} supply voltage is switched on (if V_{bat} is not used).

If the backup battery is not used, sending of the pulse to $\overline{RST}$ input is non-mandatory. The signal states and levels timing diagram at the module connection terminals at V_{dd} switching-on without V_{bat} being used is shown in figure 7.

The pulse can be sent to $\overline{RST}$ input for restart of the module internal program in case of cycling.

The antenna (active or passive) is connected to terminal 3 (RF IN). The wire, connecting terminal 3 of the receiver with the antenna, must be implemented as microwave PCB line with wave resistance 50 Ohm. Terminals 1, 2, 4 and 5 (AGND) of the module are the high-frequency ground circuit for terminal 3. The power to the active antenna for receiving of signals from satellites shall be connected via built-in circuits of the module. The supply circuit of the active antenna is protected with a resettable fuse with trip current 100 mA. If the active antenna is used, provision should be made for the relevant load characteristics of the module power supply.

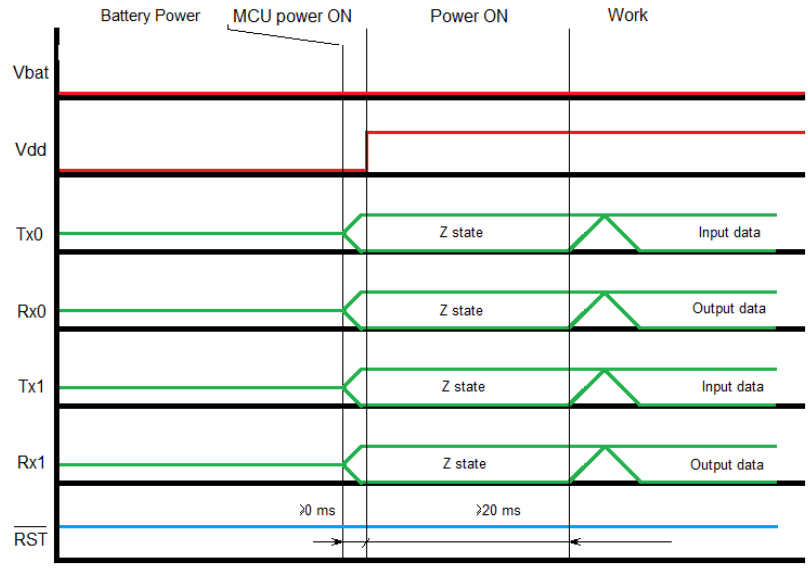

Fig. 7. The signal states and levels timing diagram at the module connection terminals when the module is used without Vbat.

For the module start operating, make sure to provide provision a logical level= "1" from 1.0 V to VDD on terminal pad 11 (ON/OFF); wise-versa, to switch the module off, apply to the terminal pad “ON/OFF” a logical level= "0" from 0 V to 0.4 V.

The output signal as a sequence of NMEA messages is generated via UART1 serial port (signal TXD1 pad 15, signal RXD1 pad 14). NMEA messages are present on this port in as built state.

Setting of the exchange rate via UART serial port, selection of GLONASS, GLONASS/GPS or GPS satellite constellations and other setups are performed through sending of special NMEA messages to the module.

UART0 port signals have output to terminals 13 and 12 of the receiver (signal TxD0 pad 13 and signal RxD0 pad 12). In as built state, this port is designed for programming of the receiver built-in flash memory. Depending on the program setups of the module, this port can be designed for transferring of information about differential corrections to the receiver, receiving of NMEA messages, loading of information about satellite positioning, etc. These signals are not designated in the diagram.

1PPS time sinchronisation signal has output to pad 16. This signal can be used by the customer's equipment for precise binding of the device time to UTC standard time. In the application schematic this signal is designated as 1PPS Out.

GND circuit must be connected to GND circuit of the peripheral device the module is used in.

Circuits GND and AGND must be integrated in one point that should be as close as possible to terminals 1, 2, 4 and 5.

In the application schematic, this connection is designated as resistor R1 0Ω (jumper). Integration of AGND circuit with other circuits is only allowed via GND circuit (in case of R1 removal, there should be no electrical contact of AGND with other circuits of the device). Failure to observe this instruction can reduce the sensitivity of the module to radio signals from satellites.

The connection terminals of the module designated as NC (not connected) must have electrical contact neither with each other nor with any circuits and elements of the device the module is used in.

Receiver module Control interfaces

The receiver operation control is performed with the use hardware features, as well as with special commands issued to the receiver.

The hardware features ensure on/off switching of the receiver at voltage being constantly on, hardware reset and selection of work/programming mode of functioning.

The receiver is switched on by appling of a high logic level signal to ENA input. The receiver is switched off by appling of a low logic level signal to ENA input.

For hardware reset of the receiver, a low logic level pulse is sent to $\overline{\text{RST}}$ input. The parameters of the pulse are set out above.

For selection of work/programming mode of functioning, relevant logical levels applies to connection terminals TxD0 and TxD1 at the moment of the receiver hardware reset pulse generation. In order to ensure functioning of the receiver in work mode, hold connection terminals TxD0 and TxD1 in Input state or high input impedance (Z state) at the moment of the receiver hardware reset pulse generation or for at least 20 milliseconds following its completion.

In order to switch the receiver into programming mode, hold TxD0 connection terminal in input state or high input impedance (Z state) and TxD1 connection terminal – in 0 (low logical level) state at the moment of the receiver hardware reset pulse generation or for at least 20 milliseconds following its completion.

A set of special commands with NMEA-like format is designed for control of program modes and parameters of the receiver. The commands are issued to RxD1 input. The description of the commands is provided in document The Set of NMEA Commands of GL8088s Receiver.pdf (available for developers upon request).

Maintenance

The receiver module does not require special types of maintenance.

Repairing procedure

The receiver module does not require any permamnet repair, provided that the rules of operation set forth in this Operations Manual, and requirements for operation, storage and transportation conditions are observed. If failures occur, the receiver must be returned to the manufacturer for subsequent repair.

Transportation and Storage

Packed receiver units can be transported by all transportation vehicles over distances up to 20,000 km without speed limitation at temperatures from -40°C to +85°C, subject to protection of receiver units from direct atmospheric exposure and mechanical damage according to the rules that comply with requirements of GOST 23088. The storage life of a packed receiver in heated storage facilities with controlled ambient temperature from + 5 to + 35°C and relative air humidity up to 80% at + 25°C temperature is 10 years minimum.