Genesys Logic, Inc.

GL827S

USB 2.0 Single Slot SD/MMC/MS/xD-Picture Card Reader Controller

Datasheet

Revision 1.06

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Revision History

Revision	Date	Description
1.00	2007/12/17	First formal release
1.01	2008/06/02	Modify feature description SD2.0 (SDHC), p.7
1.02	2008/08/08	1. Remove Smart Media support, p.7 2. Update Electrical and AC characteristic, p.14
1.03	2008/09/24	1. Update card power, p10 2. Update Electrical and AC characteristic, p.13
1.04	2008/12/17	Add QFN28 Pin: ● 28 Pinout, p.10 ● 28 Pin list/descriptions, p.11~12 ● 28 Pin Package, p.20
1.05	2009/03/11	Modified 1.Pinout, Ch3.1, p.8 2.Pin List/Description, Ch3.2, p.11~12 3.Update Electrical and AC characteristic, p13
1.06	2009/3/20	Modified 1. Pinout for QFN 28, Cha3.1, p.9 2. Pin List/Description for QFN 28, Cha3.2, p11~12

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CHAPTER 1 GENERAL DESCRIPTION

The GL827S is USB 2.0 Single Interface Flash Card Reader controller. It supports USB 2.0 high-speed transmission to Secure Digital™ (SD), SDHC, Mini SD™, Micro SD™ (T-Flash) , MultiMediaCard™ (MMC), RS MultiMediaCard™ (RS MMC), MMC Plus, MMC Micro, MMC-Mobile , Memory Stick™ (MS), Memory Stick Duo™ (MS Duo), High Speed Memory Stick™ (HS MS), Memory Stick PRO™ (MS PRO), Memory Stick PRO™ Duo (MS PRO Duo), Memory Stick PRO-HG™ (MS PRO-HG), Memory Stick ROM, MS PRO Micro, and xD-Picture Card ™ (xD) on one chip. As a single chip solution for USB 2.0 flash card reader, the GL827S complies with Universal Serial Bus specification rev. 2.0, USB Storage Class specification ver.1.0, and flash card interface specification each.

The GL827S can support different kinds of interfaces in single slot and integrates a high speed 8051 microprocessor and a high efficiency hardware engine for the best data transfer performance between USB and flash card interfaces.

The GL827S pin assignment design fits to card sockets to provide easier PCB layout. 48 Pin LQFP (7mm x 7mm) , QFN28 (5mm x 5mm) and QFN24 (4mm x 4mm) are available package types.

CHAPTER 2 FEATURES

- USB specification compliance
  - Comply with 480Mbps Universal Serial Bus specification rev. 2.0.
  - Comply with USB Storage Class specification rev. 1.0.
  - Support 1 device address and up to 4 endpoints: Control (0)/ Bulk Read (1)/ Bulk Write (2)/Interrupt (3).
- Integrated USB building blocks
  - USB2.0 transceiver macro (UTM), Serial Interface Engine (SIE), Build-in power-on reset (POR) and low-voltage detector (LVD)
- Embedded 8051 micro-controller
  - Operate @ 60 MHz clock, 12 clocks per instruction cycle
  - Embedded 48K Byte mask ROM and 256 byte SRAM
  - Support up to external 48K code ROM
- Secure Digital™ and MultiMediaCard™
  - Supports SD specification v1.0 / v1.1 / v2.0 (SDHC)
  - Supports MMC specification v3.X / v4.0 / v4.1 / v4.2.
  - x1 / x4 / x8 data transmission. (For QFN24/QFN28 up to x4)
  - Automatic CRC7 generation for command and CRC7 verification for response on CMD
  - Support automatic CRC16 generation and verification on DAT0:7
  - In addition to full packet transaction, optional single byte / bit operation on both CMD and DAT line / lines
  - Process data in block or byte
- Memory Stick™ / Memory Stick PRO / Memory Stick PRO Duo / Memory Stick Micro /Memory Stick PRO-HG
  - Comply with Memory Stick™ Rev.1.43, Memory Stick PRO™ Rev.1.04, Memory Stick Micro™ Rev.1.06, Memory Stick PRO-HG™ Rev.1.02
  - Support INS signal
  - Support automatic CRC16 generation and verification
  - Memory Stick PRO-HG 60MHz 8bit for LQFP48 / 40MHz 4bit for QFN24/QFN28
- xD-Picture (Only for LQFP48)
  - xD-Picture specification v1.21A. Type-H /Type-M /Type-M+
- On board 12 MHz Crystal driver circuit or 12/48 MHz Clock input.
- On-Chip 5V to 3.3V and 3.3V to 1.8V regulator. No external regulator required.
- On-Chip power MOSFETs for supplying flash media card power.
- Reduces the power consumption efficiently when the card reader is idle
- Available in 48 Pin LQFP (7x7 mm) package
- Available in 28 Pin QFN (5x5 mm) package
- Available in 24 Pin QFN (4x4 mm) package

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinout

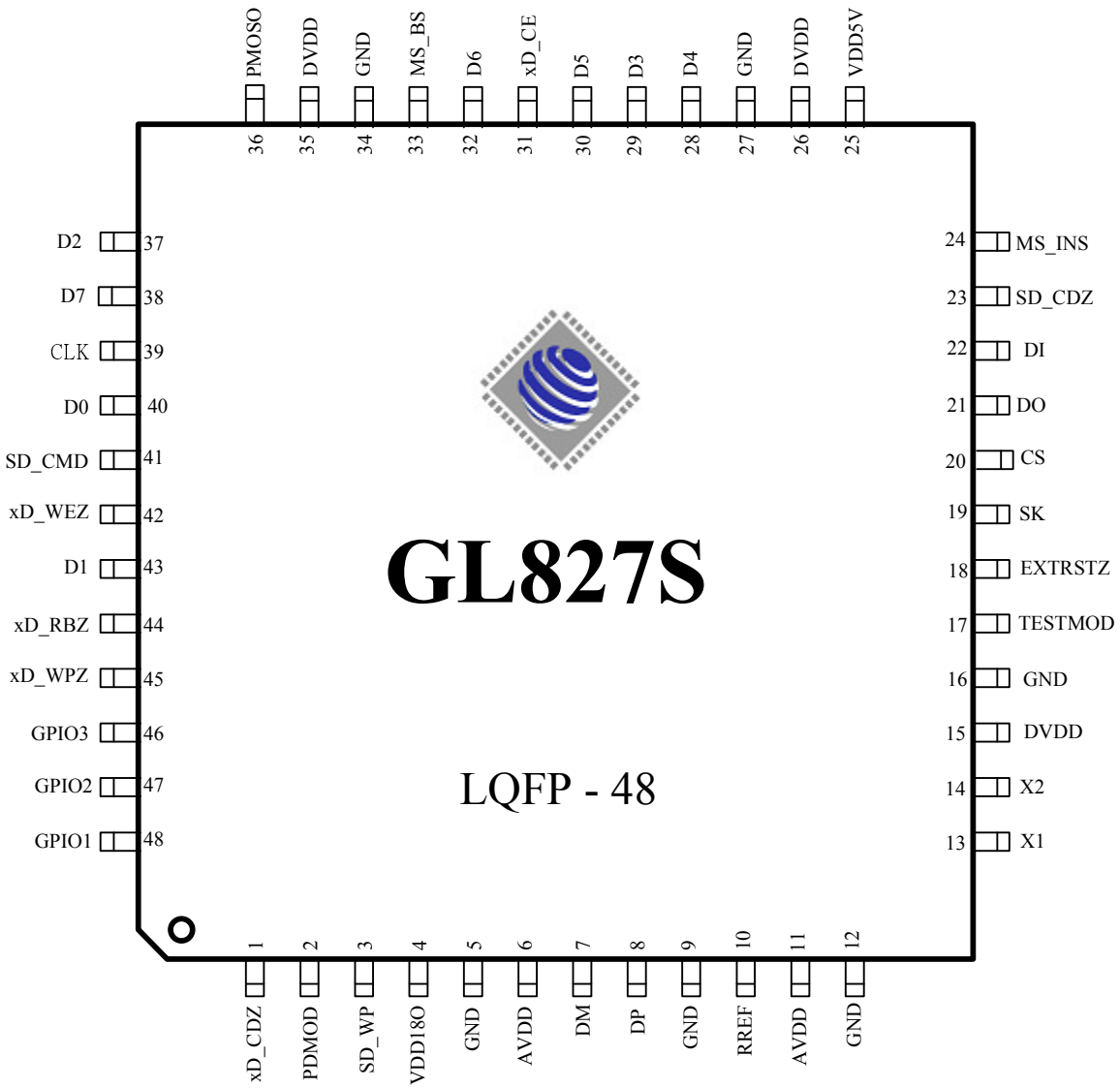


Figure 3.1 - 48 Pin LQFP Pin out Diagram

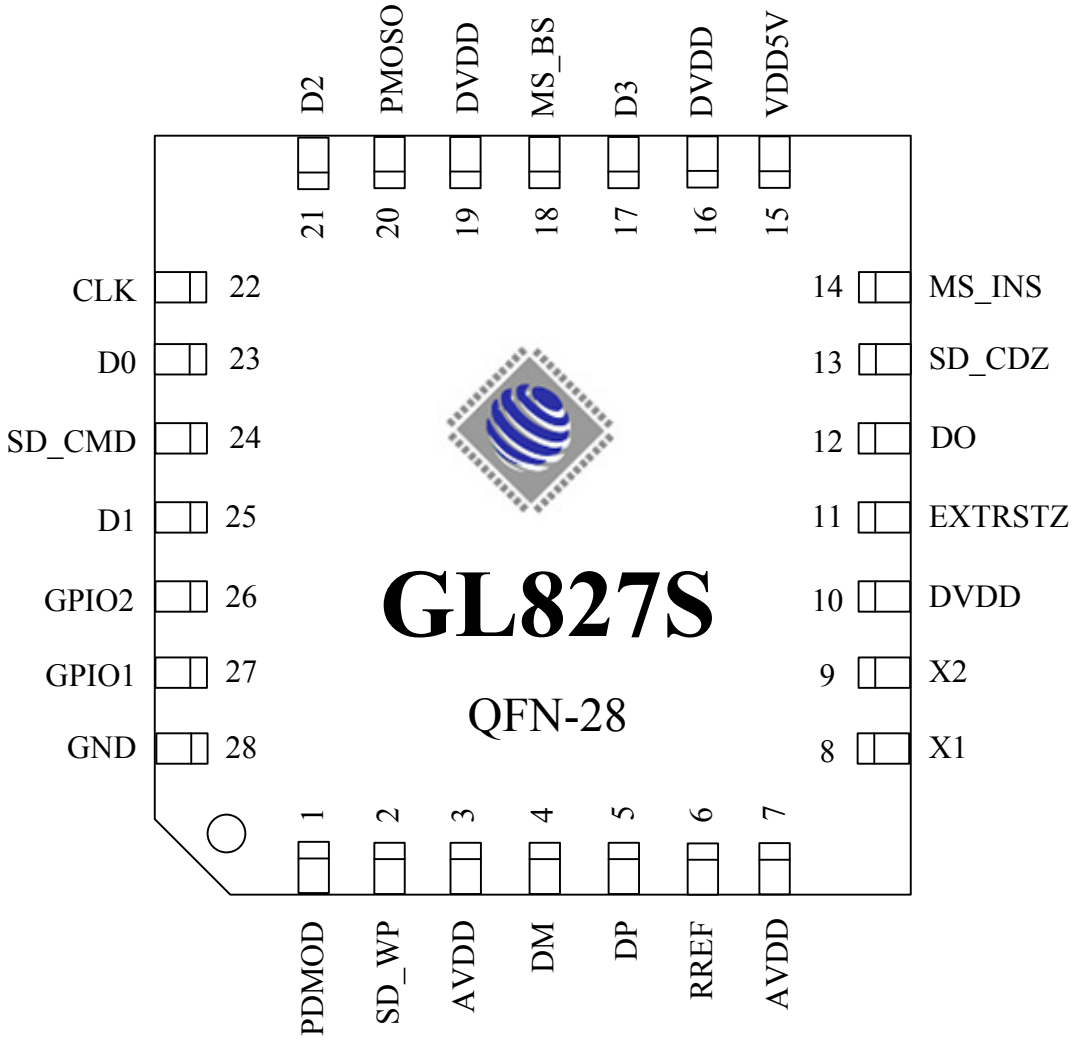


Figure 3.2 - 28 Pin QFN Pin out Diagram

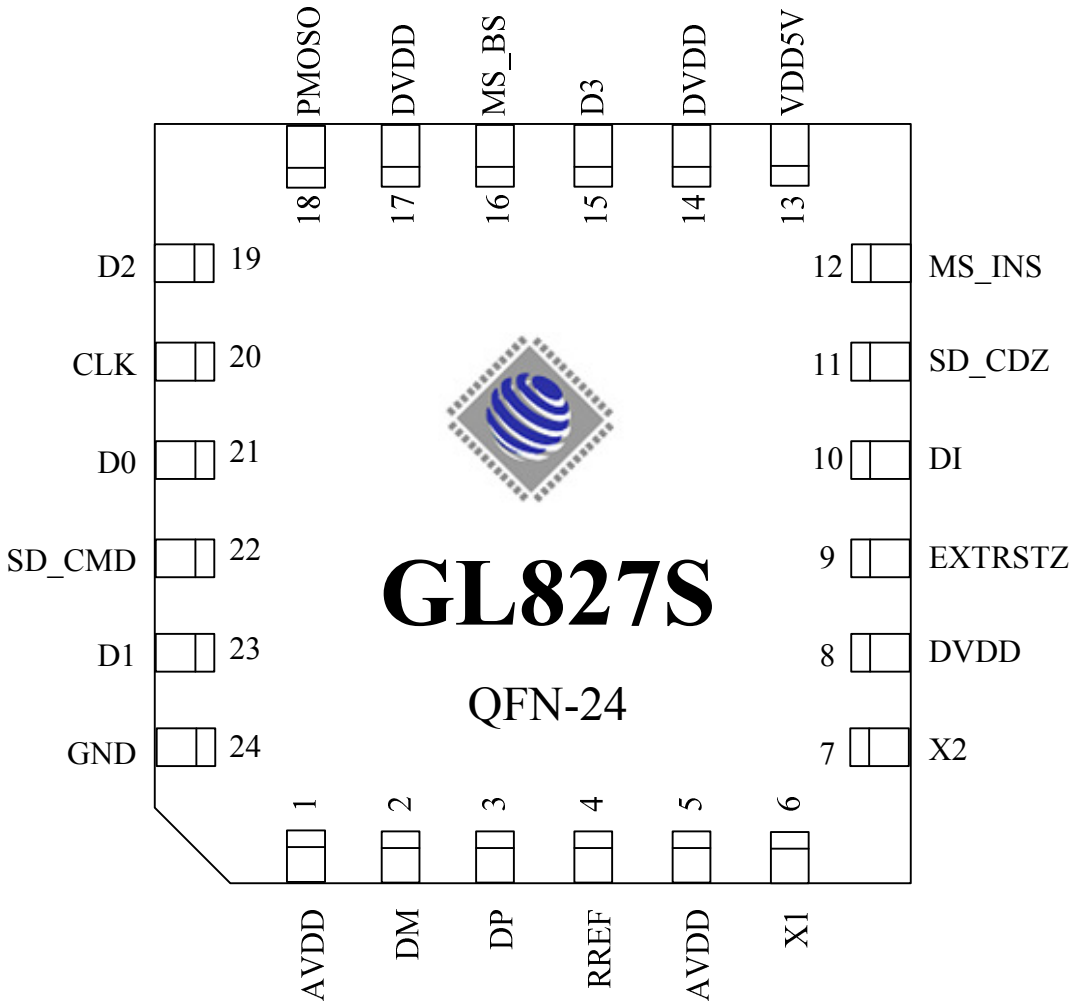


Figure 3.3 - 24 Pin QFN Pin out Diagram

3.2 Pin List/Descriptions

Table 3.1 - Pin Descriptions

Pin name	LQFP 48PIN	QFN 28PIN	QFN 24PIN	Type	Description
VDD18O	4	-	-	P	Internal regulator 1.8V output. For internal test usage
GND	5,9,12, 16,27,34	28	24	P	Ground
AVDD	6,11	3, 7	1,5	P	Analog power
DM	7	4	2	A	USB D-
DP	8	5	3	A	USB D+
RREF	10	6	4	A	Reference resistor
X1	13	8	6	I	12MHz XTAL input. It can be connected to external 12MHz/48MHz clock input.
X2	14	9	7	O	12MHz XTAL output.
DVDD	15,26,35	10, 16,19	8,14,17	P	Digital power 3.3V
VDD5V	25	15	13	P	Regulator 5V Input
PMOSO	36	20	18	P	Card power 250mA
TESTMOD	17	-	-	I, pd	Test mode selection
EXTRSTZ	18	11	9	I, pu	System reset, active low
PDMOD	2	1	-	I, pd	Power saving mode
xD_CDZ	1	-	-	I, pu	xD-Picture card detect 0: card insert 1: no card
MS_INS	24	14	12	I, pu	Memory Stick insertion detect 0: card insert 1: no card
SD_CDZ	23	13	11	I, pu	SD Card detect 0: card insert 1: no card
D0~D7	40,43,37,29,28,30,32,38	23, 25, 21, 17	21,23,19,15	B	xD data 0~7 MS/MS PRO data 0~7 SD data 0~3 MMC data 0~7
xD_CE	31	-	-	O	xD-Picture Card Enable
CLK	39	22	20	O	SD/MMC CLK/ Memory Stick SCLK output./ xD-Picture ALE
SD_WP	3	2	-	I, pd	SD Write Protect 0: write enable 1: write protect xD-Picture Write Protect 0: write protect 1: write enable
MS_BS	33	18	16	I, pd	MemoryStick BS/ xD-Picture CLE
SD_CMD	41	24	22	I, pd	SD/MMC CMD/ xD-Picture Read Enable#
xD_WEZ	42	-	-	I, pd	xD-Picture Write Enable#

xD_RBZ	44	-	-	I, pd	xD-Picture Ready/Busy#
xD_WPZ	45	-	-	I, pd	xD-Picture Write Protect#
GPIO1~3	48~46	27,26	-	B	GPIO1~3 / GPIO3 : Power LED
SK	19	-	-	O	93C46 Clock
CS	20	-	-	O	93C46 Chip Select
DO	21	12	-	O	93C46 Data out
DI	22	-	10	I, pd	93C46 Data in / ACCESS LED

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	P	Power / Ground
	A	Analog
	pu	Internal pull up
	pd	Internal pull down

CHAPTER 4 ELECTRICAL and AC CHARACTERISTICS

4.1 Absolute Maximum Ratings

Table 4.1 - Absolute Maximum Ratings

Parameter	Value
Storage Temperature	-65°C to +150 °C

4.2 Operating Conditions

Table 4.2 - Operating Conditions

Parameter	Value
Ta (Ambient Temperature Under Bias)	0°C to 70°C
Supply Voltage	+4.75V to +5.25V
Ground Voltage	0V
F_{OSC} (Oscillator or Crystal Frequency)	12 MHz ± 0.05% 12 MHz ± 0.25% (for USB full-speed only)

4.3 DC Characteristics

Table 4.3 - DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage		4.75	-	5.25	V
V_{IH}	Input High Voltage		2.0	-	3.65	V
V_{IL}	Input Low Voltage		-0.5	-	0.4	V
I_I	Input Leakage current	$0 < V_{IN} < 3.3v$	-10	-	10	µA
V_{OH}	Output High Voltage		3.0	-	-	V
V_{OL}	Output Low Voltage		-	-	0.4	V
I_{OH}	Output Current High		-	8	-	mA
I_{OL}	Output Current Low			8	-	mA
C_{IN}	Input Pin Capacitance		-	5	-	pF

4.4 5V to 3.3 V Regulator Characteristics

Table 4.4 – Regulator Output Current

Parameters	Description	Test Conditions	Typ..	Units
Iq	Quiescent current	no loading	18	uA
Io_max	Output driving capability	V33 > 2.9V	350	mA
Vo_0mA	V33 voltage without loading		3.33	V
Vo_200mA	V33 voltage with 200mA load		3.18	V
Vo_250mA	V33 voltage with 250mA load		3.04	V

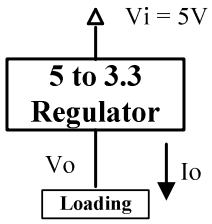


Figure 4.1 - 5V to 3.3 V Regulator Architecture

4.5 PMOS Characteristics

Table 4.5 - PMOS I-V table

(IO Power=3.3V, Temperature 25 °C)

Driving Loading (mA)	Vd output voltage(V)
100mA	**3.21**
200mA	**3.11**
250mA	**2.93**

Note:

1. Driving strength is defined as the PMOS sinking current when Vio=3.3V

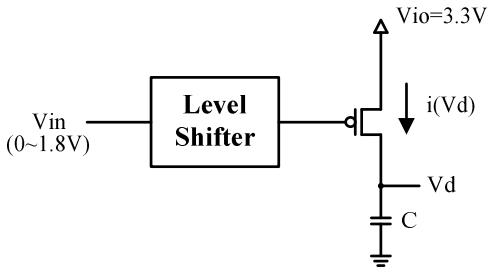


Figure 4.2 - Embedded PMOS Switch Architecture

4.6 Reset Timing

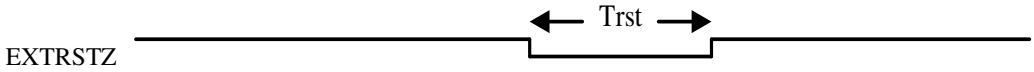


Figure 4.3 - Timing Diagram of Reset width

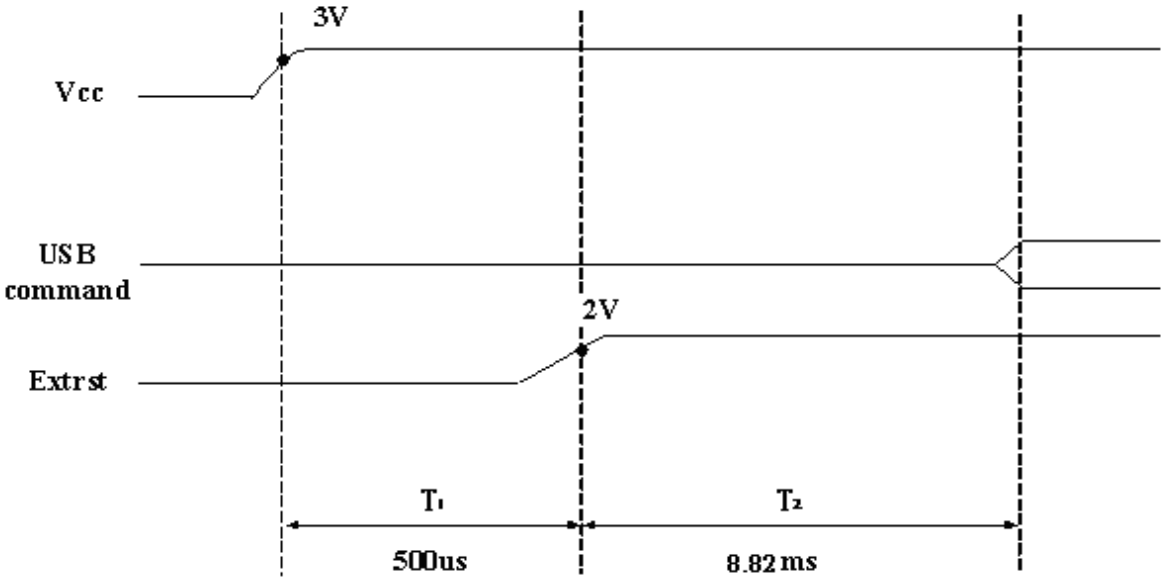


Figure 4.4 - Timing Diagram of Power Good to USB command receive ready

Parameter	Description	Min	Unit
Trst	Chip reset sense timing width	2	us
T1	External reset valid from power up to high	500	us
T2	Reset deassertion to respond USB command ready	8.82	ms

CHAPTER 5 BLOCK DIAGRAM

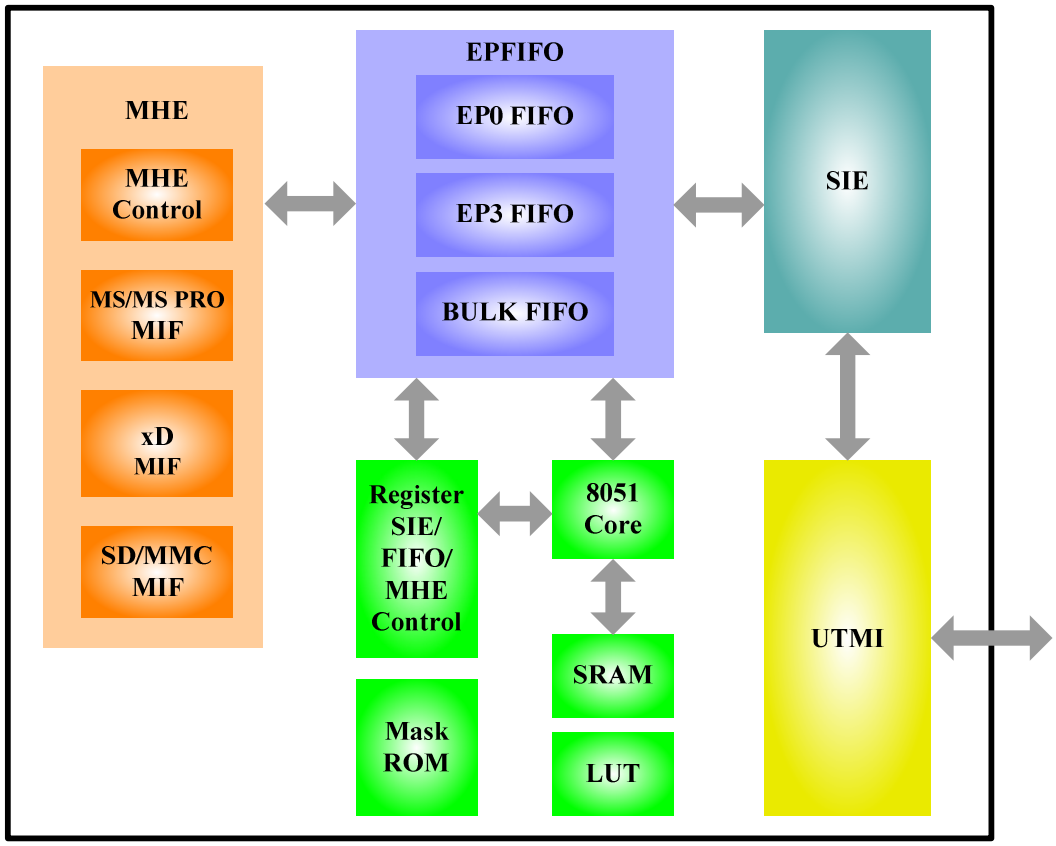


Figure 5.1 - Block Diagram

CHAPTER 6 FUNCTION DESCRIPTION

UTM

The USB 2.0 Transceiver Macrocell is the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic.

SIE

The Serial Interface Engine, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

EPFIFO

Endpoint FIFO includes Control FIFO (FIFO0), interrupt FIFO (FIFO3), Bulk In/Out FIFO (BULKFIFO)

- **Control FIFO** FIFO of control endpoint 0.
  It is 64-byte FIFO, and it is used for endpoint 0 data transfer.
- **Interrupt FIFO** 64-byte depth FIFO of endpoint 3 for status interrupt
- **Bulk In/Out FIFO** It can be in the TX mode or RX mode:
  1. It contains ping-pong FIFO (512 bytes each bank) for transmit/receive data continuously.
  2. It can be directly accessed by Uc

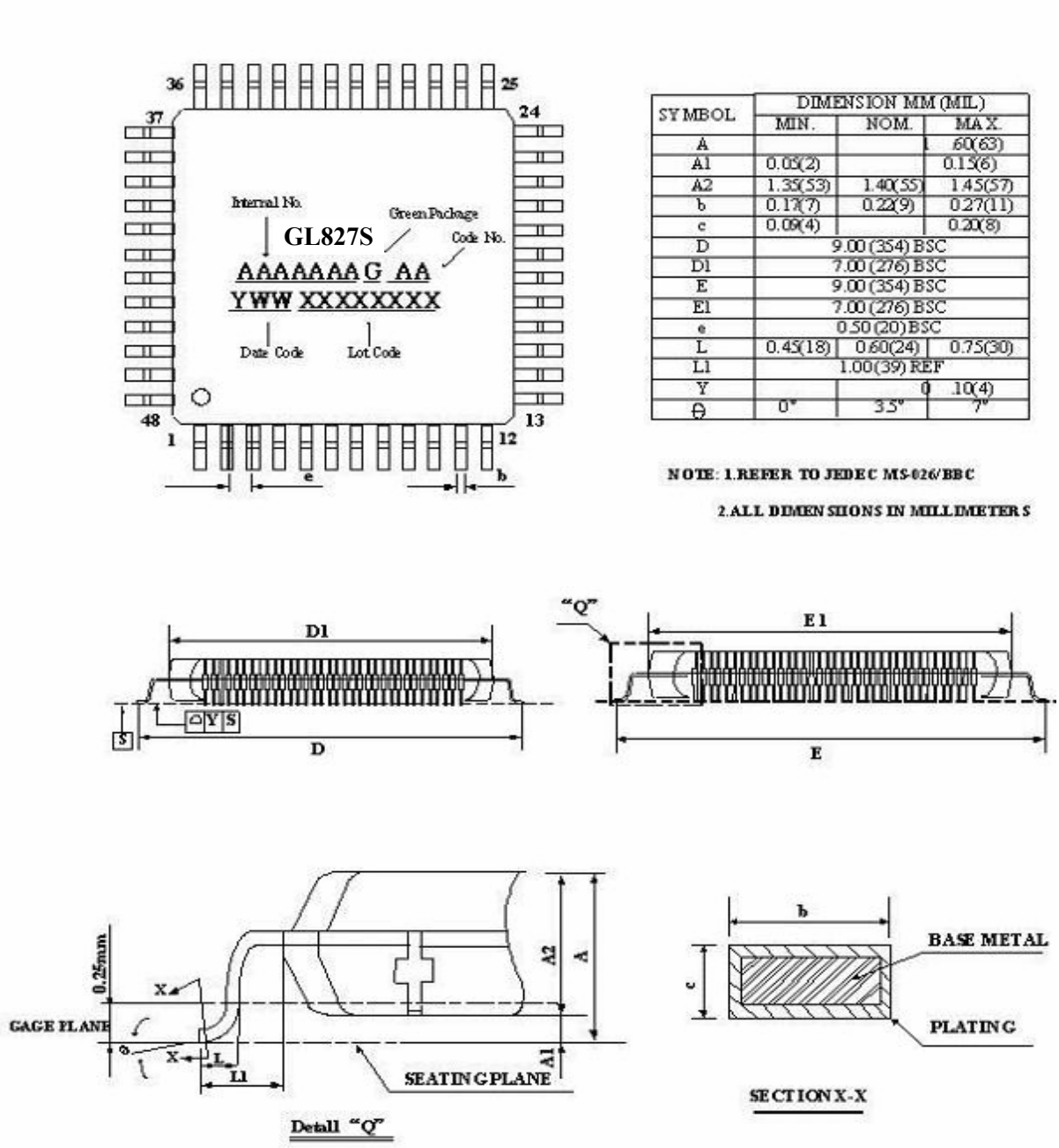
MHE

It contains 3 MIFs (Media Interface)

- **MIFs**
  1. SD / MMC
  2. MemoryStick/ MemoryStick PRO / MemoryStick PRO-HG
  3. xD-Picture

- **External reset circuit**
  Non-inverting, Schmitt input with weak pull-up using DVDD power.

CHAPTER 7 PACKAGE DIMENSION



SYMBOL	DIMENSION MM (MIL.)		
	MIN.	NOM.	MAX.
A			1.60(63)
A1	0.05(2)		0.15(6)
A2	1.35(53)	1.40(55)	1.45(57)
b	0.17(7)	0.22(9)	0.27(11)
c	0.09(4)		0.20(8)
D	9.00 (354) BSC		
D1	7.00 (276) BSC		
E	9.00 (354) BSC		
E1	7.00 (276) BSC		
e	0.50 (20) BSC		
L	0.45(18)	0.60(24)	0.75(30)
L1	1.00(39) REF		
Y			0.10(4)
θ	0°	3.5°	7°

Figure 7.1 – GL827S 48 Pin LQFP Package

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (28)	0.75 (30)	0.80 (32)
A1	0 (0)	0.02 (0.8)	0.05 (2)
A2		0.20 (8) REF	
b	0.18 (7)	0.25 (10)	0.30 (12)
D		5.00 (197) BSC	
D1	3.40 (134)	3.50 (138)	3.60 (142)
E		5.00 (197) BSC	
E1	3.40 (134)	3.50 (138)	3.60 (142)
e		0.50 (20) BSC	
L	0.30 (12)	0.40 (16)	0.50 (20)
y	---	0.80 (3)	---

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

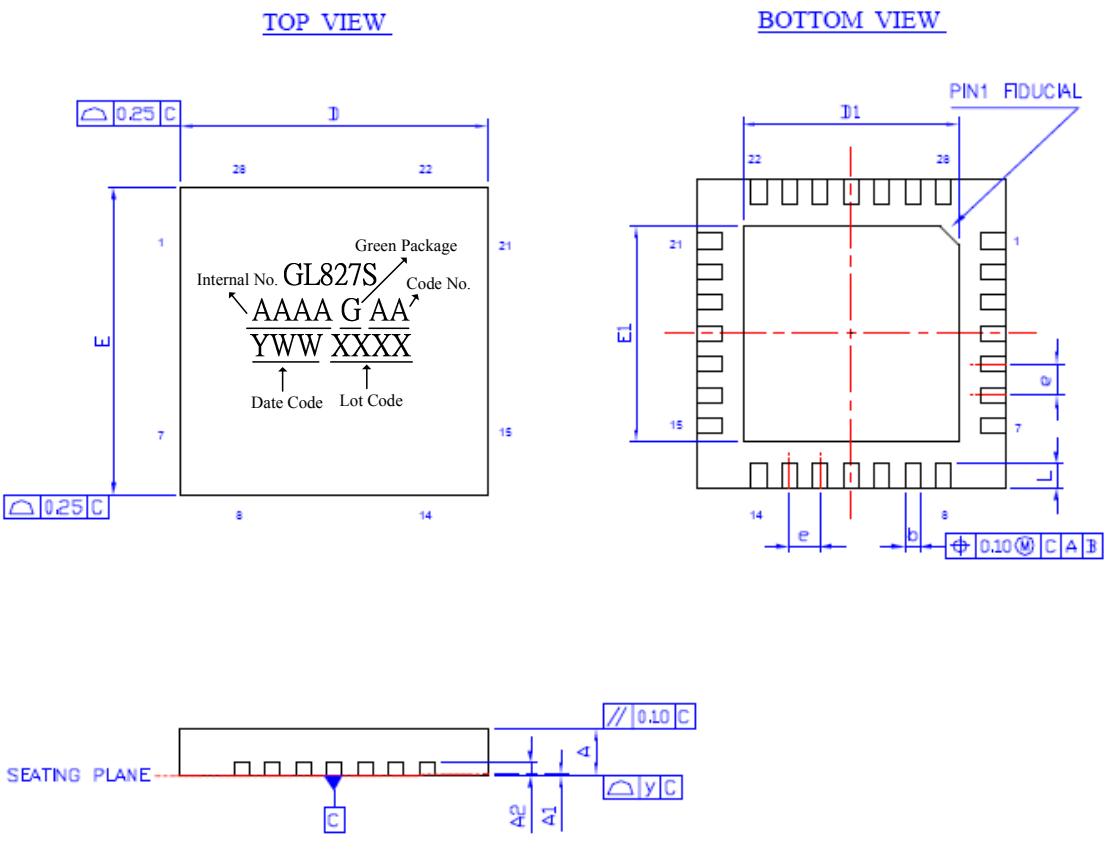


Figure 7.2 – GL827S 28 Pin QFN Package

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (28)	0.75 (30)	0.80 (32)
A1	0.00 (0)	0.02 (0.8)	0.05 (2)
A3	0.20 (8) REF		
b	0.18 (7)	0.25 (10)	0.30 (12)
D	3.90 (154)	4.00 (158)	4.10 (161)
E	3.90 (154)	4.00 (158)	4.10 (161)
D2	1.90 (75)	2.00 (79)	2.10 (83)
E2	1.90 (75)	2.00 (79)	2.10 (83)
e	0.50 (20) BSC		
L	0.30 (12)	0.40 (16)	0.50 (20)
y	0.08 (3)		

NOTE: 1. REFER TO JEDEC MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

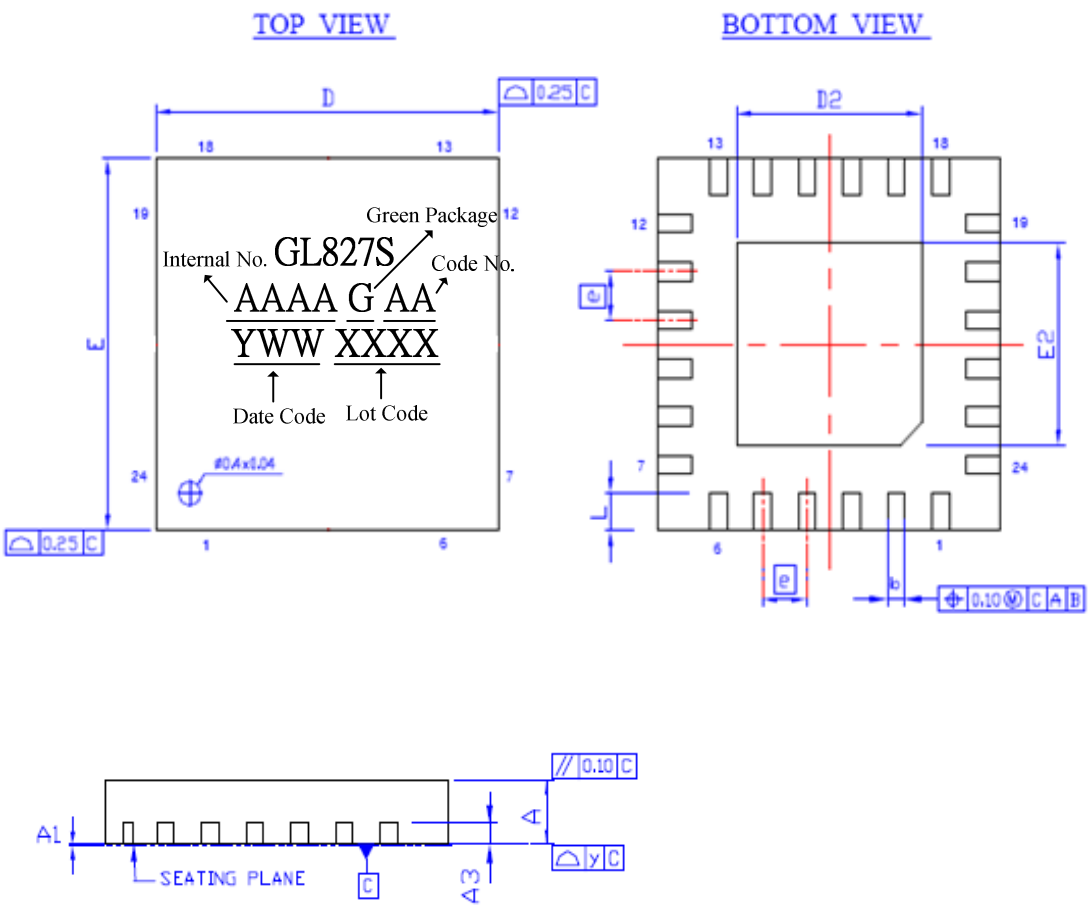


Figure 7.3 – GL827S 24 Pin QFN Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Normal/Green	Version	Status
GL827S-MNG	48-pin LQFP	Green Package	XX	Available
GL827S-OHG	28-pin QFN	Green Package	XX	Available
GL827S-OGG	24-pin QFN	Green Package	XX	Available