Genesys Logic, Inc.

GL831A

SATA / PATA
Bridge Controller

Datasheet

Rev. 1.03
Jul 27, 2009

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Revision History

Revision	Date	Description
1.00	12/18/2008	First formal release
1.01	01/21/2009	Add Power Consumption, Ch6.5, p.15
1.02	04/09/2009	Modify features, Ch2, p.7 Modify figure 3.1 - 64 pin LQFP pinout diagram, p.8 Add power output pin description, p. 11 Modify power consumption Ch6.3.6, p.15
1.03	07/27/2009	Add Ch2 features, p.7 Modify power consumption-table 6.6, p.15 Add 6.3.7 reset timing, p.15

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CHAPTER 1 GENERAL DESCRIPTION

The GL831A is a highly-compatible, low cost SATA to PATA and PATA to SATA bridge controller, which integrates Genesys Logic own design Serial ATA PHY. As a one-chip solution which complies with Serial ATA specification rev. 2.6 and ATA / ATAPI-6 specification rev 1.0, the GL831A can support various kinds of ATA / ATAPI device in SATA to PATA and SATA device in PATA to SATA. The GL831A uses 25MHz crystal and slew-rate controlled pads to reduce the EMI issue. With 64-pin LQFP (7X7mm) package, the GL831A is the best cost/ performance solution for SATA to PATA and PATA to SATA application.

CHAPTER 2 FEATURES

· Complies with ATA/ATAPI-6 specification rev 1.0

· Support 16-bit Multiword DMA mode and Ultra DMA mode interface

· Operating system supported: Win Vista/ Win XP / 2000 / Me / 98 / 98SE; Mac OS 9.X / X

· Complies with Serial ATA specification rev. 2.6

· Support Spread Spectrum Clocking to reduce EMI

· Support SATA hot-plug

· Provide adjustable TX signal amplitude and pre-emphasis level

· Provide specified OOB signal detection and transmission

· Supports 1.5Gbps data rate

· Supports both Host/Device controller configuration

· Support SATA 25MHz external crystal

· Support Mater/Slave setting

· 3.3V power input; 5V tolerance pad

· Embedded Regulator (3.3V to 1.8V)

· Available in 64 pin LQFP

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinouts

Figure 3.1 - 64 Pin LQFP Pinout Diagram

3.2 Pin List

Table 3.1 - Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	BUSY	O	17	DEVICE1	I	33	INTRQ	B	49	RTERM	A
2	DD7	B	18	HOST	I	34	VDD	P	50	PLLVDD	P
3	DD8	B	19	DD2	B	35	CVDD	P	51	PLLVDD	P
4	HRST_	I	20	DD13	B	36	DA1	B	52	PLLVSS	P
5	DD6	B	21	DD1	B	37	DA0	B	53	TXVSS	P
6	DD9	B	22	DD14	B	38	DA2	B	54	TXVDD	P
7	DD5	B	23	DD0	B	39	CS0_	B	55	TXP	O
8	CVDD	P	24	DD15	B	40	CS1_	B	56	TXN	O
9	VDD	P	25	CVDD	P	41	GND	P	57	RXN	I
10	GND	P	26	GND	P	42	VDD	P	58	RXP	I
11	DD10	B	27	VDD	P	43	GND	P	59	RXVDD	P
12	TEST	I	28	DMARQ	B	44	VDD	P	60	RXVSS	P
13	DD4	B	29	DIOW_	B	45	X2	B	61	CVDD	P
14	DD11	B	30	DIOR_	B	46	X1	I	62	GND	P
15	DD3	B	31	IORDY	B	47	CVDD	P	63	RESET#	B
16	DD12	B	32	DMACK_	B	48	GND	P	64	SPDSEL	I

3.3 Pin Descriptions

Table 3.2 - Pin Descriptions

ATA/ ATAPI Interface (Host mode)			
Pin Name	**Pin#**	**Type**	**Description**
DD0~15	23, 21, 19, 15, 13, 7, 5, 2, 3, 6, 11, 14, 16, 20, 22, 24	B	IDE Data Bus
RESET#	63	I (pu)	Device Reset
CS1_, CS0_	40, 39	I (pu)	Chip Select #1,#0
DA0~2	37, 36, 38	I (pd)	IDE Address #2,#1,#0
INTRQ	33	O	IDE interrupt input

DMACK_	32	I (pu)	IDE Acknowledge
IORDY	31	O	IDE Ready
DIOR_	30	I (pu)	IDE read signal
DIOW_	29	I (pu)	IDE write signal
DMARQ	28	O	IDE request

ATA/ ATAPI Interface (Device mode)			
Pin Name	**Pin#**	**Type**	**Description**
DD0~15	22, 20, 18, 15, 13, 7, 5, 2, 3, 6, 11, 14, 16, 19, 21, 23	B	IDE Data Bus
RESET#	63	O	Device Reset
CS1_, CS0_	40, 39	O	Chip Select #1,#0
DA0~2	37, 36, 38	O	IDE Address #2,#1,#0
INTRQ	33	I (pd)	IDE interrupt input
DMACK_	32	O	IDE Acknowledge
IORDY	31	I (pu)	IDE Ready
DIOR_	30	O	IDE read signal
DIOW_	29	O	IDE write signal
DMARQ	28	I (pd)	IDE request

SATA Interface			
Pin Name	**Pin#**	**Type**	**Description**
RTERM	49	A	Reference resistor
PLLVDD	50, 51	P	1.8V Power Supplies for internal PLL
PLLVSS	52	P	Ground for internal PLL
TXVSS	53	P	1.8V Power Supplies for transceiver part
TXVDD	54	P	Ground for transceiver part
TXP	55	O	SATA Differential Transmit TX+
TXN	56	O	SATA Differential Transmit TX-
RXN	57	I	SATA Differential Receive RX-
RXP	58	I	SATA Differential Receive RX+
RXVDD	59	P	1.8V Power Supplies for receiver part
RXVSS	60	P	Ground for receiver part

Digital Power and Ground			
Pin Name	**Pin#**	**Type**	**Description**
CVDD	8, 25, 35, 61	P	1.8V Digital Power (Pin 8 is internal regulator 3.3V to 1.8V output pin)
VDD	9, 27, 34, 42, 44	P	3.3V Digital Power (Pin 9 is internal regulator 3.3V to 1.8V input pin)
GND	10, 26, 41, 43, 120	P	Digital Ground

Miscellaneous Interface			
Pin Name	**Pin#**	**Type**	**Description**
TEST	12	I (pd)	Test Mode Input
X2	45	B	Crystal Output
X1	46	I	Crystal Input
HRST_	4	I (pu)	Reset Pin
HOST	18	I (pd)	1=> Host mode; 0=> Device mode
BUSY	1	O	Busy LED
SPDSEL	64	I (pd)	0 => force in 1.5G; 1 => negotiate interface speed with attached device (1.5G or 3G)
DEVICE1	17	I (pd)	0 => ATA device 0; 1=> ATA device 1 in host mode

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	B/I	Bi-directional, default input
	B/O	Bi-directional, default output
	P	Power / Ground
	A	Analog
	SO	Automatic output low when suspend
	pu	Internal pull up
	pd	Internal pull down
	odpu	Open drain with internal pull up

CHAPTER 4 BLOCK DIAGRAM

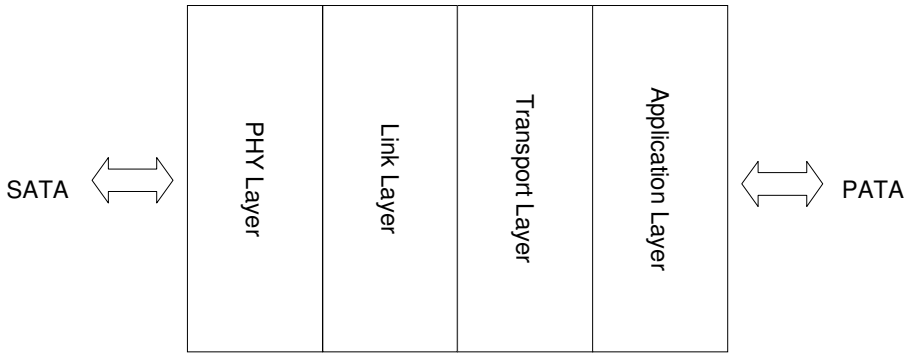

Figure 4.1 - Block Diagram

CHAPTER 5 FUNCTION DESCRIPTION

5.1 PHY Layer

It has elastic buffer and supports receiver detection, data serialization and de-serialization.

5.2 Link Layer

The Link layer transmits and receives frames, transmits primitives based on control signals from the Transport layer, and receives primitives from the Phy layer which are converted to control signals to the Transport layer.

5.3 Transport Layer

The Transport layer constructs Frame Information Structures for transmission and decomposes received Frame Information Structure

5.4 Application Layer

The Application Layer contains an ATA engine and translates the ATA operation onto internal protocols.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Table 6.1 - Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IO}	Digital I/O pad power supply voltage	3.0	3.3	3.6	V
Vcore	Digital power supply voltage	1.62	1.8	1.98	V
V_{ASATA}	Analog power supply voltage for SATA PHY	1.62	1,8	1.98	V
V_{ESD}	Static discharge voltage	4000			V
T_A	Ambient Temperature	0		100	°C

6.2 Temperature Conditions

Table 6.2 - Temperature Conditions

Item	Value
Storage Temperature	-50°C ~ 150 °C
Operating Temperature	0 °C ~ 70 °C

6.3 DC Characteristics

6.3.1 I/O Type Digital Pins

Table 6.3 - I/O Type Digital Pins

Parameter	Min.	Typ.	Max.	Unit
Current sink @ V_{OL} = 0.4V	10.58	14.21	16.87	mA
Current output @ V_{OH} = 2.4V (TTL high)	14.74	27.46	43.0	mA
Falling slew rate at 30 pF loading capacitance	0.56	0.91	1.28	V/ns
Rising slew rate at 30 pF loading capacitance	0.58	0.91	1.72	V/ns
Schmitt trigger low to high threshold point	1.4	1.5	1.6	V
Schmitt trigger low to high threshold point	1.4	1.5	1.6	V
Pad internal pull up resister	37.87K	64.7K	108.11K	Ohms
Pad internal pull down resister	29.85K	59.45K	134.26K	Ohms

6.3.2 PATA Interface DC Characteristics

The GL831A conforms to DC characteristics for ATA/ATAPI-6specification rev 1.0. Please refer to this specification for more information.

6.3.3 SATA Interface DC Characteristics

The GL831A conforms to DC characteristics for Serial ATA specification rev. 2.6. Please refer to this specification for more information.

6.3.4 Reference Clock Input Requirement

Table 6.4 - Reference Clock Input Requirement

Parameter	Min.	Typ.	Max.	Unit
X1 crystal frequency		25		MHz
X1 cycle time		40		ns

6.3.5 Reference Resistor Requirement

Table 6.5 - Reference Resistor Requirement

Parameter	Min.	Typ.	Max.	Unit
SATA Reference Resistor		5.1K		Ohms

6.3.6 Power Consumption

Table 6.6 - Power Consumption

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{3.3V}$	3.3V power Dissipation (3.3V system power source input)			135	mA

Power Domain	Description	Voltage	Power Dissipation
IO	Digital Input/Output pad	3.3V	5mA
Crystal	Crystal pad		
Core	Digital core power supply	1.8V	126~128mA
SATA digital	SATA Serdes digital power		
SATA Analog	Analog power supply for SATA PHY		

6.3.7 Reset Timing

GL831A's power on reset is triggered by external reset circuit. The power on sequence will start from power on and should be released after PGOOD is asserted. It is approximately 380us from power on.

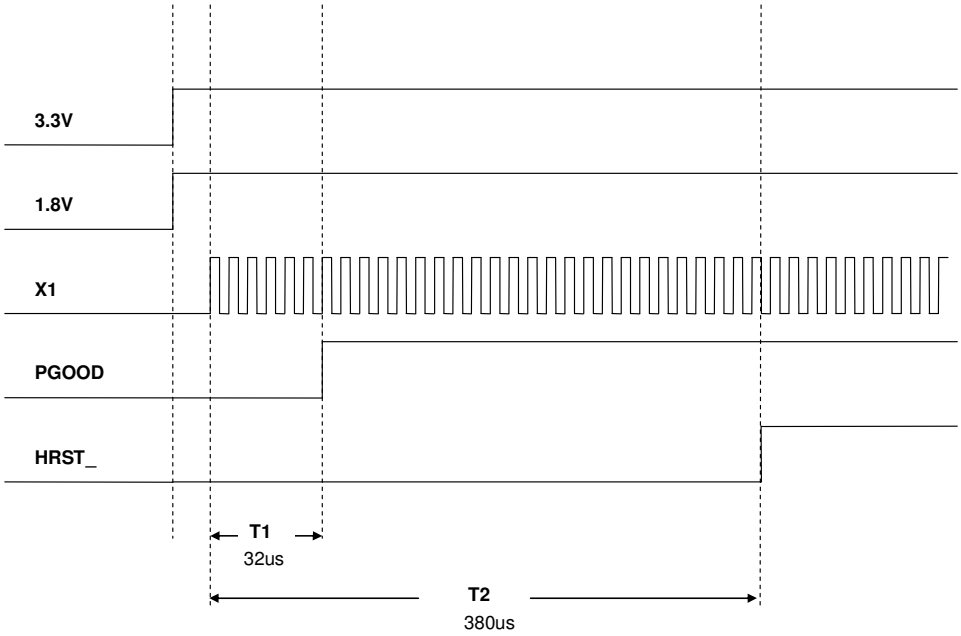

Figure 6.1 - Reset Timing

6.4 AC Characteristics

6.4.1 PATA Interface AC Characteristics

The GL831A conforms to DC characteristics for ATA/ATAPI-6specification rev 1.0. Please refer to this specification for more information.

6.4.2 SATA Interface AC Characteristics

The GL831A conforms to all timing diagrams and specifications for Serial ATA specification rev. 2.6. Please refer to this specification for more information.

CHAPTER 7 PACKAGE DIMENSION

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A			1.60 (63)
A1	0.05 (2)		0.15 (6)
A2	1.35 (53)	1.40 (55)	1.45 (57)
b	0.13 (5)	0.18 (7)	0.23 (9)
c	0.09 (4)		0.20 (8)
D	9.00 (354) BSC		
D1	7.00 (276) BSC		
E	9.00 (354) BSC		
E1	7.00 (276) BSC		
e	0.40 (15.8) BSC		
L	0.45 (18)	0.60 (24)	0.75 (30)
L1	1.00 (39) REF		
Y			0.10 (4)
θ	0°	3.5°	7°

NOTE: 1. REFER TO JEDEC MS-026(ISSUE C)/BBD
2. ALL DIMENSIONS IN MILLIMETERS.

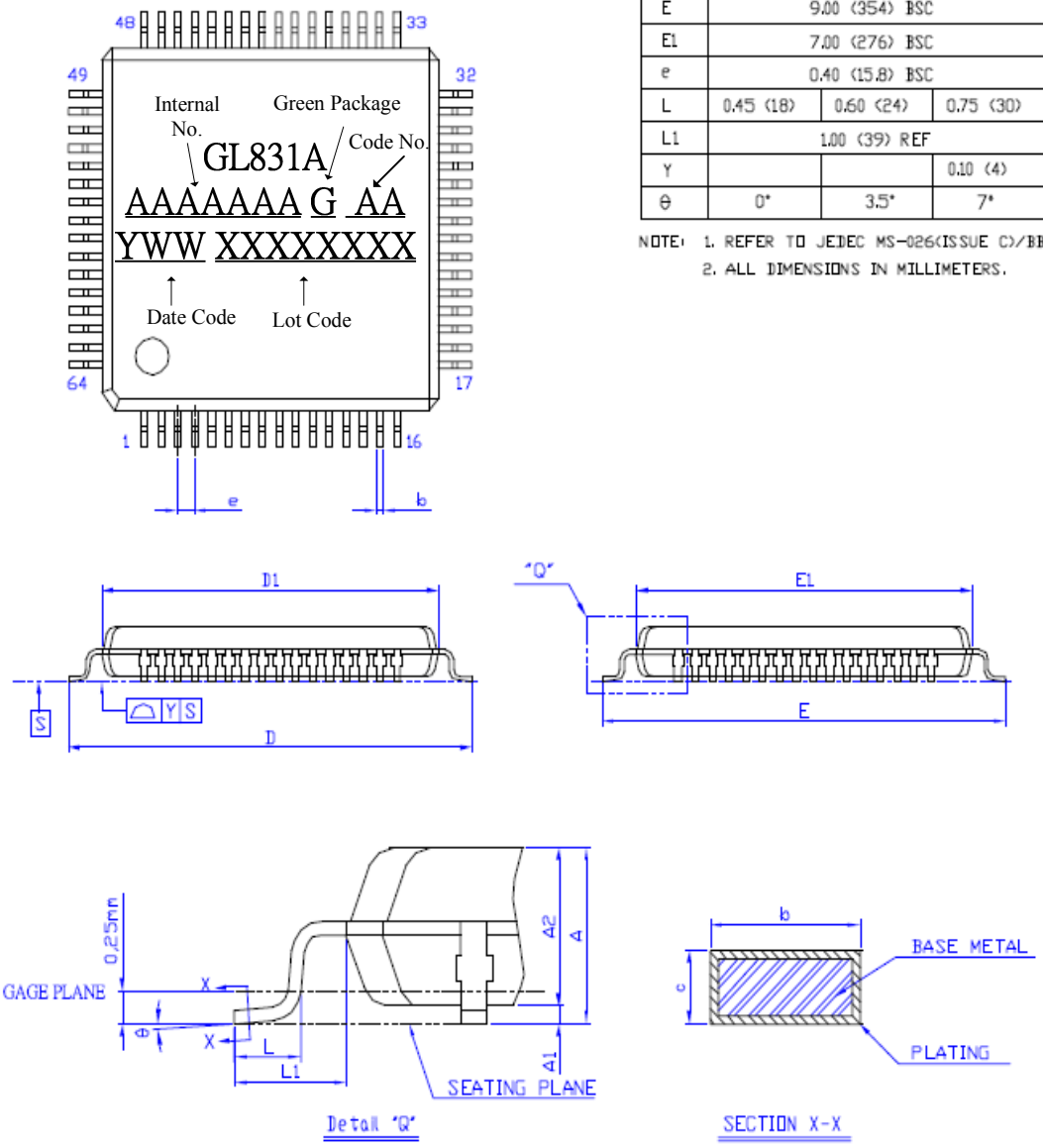

Figure 7.1 - LQFP 64 Pin Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Green	Version	Status
GL831A-MSGXX	64 pin LQFP	Green Package	XX	Available