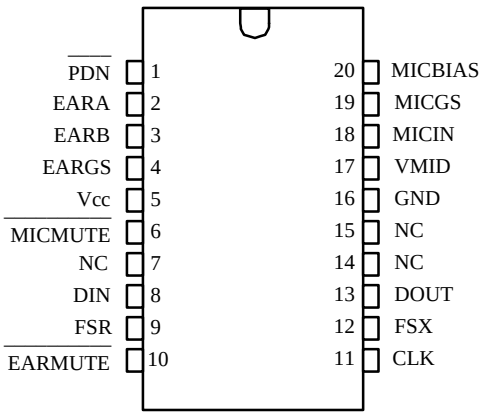
GM0936TQ

Voice-Band Audio CODEC for CDMA

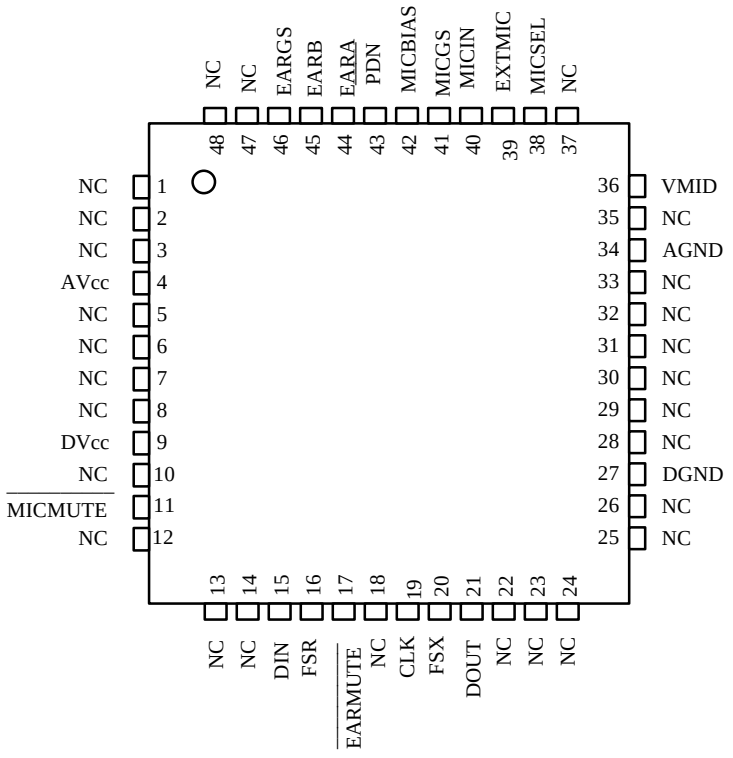
Features

- Single 3-V operation
- Low power consumption
  - Operating mode .... 20mW Typ
  - Power-down mode ... 1mW Typ
- Combined A/D, D/A, and Filters
- Electret microphone bias reference voltage available
- Compatible with all digital signal processors (DSPs)
- Programmable volume control
- 300 Hz - 3.6 kHz Passband with Specified Master clock
- Designed for standard 2.048MHz master clock for U.S. Analog, U.S. Digital, CT2, DECT, GSM, and PCS Standards for Hand-held Battery-Powered Telephones
- On-chip voltage references
- Package Type : 48 LQFP, 20 DIP, 20 SOP

20 DIP/SOP
(TOP VIEW)



48 LQFP
(TOP VIEW)



Description

The GM0936TQ contains A/D and D/A conversion functions integrated on a single chip, and utilizes the sigma-delta modulation technique to achieve high resolution data conversion and low power consumption. The GM0936TQ is an ideal analog front end device for high performance voice-band communication systems. Cellular telephone systems are targeted in particular; however, these integrated circuits can function in other systems including digital audio, telecommunications, and data acquisition.

The transmit section is designed to interface directly with an electret microphone element. One of two microphone input signals, MICIN and EXTMIC, is selected by MICSEL. If MICSEL is floated or Low, then MICIN is selected, and if MICSEL is high, then EXTMIC is selected. The microphone input signal (MICIN and EXTMIC) is buffered, first-order low-pass filtered, and amplified with provision for setting the amplifier gain to accommodate a range of signal input levels. The amplified signal is 1bit-modulated by second-order sigma-delta modulator. The modulated signal is then applied to the input of high-performance FIR-type digital decimation filters with frequency response equalization. The resulting data is then clocked out of DOUT as a serial data stream.

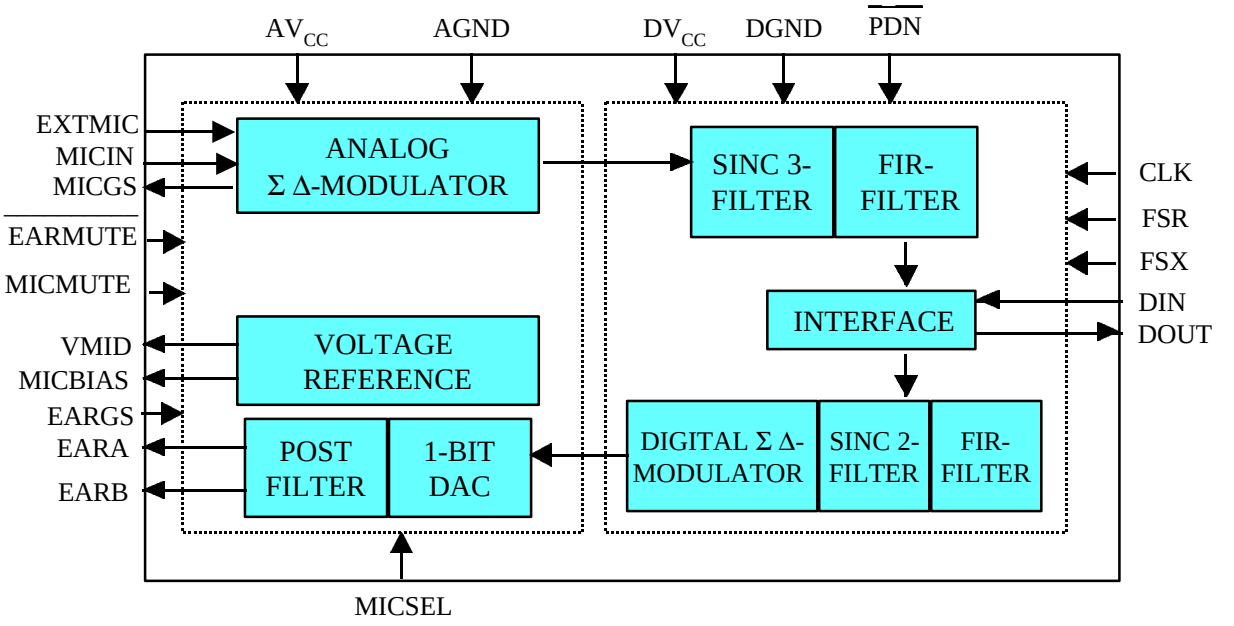
The receive section takes a frame of sereal data on DIN and converts it to analog through high-performance FIR-type digital interpolation filter together with frequency response equalization, second-order digital sigma-delta modulator, and analog reconstruction filters.

On-chip voltage reference ensures a highly integrated solution and all internal voltage references are generated. An internal reference voltage, VMID, is used to develop the midlevel virtual ground for all the amplifier circuits and the microphone bias circuit.Another reference voltage, MICBIAS, can supply bias current for the microphone.

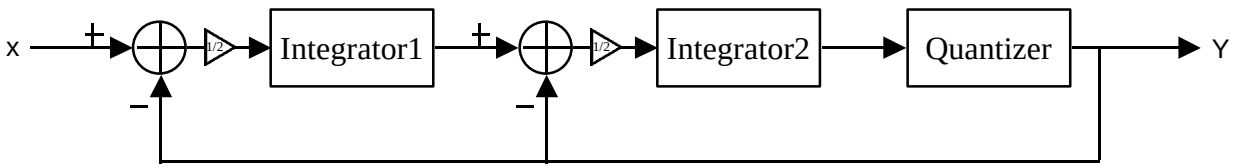
Serial DSP interfaces for transmit and receive paths support directly industry standard DSP processors.

The GM0936TQ devices are characterized for operation from -20 to 70¡ É

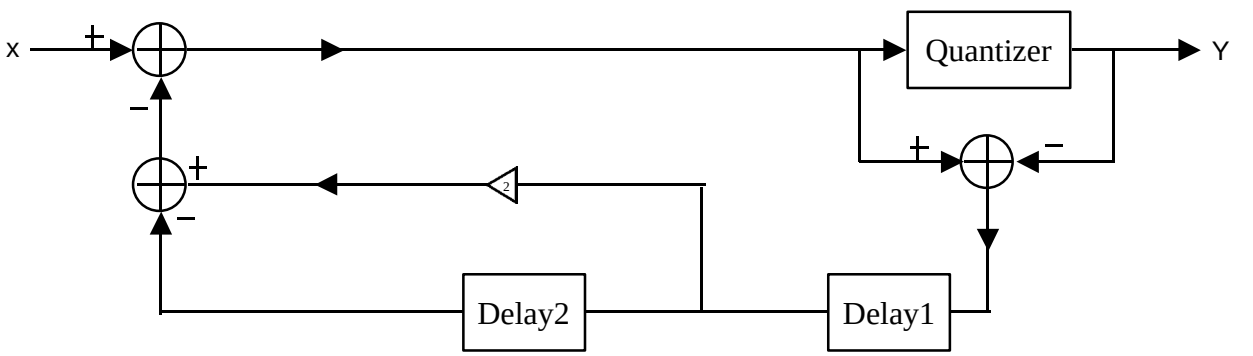
Block Diagram



Analog 2nd orderS -D **Modulator Block Diagram**



Digital 2nd order S -D **Modulator Block Diagram**



Pin Description

ANALOG SIGNALS

TERMINAL NAME	LQFP	SOP&DIP	I/O	DESCRIPTION
AGND	34	16		Analog Ground
AVcc	4	5		Analog Power (3V)
EARA	44	2	O	Earphone output
EARB	45	3	O	Side-tone output
EARGS	46	4	I	Side-tone input
EARMUTE_	17	10	I	Earphone output mute control signal
MICBIAS	42	20	O	Microphone bias
MICGS	41	19	O	Output of the internal microphone amplifier
MICIN	40	18	I	Microphone input
MICMUTE_	11	6	I	Microphone input mute
VMID	36	17	O	Bias voltage reference. A pair of external, low-leakage, high-frequency capacitors (1 μF and 470 pF) should be connected between VMID and ground for filtering
ETMIC	39	N/A	I	Hand-free MIC-IN
MICSEL	38	N/A	I	MIC-IN selection input. When float or low, MICSEL selects MICIN. When high, MICSEL selects EXTMIC.

Pin Description

DIGITAL SIGNALS

TERMINAL NAME	LQFP	SOP&DIP	I/O	DESCRIPTION
CLK	19	11	I	Clock input (2.048 MHz)
DGND	27	16		Digital ground
DIN	15	8	I	Receive data input
DOUT	21	13	O	Transmit data output
DVcc	9	5		Digital power (3 V)
FSR	16	9	I	Frame-synchronization clock input for receive channel
FSX	20	12	I	Frame-synchronization clock input for receive channel
PDN	43	1	I	Power-down input, Active Low
NC	1,2,3, 5,6,7, 8,10, 12,13, 14,18, 22,23, 24,25, 26,28, 29,30, 31,32, 33,35	7, 14, 15		No internal connection

Electrical Characteristics

Absolute Maximum Ratings over operating free-air temperature range

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage Range	DV_{CC}, AV_{CC}	- 0.3		3.6	V
Digital Input Voltage Range	V_{ind}	- 0.3		3.6	V
Analog Input Voltage Range	V_{ina}	- 0.3		3.6	V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	DV_{CC}, AV_{CC}	2.7	3.0	3.3	V
High-level Input Voltage	V_{IH}	2.2			V
Low-level Input Voltage	V_{IL}			0.8	V
Operating free-air Temperature	T_A	-20		70	¡ É

Power Supply Characteristics, f_{CLK} = 2.048 MHz, outputs not loaded, Vcc=3V, T_A=25¡ É

PARAMETER	MIN	TYP	MAX	UNIT
Power Dissipation , Operating		18		mW
Power Dissipation , Power down		1		mW

Digital Characteristics (T_A=25¡ É, DV_{CC} = AV_{CC} = 3V)

PARAMETER	MIN	TYP	MAX	UNIT
Input Capacitance			10	pF
Input Leakage Current	- 10		10	§ Ë
Low-level output Voltage (I_{OL} = 3.2mA)			0.4	V
High-level output Voltage (I_{OH} = -3.2mA)	2.4			V

Microphone interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage at MICIN		V_I= 0 to 3 V			±5	mV
I_{IB} Input bias current at MICIN					±200	nA
B_1 Unity-gain bandwidth, open loop at MICIN				1.5		MHz
Av Large-signal voltage amplification at MICGS				10000		V/V
Iomax Maximum output current	VMID		3			µA
	MICBIAS(source only)		1			mA

Speaker interface

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(PP)}$ AC output voltage				3	Vpp
I_{Omax} Maximum output current	R_L = 600 Ω			±1	mA
r_o Output resistance at EARA, EARB			1		Ω
Gain change	EARMUTE low, max level when muted	-60			dB

Analog Characteristics (T_A=25¡ É, DV_{CC} = AV_{CC} = 3V, fs = 8 KHz)

A/D Converter

PARAMETER	MIN	TYP	MAX	UNIT
Oversampling Ratio		128		
Resolution		13		bit
Dynamic Range		70		dB
S/(N+THD)	50	52		dB
Output Sample Rate		8		KHz
Maximum output current for MICBIAS	1			mA
Maximum output voltage for Microphone Amplifier	0.85		0.95	Vpp

Transmit filter transfer over recommended ranges of supply voltage and free-air temperature, CLK=2.048 MHz, FSX=8 kHz

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gain relative to input signal at 1.02 kHz	Input amplifier set for unity gain, the output for 400mVpp signal at MICGS is 0dB	f_{MICIN} = 50 Hz		0.76		dB
		f_{MICIN} = 200 Hz		0.73		
		f_{MICIN} = 300 Hz		0.67		
		f_{MICIN} = 1 kHz		0		
		f_{MICIN} = 2 kHz		-1.9		
		f_{MICIN} = 3 kHz		-4.5		
		f_{MICIN} = 3.3 kHz		-5.4		
		f_{MICIN} = 3.8 kHz		-8.9		

Transmit idle channel noise and distortion, linear mode selected, over recommended ranges of supply voltage and free-air temperature (see Notes 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmit noise	MICIN connected to MICGS through a 22 kΩ resistor		178		μV_{rms}
Gain relative to input signal at 1.02 kHz	MICIN to DOUT at 0 dBm0		53		dB
	MICIN to DOUT at -3 dBm0		52.3		
	MICIN to DOUT at -6 dBm0		51.9		
	MICIN to DOUT at -9 dBm0		50.7		
	MICIN to DOUT at -12 dBm0		49.0		

Notes: 1. The input amplifier is set for inverting unity gain.
2. Transmit noise, linear mode: 200 μV_{rms} is equivalent to -75 dB (referenced to device 0 dB level).

D/A Converter

PARAMETER	MIN	TYP	MAX	UNIT
Oversampling Ratio		128		
Resolution		13		bit
Dynamic Range		67		dB
S/(N+THD)	48	54		dB
Maximum output current (R_L =600§ Ù			± 1	mA
Output Voltage Range	0.81		0.91	Vpp

Receive distortion, linear mode selected, over recommended ranges of supply voltage and free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA at 0 dBm0		60		dB
	DIN to EARA at -3 dBm0		59.7		
	DIN to EARA at -6 dBm0		59.6		
	DIN to EARA at -9 dBm0		56.1		
	DIN to EARA at -12 dBm0		55.3		

Power supply rejection over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage rejection, transmit channel	Idle channel, supply signal = 100mVrms f = 1 kHz (measured at DOUT)		-50		dB
Supply voltage rejection, receive channel	Idle channel, supply signal = 100mVrms f = 1 kHz (measured at EARA)		-50		dB

Timing (T_A=25¡ É, DV_{CC} = AV_{CC} = 3V)

PARAMETER	MIN	TYP	MAX	UNIT
CLK Frequency		2.048		MHz
Sampling Rate		8		KHz
DOUT Delay from CLK			35	ns
DIN Delay from CLK			35	ns

Clock timing requirements

	MIN NOM MAX	UNIT
Duty cycle, CLK	45% 50% 55%	

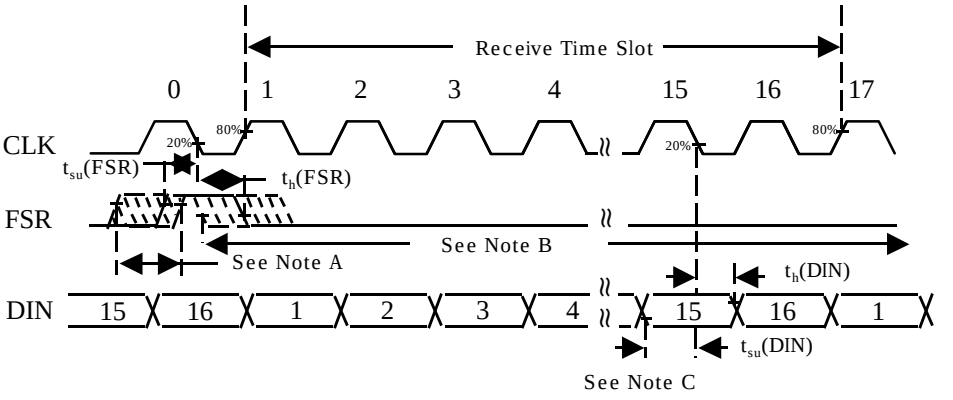
Transmit timing requirements

	MIN MAX	UNIT
t_{su}(FSX) Setup time, FSX high before CLK ¡ é	20 468	ns
t_h(FSX) Hold time, FSX high after CLK ¡ é	20 468	ns

Receive timing requirements

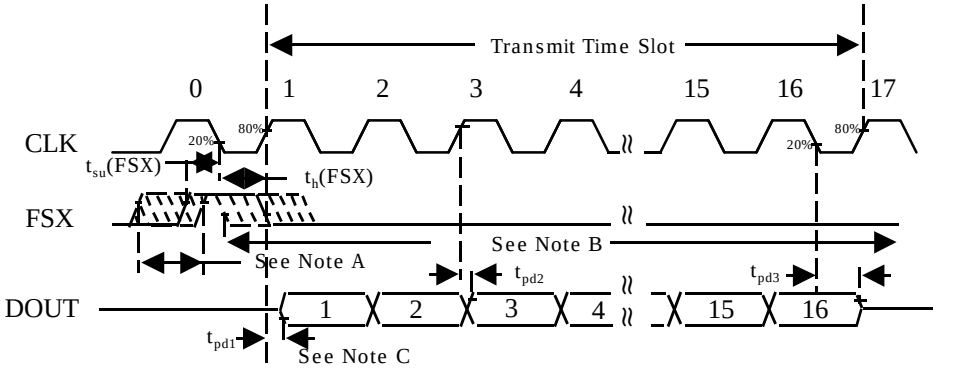
	MIN MAX	UNIT
t_{su}(FSR) Setup time, FSR high before CLK ¡ é	20 468	ns
t_h(FSR) Hold time, FSR high after CLK ¡ é	20 468	ns
t_{su}(DIN) Setup time, DIN high or low before CLK ¡ é	20	ns
t_h(DIN) Hold time, DIN high or low after CLK ¡ é	20	ns

Timing Diagram



NOTES: A. This window is allowed for FSR high.
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

Figure1. Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low.
C. Transitions are measured at 50%.

Figure2. Transmit Side Timing Diagram

PRINCIPLES OF OPERATION

power-down operation

To minimize power consumption, a power-down mode is provided.
For power down, an external low signal is applied to PDN. In the absence of a signal, PDN is internally pulled up to a high logic level and the device remains active. In the power-down mode, the average power consumption is reduced to 1mW.

Timing

FSX and FSR are inputs that set the sampling frequency. Data is transmitted on DOUT on the positive transitions of CLK following the rising edge of FSX. Data is received on DIN on the falling edges of CLK following FSR.

Table 1. Power-On and Power-Down Procedures

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power on	$\overline{PDN}$ =high, FSX = pulses, FSR = pulses	20 mW	Digital outputs active
Power down	$\overline{PDN}$ =low, FSX,FSR =X	1 mW	DOUT in the high-impedance state

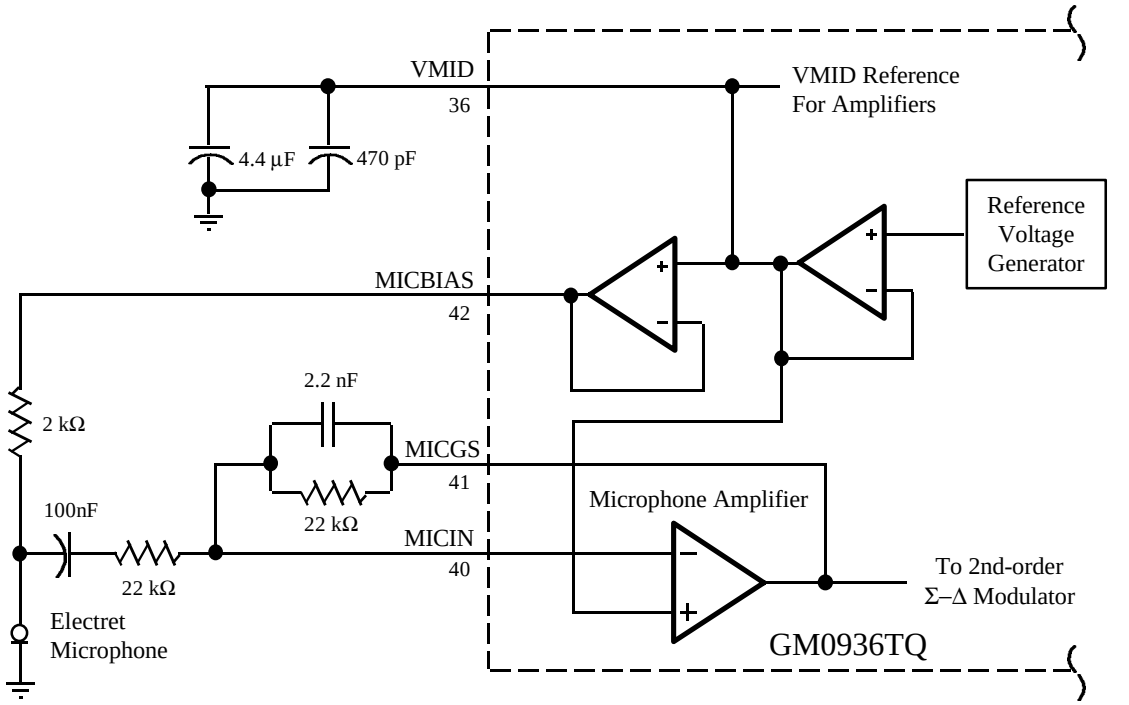
X = dont care

PRINCIPLES OF OPERATION

transmit operation

microphone input

The microphone input amplifier is designed specifically to interface to electret-type microphone elements, as shown in Figure 3. The VMID buffer circuit provides a voltage (MICBIAS) as a bias voltage to the electret microphone. The microphone amplifier output (MICGS) is used in conjunction with a feedback network and applied to the amplifier inverting input (MICIN) to set the amplifier gain. VMID appears at a terminal to provide a place to filter the VMID voltage.



NOTE A: Terminal numbers shown are for the 48 LQFP package.

Figure 3. Typical Microphone Interface

microphone mute function

The MICMUTE input causes the digital circuitry to transmit all zero code on DOUT.

transmit filter

A low-pass antialiasing section is implemented by connecting a RC-pair externally between MICGS and MICIN. The RC-pair, together with the microphone amplifier, provides a single-pole low pass filter. The antialiased signal is 1bit-modulated by second-order sigma-delta modulator. The modulated signal is then applied to the input of high-performance FIR-type digital decimation filters with frequency response equalization.

PRINCIPLES OF OPERATION

encoding

The encoder performs an A/D conversion on a 2nd-order Sigma-Delta (Σ-Δ) modulator using a switched-capacitor technology and high-performance FIR-type digital decimation filters with frequency response equalization. The resulting data is then clocked out of DOUT as a serial data.

data word structure

The data word is 16 bits long. The first 13 bits comprises the audio data sample, and the last three bits form the volume control word in the receive direction (DIN) and are zero pad bits in the transmit direction (DOUT). The sign bit is transmitted first.

receive operation

decoding

The serial data word is received at DIN on the first 13 clock cycles. The receive section converts a frame of sereal data to analog through high-performance FIR-type digital interpolation filter together with frequency response equalization, second-order digital sigma-delta modulator, and analog reconstruction filters.

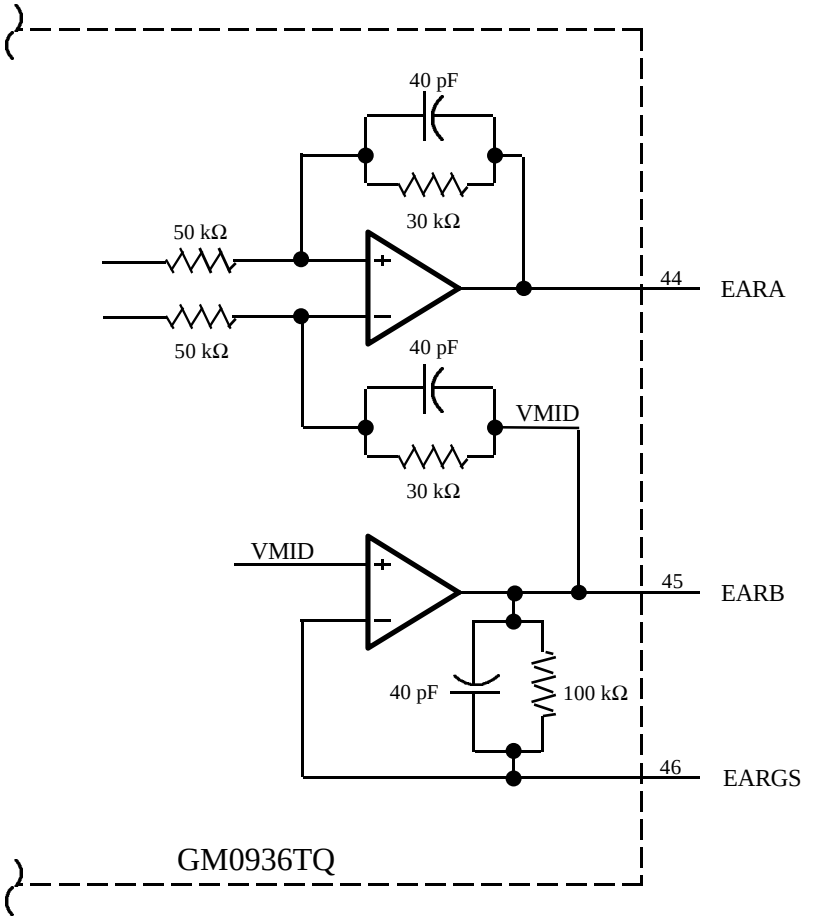
receive buffer

The receive buffer contains the volume control.

earphone amplifier

The output can be used to drive a single-ended load with the output signal voltage centered around VMID. EARA in Figure 4 is the output pin for the decoded analog signal. EARB in the figure is used for sidetone signal output which is used internally. A resistor-capacitor pair attached to EARB is embedded to reduce the number of on-board components. See the next section for more information on sidetone generation.

PRINCIPLES OF OPERATION



NOTE A: Terminal numbers shown are for the 48 LQFP package.

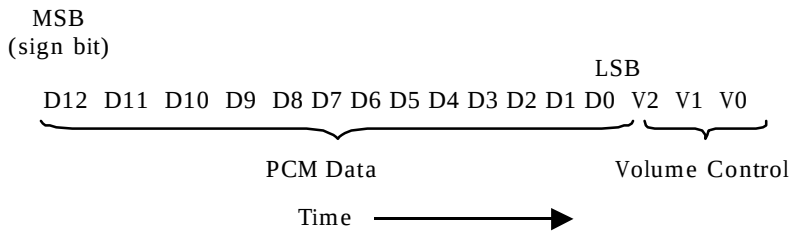
Figure 4. Earphone Audio-Output Amplifier Configuration

receive data format

In the decoding operation, 16 bits of data are received. The first 13 bits are the D/A code, and the remaining three bits from the volume control word(see Table 2). The volume control function is actually an attenuation control in which the first bit received is the most significant. The maximum volume occurs when all three volume control bits are zero. Eight levels of attenuation are selectable in 3-dB steps, giving a maximum attenuation of 21 dB when all bits are 1s. The volume control bit are not latched into the GM0936TQ and must be present in each received data word.

Table 2. Receive-Data Bit Definitions

BIT NO.	Data
0	D12
1	D11
2	D10
3	D9
4	D8
5	D7
6	D6
7	D5
8	D4
9	D3
A	D2
B	D1
C	D0
D	V2
E	V1
F	V0

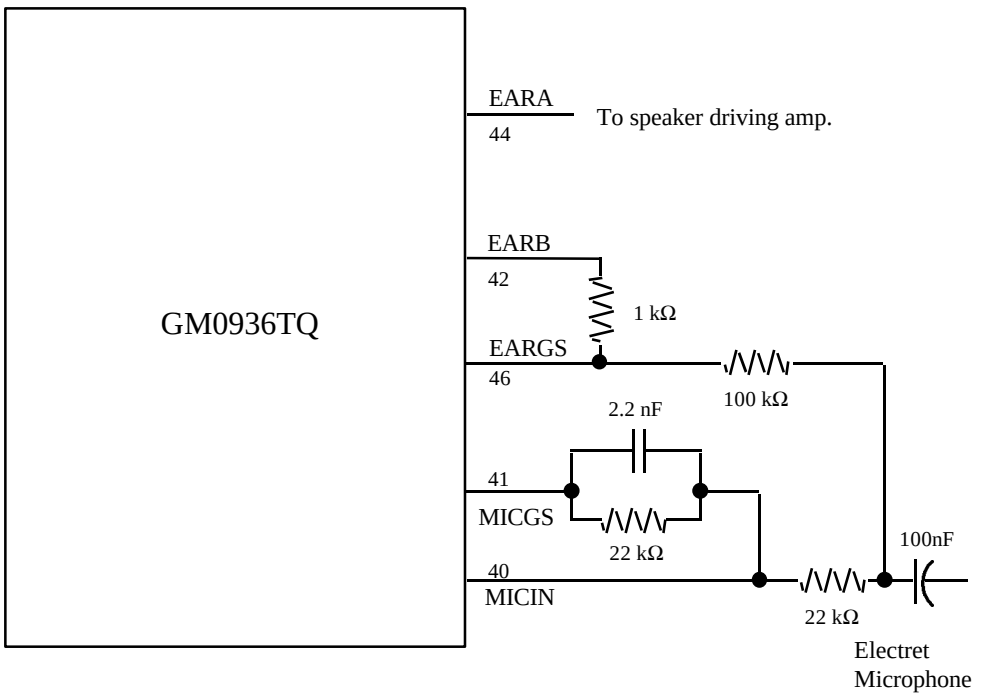


Where:
D12-D0 = PCM Data word
V2, V1, V0 = Volume (attenuation control) 000 = maximum volume, 0 dB
111 = minimum volume, -21 dB

APPLICATION INFORMATION

output gain set and sidetone considerations

The single-ended outputs EARA and EARB are capable of driving output power level up to 1mW into load impedance of 1kΩ separately.The sidetone signal and the received signal can be summed by configuring external components like in Figure 5. The amount of sidetone mixing is controlled by the resistor connected between EARB and EARGS. If the resistance become greater, the amount of sidetone mixing increases.



NOTE A: Terminal numbers shown are for the 48 TQFP package.

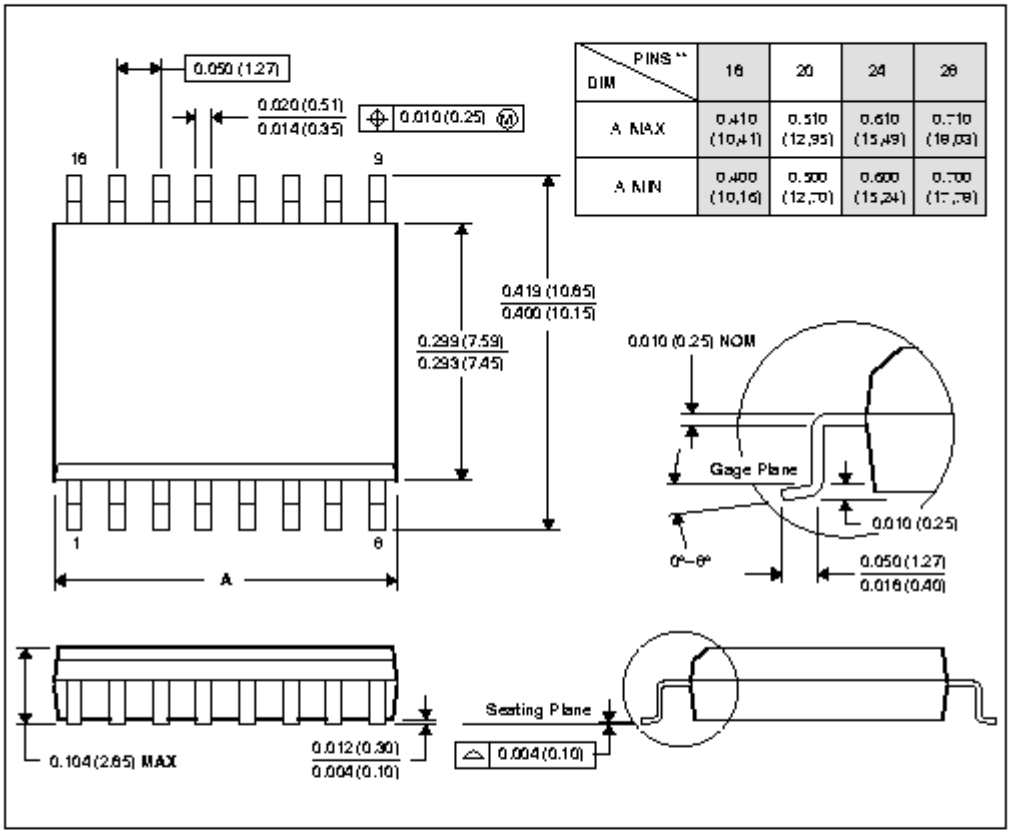
Figure 5. Configuration for Gain-Setting and Sidetone

higher clock frequencies and sample rates

The GM0936TQ is designed to work with sample rates up to 16kHz where the frequency of the frame sync determines the sampling frequency. However, there is a fundamental requirement to maintain the ratio of the master clock frequency, f_{CLK}, to the frame sync frequency, f_{FSR}/ f_{FSX}. This ratio for the GM0936TQ is 2.048 MHz/8 kHz, or 256 master clocks per frame sync. For example, to operate the GM0936TQ at a sampling rate of f_{FSR} and f_{FSX} equal to 16 kHz, f_{CLK} must be 256 times 16 kHz, or 4.096 MHz. If the GM0936TQ is operated above an 8-kHz sample rate, however, it is expected that the performance becomes somewhat degraded. Exact parameter specifications for rates up to 16-kHz sample rate are not specified at this time.

MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

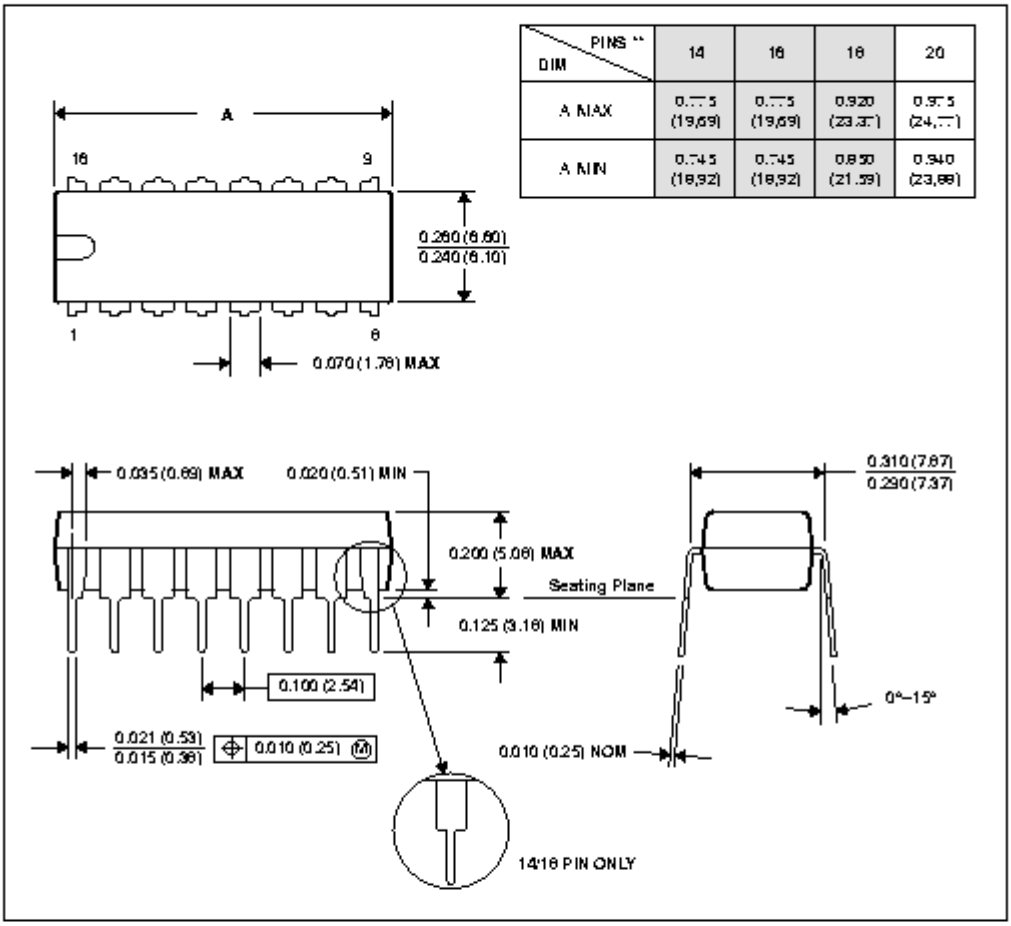


DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA

PLASTIC DUAL-IN-LINE PACKAGE

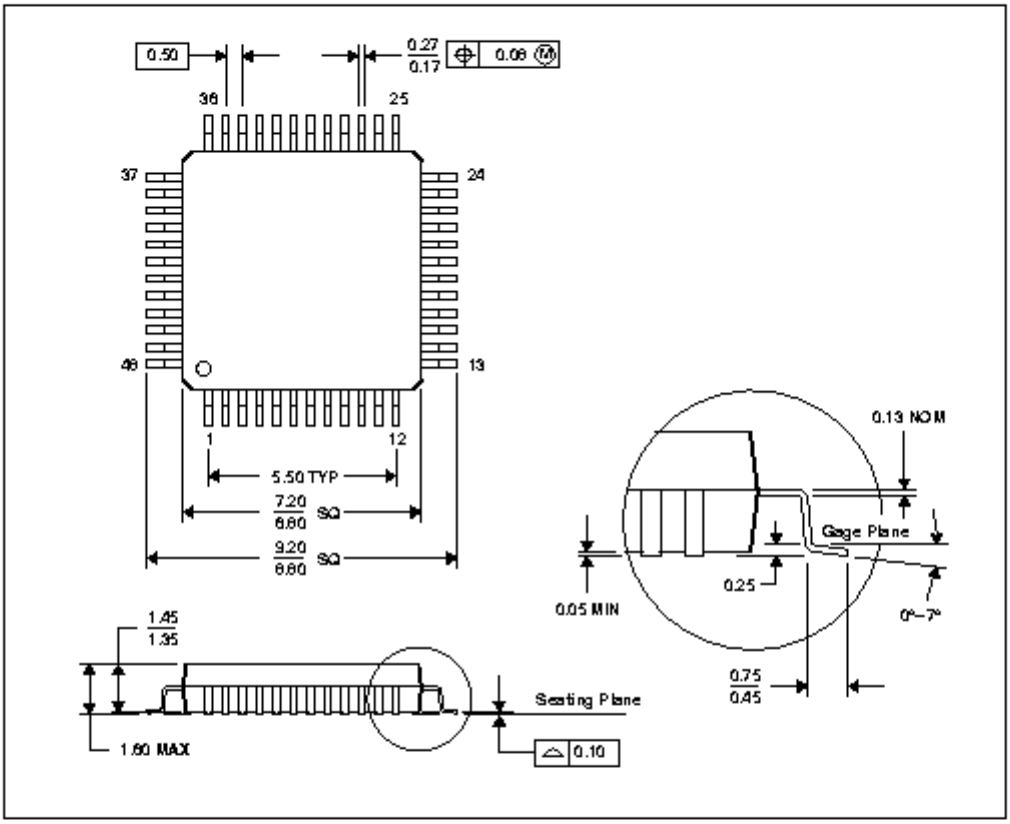


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

MECHANICAL DATA

PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136
D. This may also be a thermally-enhanced plastic package with leads connected to the die pads.