1.8V & 2.5V & 3.3V LVCMOS High-Performance Clock Buffer

FEATURES

- High-Performance 1:4 LVCMOS Clock Buffer
- Very Low Pin-to-Pin Skew < 50ps
- Very Low Additive Jitter < 50fs
- Very Low Propagation Delay < 3ns
- Synchronous Output Enable
- Supply Voltage: 3.3V or 2.5V or 1.8V
- f_{max} = 250MHz for 3.3V & 2.5V
- f_{max} = 200MHz for 1.8V
- Operating Temperature Range: -40°C to 105°C
- Available in 8-Pin TSSOP or DFN Packages

APPLICATIONS

- Factory Automation & Control
- Telecommunications Equipment
- Data Center & Enterprise Computing
- Grid Infrastructure
- Motor Drivers
- Medical Imaging
- Consumer Applications

GENERAL DESCRIPTION

The GM51104 is a modular, high-performance, low-skew, general-purpose clock buffer. High performing characteristics such as low additive jitter, low skew, and wide operation temperature range.

The GM51104 supports a synchronous output enable control (1G) which switches the outputs into a low state when 1G is low.

The GM51104 operates in a 1.8V & 2.5V & 3.3V, and are characterized for operation from -40°C to 105°C.

Device Information

PART NO.	PACKAGE	BODY SIZE
GM51104TSOG	TSSOP8	3.0mm x 4.4mm
GM51104DNG	DFN8	2.0mm x 2.0mm

FUNCTION BLOCK DIAGRAM

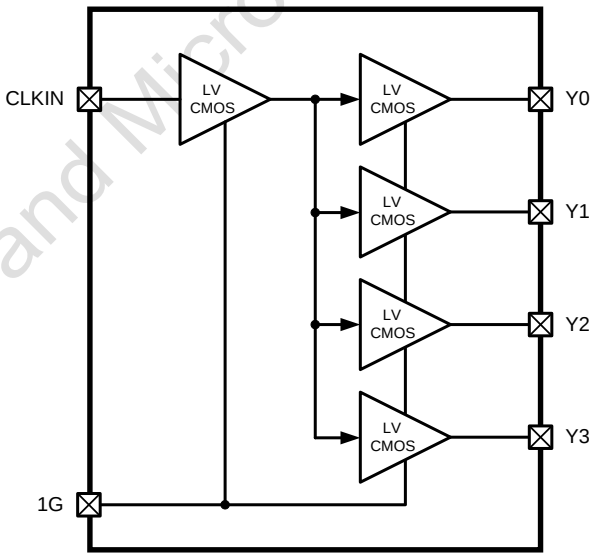


Figure 1, Function Block Diagram

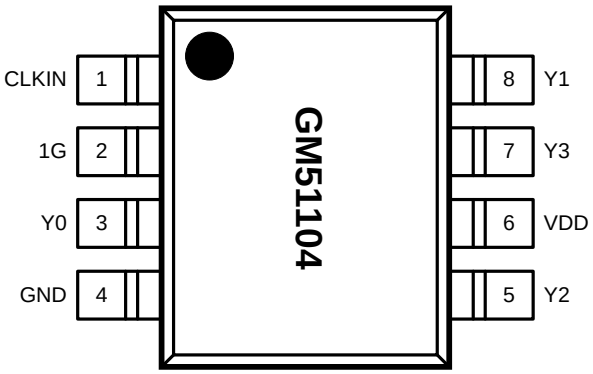
Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	CHANGE DATE	CHANGE ITEMS
V01	2024/06	Initial version completed.
V02	2024/06/24	ESD (Human Body Model) is changed from ±2500V to ±4000V.

PIN CONFIGURATIONS

TSSOP8



DFN8

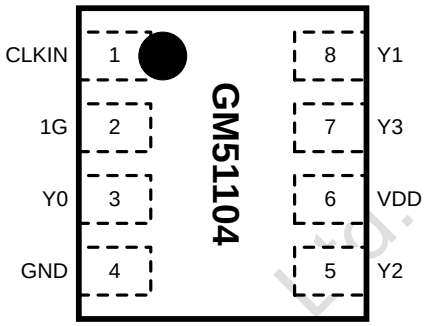


Figure 2, Pin Configurations (Top View)

PIN FUNCTION DESCRIPTIONS

PIN NO.	PIN NAME	TYPE	DESCRIPTIONS
1	CLKIN	Input	Single-Ended Clock Input. This pin has an internal pull-down resistor.
2	1G	Input	Output Enable Pin. This pin has an internal pull-down resistor. HIGH: Outputs Enabled; LOW: Outputs Disabled;
3	Y0	Output	LVCMOS Output. Unused outputs can be left floating.
4	GND	Ground	Power Supply Ground.
5	Y2	Output	LVCMOS Output. Unused outputs can be left floating.
6	VDD	Power	Power Supply.
7	Y3	Output	LVCMOS Output. Unused outputs can be left floating.
8	Y1	Output	LVCMOS Output. Unused outputs can be left floating.

ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3 to 3.6	V
Input Voltage (CLKIN)	V_{IN}	-0.3 to (V_{DD} + 0.3)	V
Output Enable and Output Voltage	V_O	-0.3 to (V_{DD} + 0.3)	V
Continuous Output Current	I_O	-50 to 50	mA
Storage Temperature Range	T_{STG}	-65 to 150	°C
Lead Temperature (solder 4s)	T_L	+260	°C
Maximum Junction Temperature	T_J	+125	°C
ESD (Human Body Model)	V_{ESD_HBM}	±4000	V
ESD (Charged Device Model)	V_{ESD_CDM}	±1000	V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Ambient Temperature	T_A	-40	25	105	°C
Supply Voltage (1.8V Supply)	V_{DD}	1.71	1.8	1.89	V
Supply Voltage (2.5V Supply)		2.375	2.5	2.625	
Supply Voltage (3.3V Supply)		3.135	3.3	3.465	
CLKIN Input Slew Rate		1		4	V/ns
LVCMOS Clock Input Frequency (2.5&3.3V Supply)	f_{CLK}	DC		250	MHz
LVCMOS Clock Input Frequency (1.8V Supply)		DC		200	

PACKAGE THERMAL RESISTANCE

PARAMETER	SYMBOL	RATINGS		UNIT
		TSSOP8	DFN8	
Thermal resistance from Junction to Ambient	θ_{JA}	181.9	163	°C/W
Thermal resistance from Junction to Case (top)	$\theta_{JC(top)}$	76.6	105.7	°C/W
Thermal resistance from Junction to Board	θ_{JB}	111.6	84.2	°C/W

DC ELECTRICAL CHARACTERISTICS

(V_{DD} =1.8V ± 5%, T_A = -40°C to +105°C, Typical Values at V_{DD} = 1.8V, T_A = 25°C, unless otherwise stated.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Operating Voltage		1.71	1.8	1.89	V
V_{IH}	Input High Voltage, CLKIN		0.7 x V_{DD}		V_{DD}	V
V_{IL}	Input Low Voltage, CLKIN				0.3 x V_{DD}	V
V_{IH}	Input High Voltage, 1G		1.3		V_{DD}	V
V_{IL}	Input Low Voltage, 1G				0.4	V
V_{OH}	Output High Voltage	I_{OH} = -5mA	V_{DD} – 0.3V			V
V_{OL}	Output Low Voltage	I_{OL} = +5mA			0.3	V
R_{OUT}	Output Impedance			54		Ω
C_{IN}	Input Capacitance, CLKIN			5		pF
Operating Supply Current						
I_{DD}	Static Supply Current	1G = V_{DD}, CLKIN = 0V or V_{DD}.		13		µA
	Active Supply Current	1G = V_{DD}, All-outputs Active, f_{CLK} = 100MHz, C_L = 5pF, T_A = 25°C		27		mA
I_{PD}	Power-Down Current	1G = 0V, CLKIN = 0V or V_{DD}.		13	50	µA

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.5V ± 5%, T_A = -40°C to +105°C, Typical Values at V_{DD} = 2.5V, T_A = 25°C, unless otherwise stated.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Operating Voltage		2.375	2.5	2.625	V
V_{IH}	Input High Voltage, CLKIN		0.7 x V_{DD}		V_{DD}	V
V_{IL}	Input Low Voltage, CLKIN				0.3 x V_{DD}	V
V_{IH}	Input High Voltage, 1G		1.3		V_{DD}	V
V_{IL}	Input Low Voltage, 1G				0.4	V
V_{OH}	Output High Voltage	I_{OH} = -8mA	V_{DD} – 0.5V			V
V_{OL}	Output Low Voltage	I_{OL} = +8mA			0.5	V
R_{OUT}	Output Impedance			52		Ω
C_{IN}	Input Capacitance, CLKIN			5		pF
Operating Supply Current						
I_{DD}	Static Supply Current	1G = V_{DD}, CLKIN = 0V or V_{DD}.		18		µA
	Active Supply Current	1G = V_{DD}, All-outputs Active, f_{CLK} = 100MHz, C_L = 5pF, T_A = 25°C		27		mA
I_{PD}	Power-Down Current	1G = 0V, CLKIN = 0V or V_{DD}.		18		µA

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V ± 5%, T_A = -40°C to +105°C, Typical Values at V_{DD} = 3.3V, T_A = 25°C, unless otherwise stated.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Operating Voltage		3.135	3.3	3.465	V
V_{IH}	Input High Voltage, CLKIN		0.7 x V_{DD}		V_{DD}	V
V_{IL}	Input Low Voltage, CLKIN				0.3 x V_{DD}	V
V_{IH}	Input High Voltage, 1G		1.6		V_{DD}	V
V_{IL}	Input Low Voltage, 1G				0.4	V
V_{OH}	Output High Voltage	I_{OH} = -12mA	V_{DD} – 0.7V			V
V_{OL}	Output Low Voltage	I_{OL} = +12mA			0.7	V
R_{OUT}	Output Impedance			50		Ω
C_{IN}	Input Capacitance, CLKIN			5		pF
Operating Supply Current						
I_{DD}	Static Supply Current	1G = V_{DD}, CLKIN = 0V or V_{DD}.		24		µA
	Active Supply Current	1G = V_{DD}, All-outputs Active, f_{CLK} = 100MHz, C_L = 5pF, T_A = 25°C		45		mA
I_{PD}	Power-Down Current	1G = 0V, CLKIN = 0V or V_{DD}.		24		µA

AC ELECTRICAL CHARACTERISTICS(1)

(V_{DD} = 1.8V ± 5%, T_A = -40°C to +105°C, Typical Values at V_{DD} = 1.8V, T_A = 25°C, unless otherwise stated.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLK}	Input Frequency(4)		0		200	MHz
t_{PD}	Propagation Delay, CLKIN to Yn(2)	C_L = 5pF		2.5		ns
t_{skew}	Output Skew(2)	Measured between Outputs Referenced to Y0		25	50	ps
t_r / t_f	Rise and Fall Time	20/80%(VOH - VOL) , C_L = 5pF	0.3		0.9	ns
t_j	RMS Additive Phase Jitter	f_{CLK} = 156.25MHz, BW = 12KHz to 20MHz		25		fs
O_{DC}	Output Duty Cycle	50% Input Duty Cycle, f_{CLK} = 100MHz	45		55	%
t_{EN}	Output Enable Time	1G to Yn, See Figure 3			6	cycles
t_{DIS}	Output Disable Time	1G to Yn, See Figure 3			5	cycles

AC ELECTRICAL CHARACTERISTICS(1)

(V_{DD} = 2.5V ± 5%, T_A = -40°C to +105°C, Typical Values at V_{DD} = 2.5V, T_A = 25°C, unless otherwise stated.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLK}	Input Frequency(4)		0		250	MHz
t_{PD}	Propagation Delay, CLKIN to Yn(2)	C_L = 5pF		2.5		ns
t_{skew}	Output Skew(2)	Measured between Outputs Referenced to Y0		25	50	ps
t_r / t_f	Rise and Fall Time	20/80%(VOH - VOL) , C_L = 5pF	0.3		0.9	ns
t_j	RMS Additive Phase Jitter	f_{CLK} = 156.25MHz, BW = 12KHz to 20MHz		22		fs
O_{DC}	Output Duty Cycle	50% Input Duty Cycle, f_{CLK} = 100MHz	45		55	%
t_{EN}	Output Enable Time	1G to Yn, See Figure 3			6	cycles
t_{DIS}	Output Disable Time	1G to Yn, See Figure 3			5	cycles

AC ELECTRICAL CHARACTERISTICS(1)

(V_{DD} = 3.3V ± 5%, T_A = -40°C to +105°C, Typical Values at V_{DD} = 3.3V, T_A = 25°C, unless otherwise stated.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLK}	Input Frequency(4)		0		250	MHz
t_{PD}	Propagation Delay, CLKIN to Yn(2)	C_L = 5pF		2.5		ns
t_{skew}	Output Skew(2)	Measured between Outputs Referenced to Y0		25	50	ps
t_r / t_f	Rise and Fall Time	20/80%(VOH - VOL) , C_L = 5pF	0.3		0.9	ns
t_j	RMS Additive Phase Jitter	f_{CLK} = 156.25MHz, BW = 12KHz to 20MHz		18		fs
O_{DC}	Output Duty Cycle	50% Input Duty Cycle, f_{CLK} = 100MHz	45		55	%
t_{EN}	Output Enable Time	1G to Yn, See Figure 3			6	cycles
t_{DIS}	Output Disable Time	1G to Yn, See Figure 3			5	cycles

1) *AC Parameters for CMOS are dependent upon output capacitive loading.*
2) *Parameter is specified by design, not tested in production.*
3) *Part-to-part skew is calculated as the difference between the fastest and slowest t_{PD} across multiple devices.*
4) *Specified by characterization.*

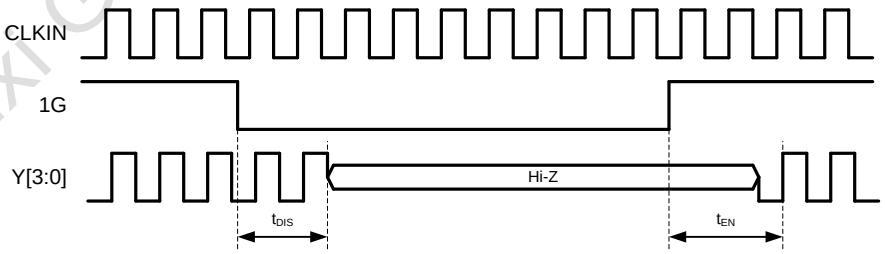


Figure 3, Output Timing Diagram

TYPICAL CHARACTERISTICS

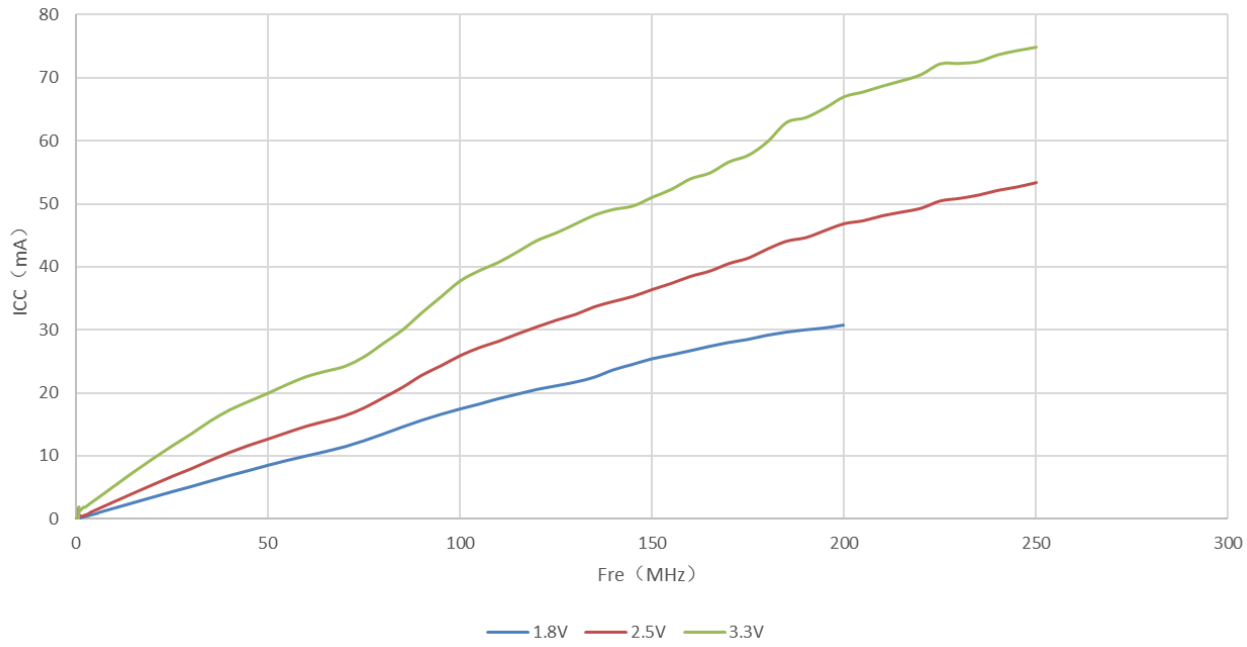


Figure 4, Device Power Consumption vs. Clock Frequency (C_L = 5pF) of GM51104 @25℃

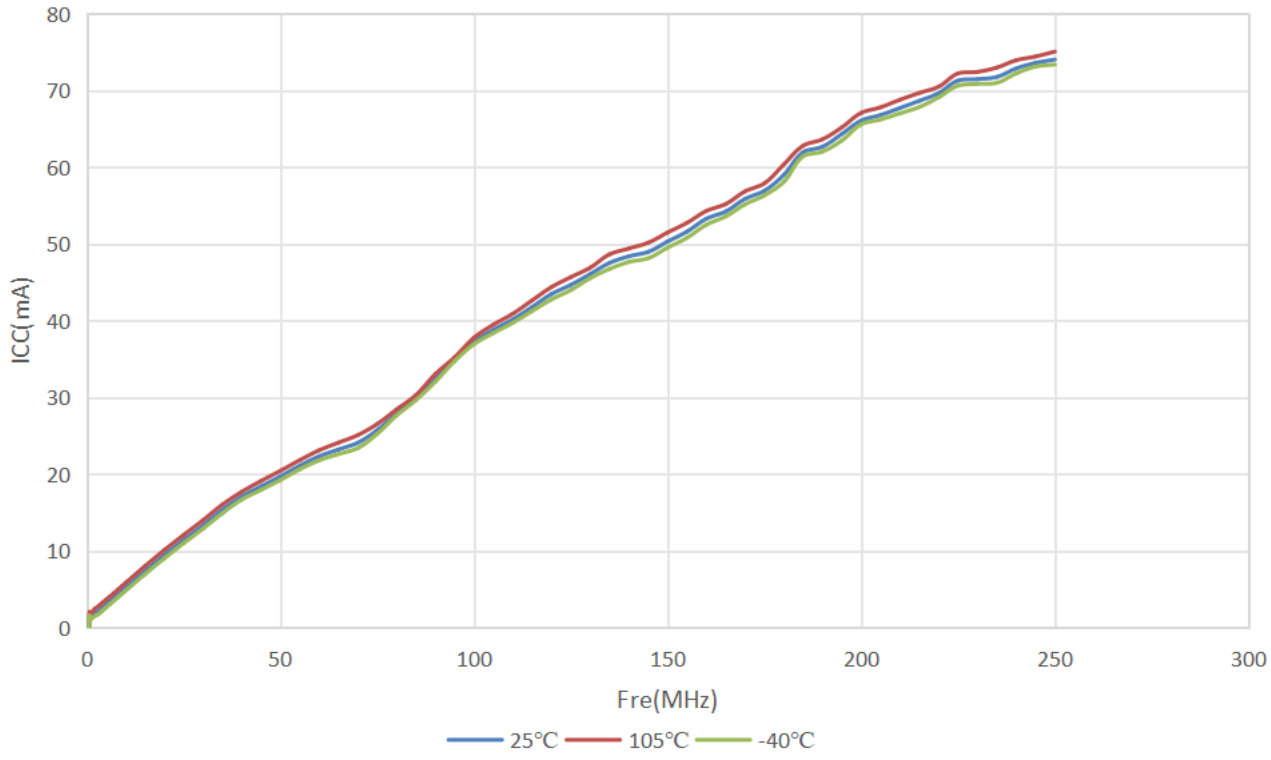


Figure 5, Device Power Consumption vs. Clock Frequency (C_L = 5pF) of GM51104 @VDD=3.3V

Additive Phase Jitter

The additive phase jitter for this device was measured using a CRYSTEK CVHD-950X_100MHz as an input source and Keysight E5052B phase noise analyzer at room temperature.

- With an integration range of 12kHz to 20MHz (VDD is 1.8V), the reference input has about 55.62 fs of RMS phase jitter shown in figure 6, and the output of GM51104 has about 59.14 fs of RMS jitter shown in figure 7. This results in a low additive phase jitter is less than 20.1 fs.

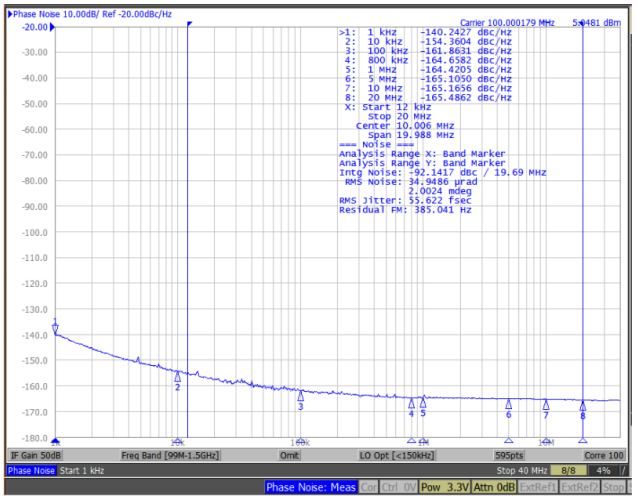


Figure 6, Reference Input Phase Noise @1.8V VDD
55.62-fs (12 kHz to 20 MHz)

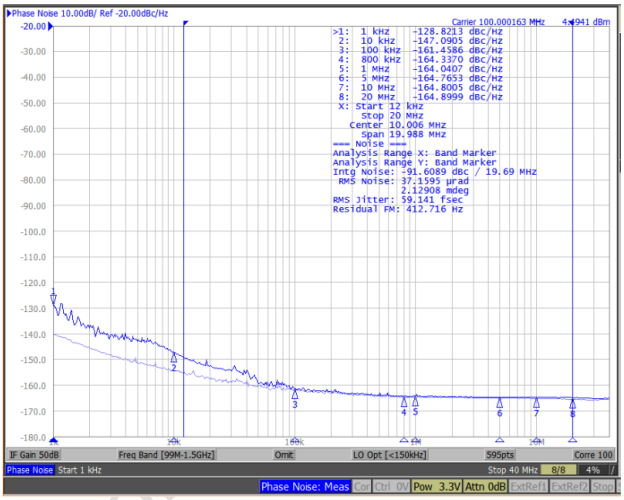


Figure 7, Input Phase Noise (Light Blue) and Output Phase Noise (Dark Blue) @1.8V VDD,
59.14-fs (12 kHz to 20 MHz)

- With an integration range of 12kHz to 20MHz (VDD is 2.5V), the reference input has about 51.75 fs of RMS phase jitter shown in figure 8, and the output of GM51104 has about 54.73fs of RMS jitter shown in figure 9. This results in a low additive phase jitter is less than 17.8 fs.

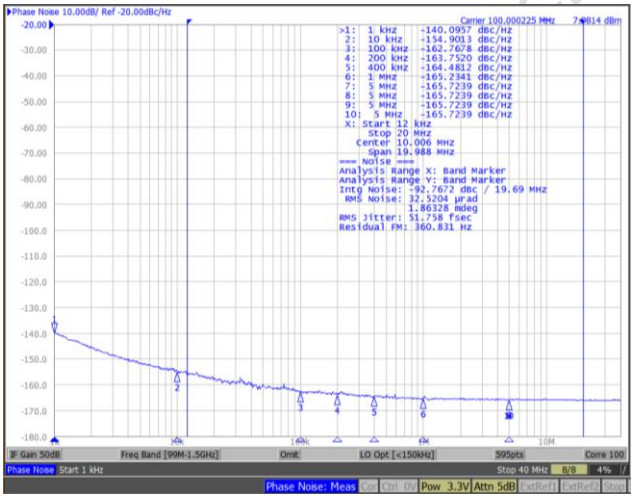


Figure 8, Reference Input Phase Noise @2.5V VDD
51.75-fs (12 kHz to 20 MHz)

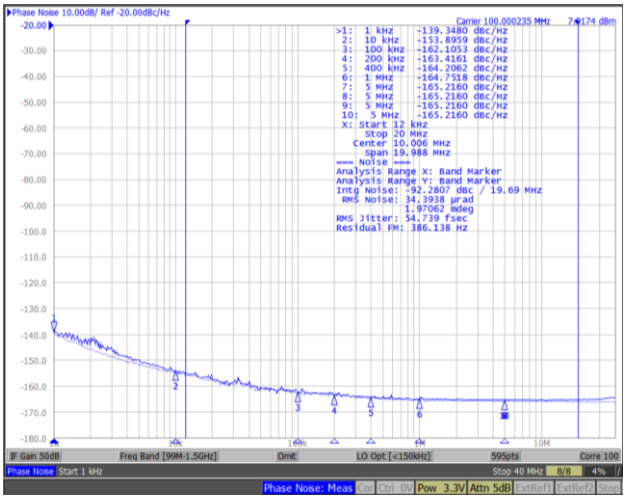


Figure 9, Input Phase Noise (Light Blue) and Output Phase Noise (Dark Blue) @2.5V VDD,
54.73-fs (12 kHz to 20 MHz)

- With an integration range of 12kHz to 20MHz (VDD is 3.3V), the reference input has about 52.55 fs of RMS phase jitter shown in figure 8, and the output of GM51104 has about 55.59fs of RMS jitter shown in figure 9. This results in a low additive phase jitter is less than 18.13 fs.

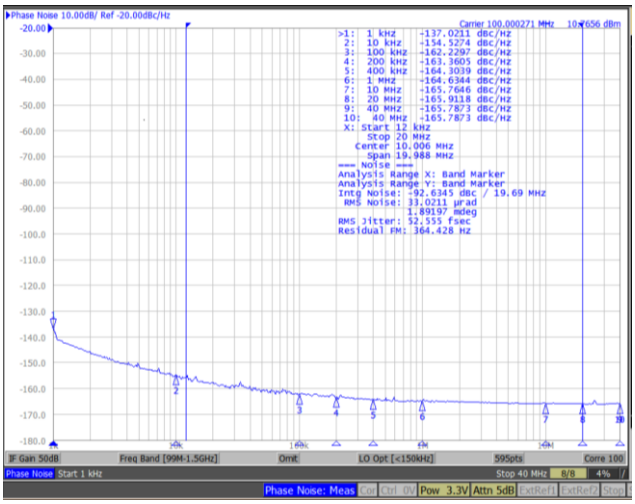


Figure 10, Reference Input Phase Noise @3.3V VDD
52.55-fs (12 kHz to 20 MHz)

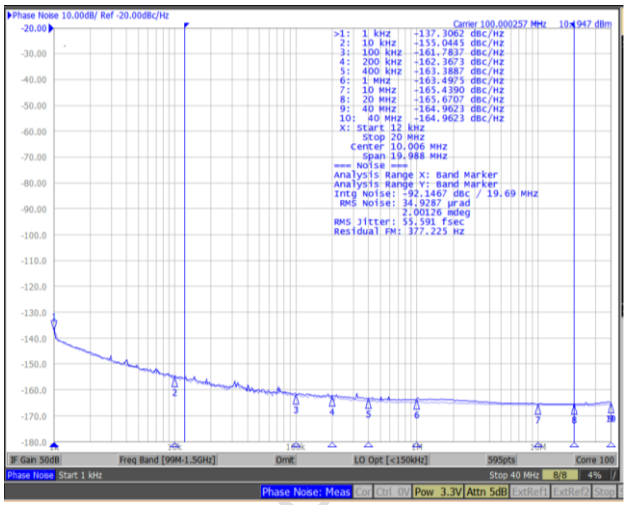


Figure 11, Input Phase Noise (Light Blue) and Output Phase Noise (Dark Blue) @3.3V VDD,
55.59-fs (12 kHz to 20 MHz)

FUNCTIONAL DESCRIPTION

■ Overview

The GM51104 is a low additive jitter LVCMOS buffer solution that can operate up to 250 MHz at V_{DD} = 3.3V & 2.5V and 200 MHz at V_{DD} = 1.8V. The outputs of the GM51104 can be disabled by driving the synchronous output enable pin (1G) low. Unused outputs can be left floating with a minimum copper length to minimize capacitance. In this way, this output will consume minimal output current because it has no load.

■ Output Enable Pin

When the output enable pin 1G is held High, the outputs are enabled. When it is held Low, the outputs are held in a Low state. The 1G pin is synchronized to the input clock to ensure that there are no runt pulses. When 1G is changed from Low to High, the outputs will initially have an impedance of about 400Ω to ground until the second falling edge of the input clock. Starting with the second falling edge of the input clock, the outputs will buffer the input. If the 1G pin is taken from Low to High when there is no input clock present, the outputs will either go High or Low and stay at that state; they will not oscillate. When the 1G pin is taken from High to Low, the outputs will become Low after the second falling edge of the clock input and then will go to a Disabled (Hi-Z) state starting after the next rising edge.

■ Device Function Modes

Table 1 shows the output logics of the GM51104.

Inputs		Outputs
CLKIN	1G	Yn
X	L	L
L	H	L
H	H	H

Table 1, Output Logic Table

APPLICATION INFORMATION

■ Typical Application

The GM51104 shown in Figure 12 is configured to fan out a 100MHz signal from a local LVCMOS oscillator. The CPU is configured to control the output state through 1G. The configuration example is driving three LVCMOS receivers in a backplane application with the following properties:

- The CPU clock can accept a full swing DC-coupled LVCMOS signal. A series resistor is placed near the GM51104 to closely match the characteristic impedance of the trace to minimize reflections.
- The FPGA clock is similarly DC-coupled with an appropriate series resistor placed near the GM51104.
- The PLL in this example can accept a lower amplitude signal, so a Thevenin's equivalent termination is used. The PLL receiver features internal biasing, so AC-coupling can be used when common-mode voltage is mismatched.

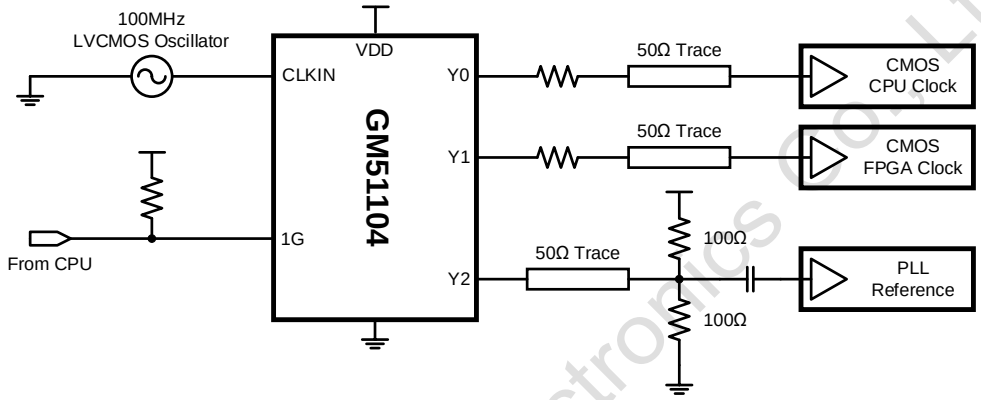


Figure 12, Typical Application Diagram

■ Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when the jitter and phase noise is critical to applications. Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guards the power supply system against induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power-supply terminals and laid out with short loops to minimize inductance. It is recommended to add as many high-frequency (for example, 0.1μF) bypass capacitors, as there are supply terminals in the package. It is recommended, but does not require, to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock buffer; these beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low DC resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

Figure 13 shows this recommended power supply decoupling method.

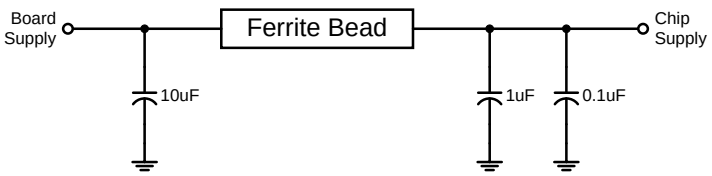
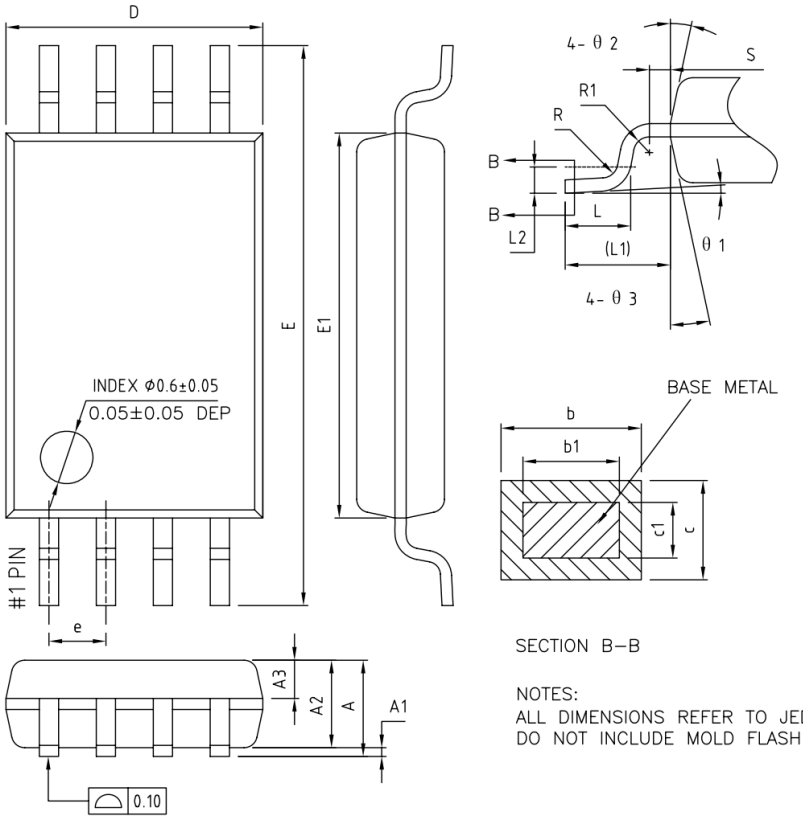


Figure 13, Power Supply Decoupling

PACKAGE OUTLINE (TSSOP8)

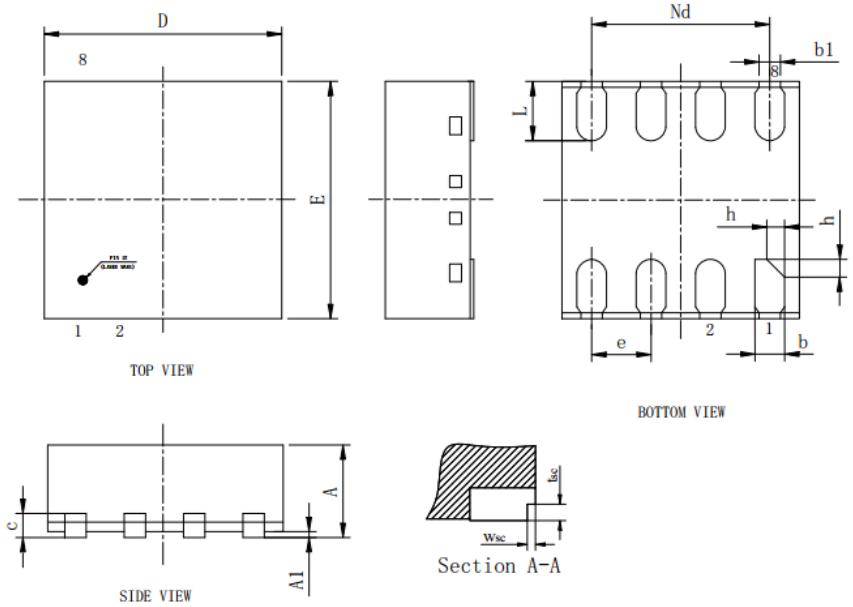


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	2.83	2.93	3.03
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ 1	0°	–	8°
θ 2	10°	12°	14°
θ 3	10°	12°	14°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO–153
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

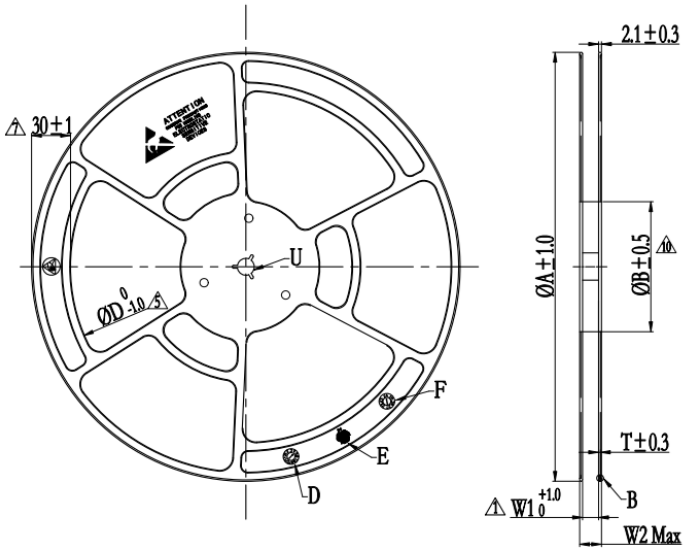
PACKAGE OUTLINE (DFN8-2x2)

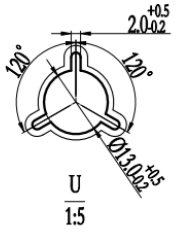


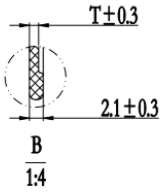
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.18	0.25	0.30
b1	0.18REF		
c	0.203REF		
D	1.90	2.00	2.10
e	0.50BSC		
Nd	1.50BSC		
E	1.90	2.00	2.10
L	0.45	0.50	0.55
h	0.10	0.15	0.20
Wsc	0.01	-	0.09
tsc	0.08	-	0.18

TAPE AND REEL INFORMATION OF GM51104TSOG

REEL (13 Inch)

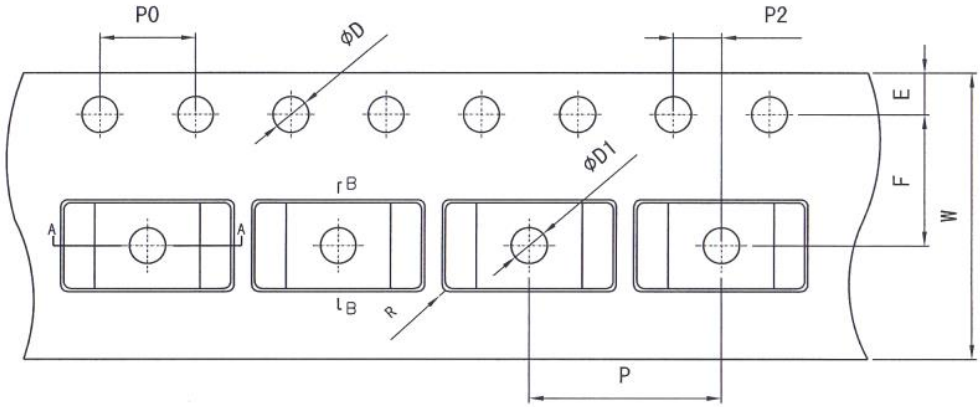


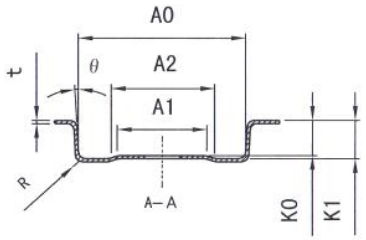




型号规格⚠	匹配的载带宽度	基本尺寸 (mm)					
		A	B	W1	W2Max	T	D
13″ -12×100	12/12.2	330	100	12.4	18.4	⚠4	⚠5
13″ -16×100	16			16.4	22.4	1.5	270
13″ -24×100	24			24.4	30.4		

TAPE (Pin 1 orientation in tape locates at upper left)





共同尺寸

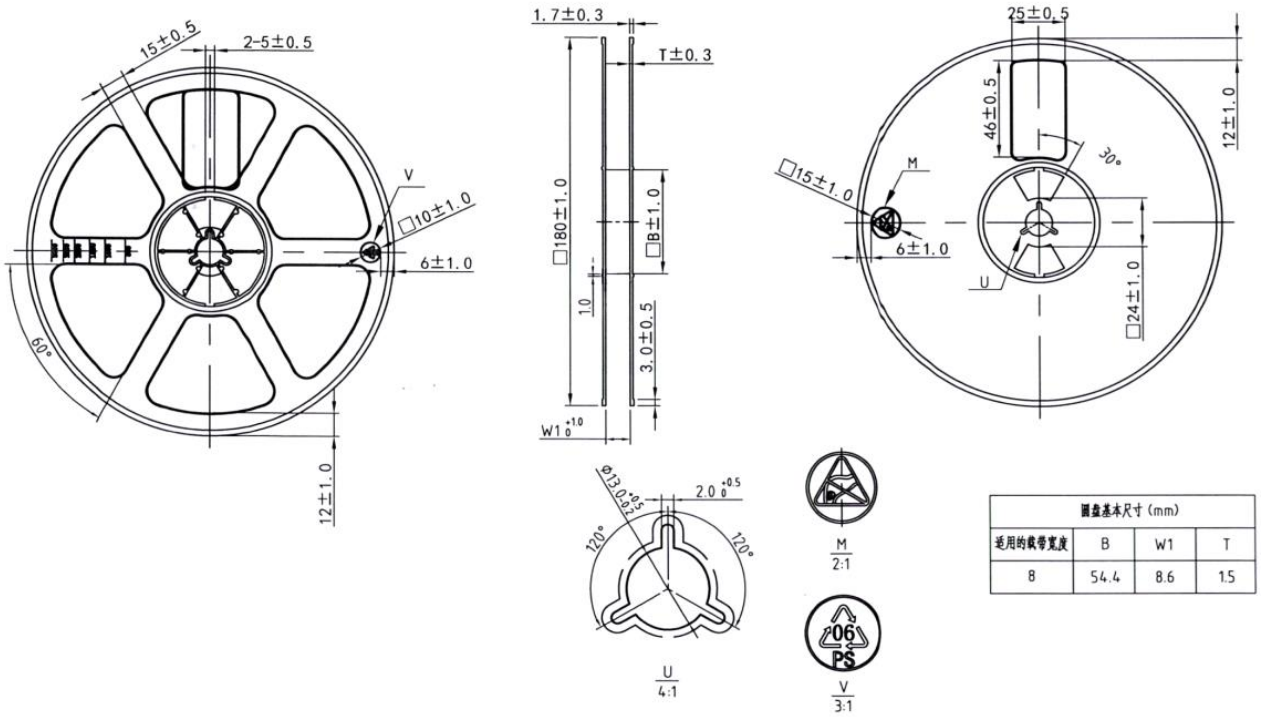
外观	尺寸(mm)
E	1.75±0.1
F	5.5±0.05
P2	2.0±0.05
D	$1.5^{+0.1}_{0}$
D1	$1.5^{+0.1}_{0}$
P0	4.0±0.1
R	0.5TYP
10P0	40.0±0.20

口袋尺寸

W	12.0±0.1	
P	8.0±0.1	
A0	6.9±0.1	⚠
B0	3.4±0.1	⚠
K0	1.2±0.1	
t	0.3±0.05	
K1	1.6±0.1	
A1	3.8±0.1	⚠⚠
A2	4.4±0.1	⚠
θ	3° TYP	

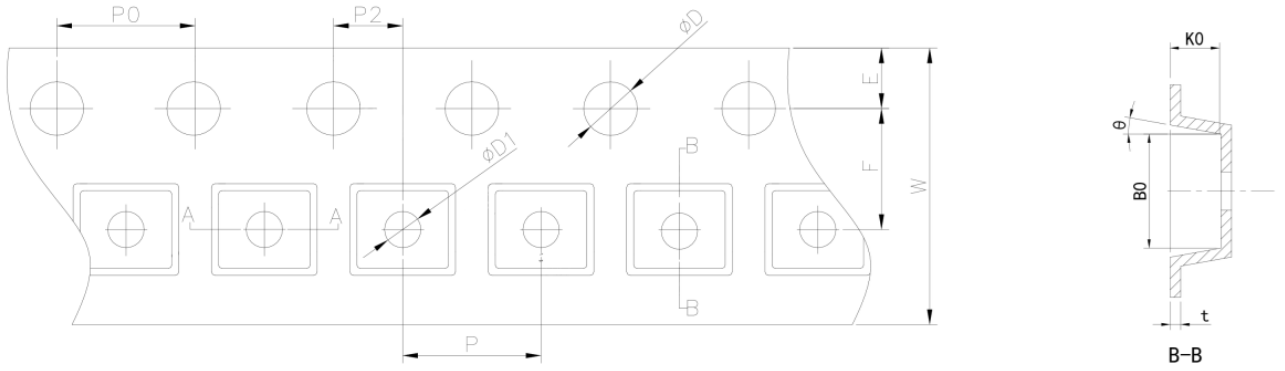
TAPE AND REEL INFORMATION OF GM51104DNG

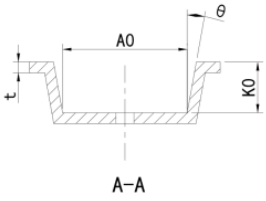
REEL (7 Inch)



圆盘基本尺寸 (mm)			
适用的载带宽度	B	W1	T
8	54.4	8.6	1.5

TAPE (Pin 1 orientation in tape locates at upper right)





共同尺寸

外 观	尺 寸(mm)
E	1.75±0.10
F	3.50±0.05
P2	2.00±0.05
D	1.50±0.10
D1	1.00 +0.25 0
P0	4.00±0.10
10P0	40.00±0.20

口袋尺寸

外 观	尺 寸(mm)	
W	8.00 +0.3 -0.1	
P	4.00±0.10	
A0	2.15±0.03	1
B0	2.15±0.03	1
K0	0.88±0.05	
t	0.254±0.02	
θ	5° MAX	

产品订购信息

器件编号	产品丝印	工作温度范围	封装信息	湿敏等级	环保信息	包装方法
GM51104TSOG	51104 XXXXX(1) YYWW(2)Z(3)	-40°C 至 +105°C	TSSOP8	MSL-3	RoHS & Green	卷带和卷盘 (每卷 5000 只)
GM51104DNG	51104D XXXXXX(1) YYWW(2)ZZ(3)	-40°C 至 +105°C	DFN8-2x2	MSL-3	RoHS & Green	卷带和卷盘 (每卷 3000 只)

注：(1) XXXXX 和 XXXXXX 表示批次号。 (2) YY 表示年号，WW 表示周号。(3) Z 和 ZZ 表示生产信息。