GM5351A

I²C Programmable Any-Frequency CMOS Clock Generator

Features

- Generates up to 3 non-integer-related frequencies from 2.5KHz to 250MHz
- I²C user definable configuration
- Exact frequency synthesis at each output (0 ppm error)
- Optional clock input (CLKIN)
- Low output period jitter: <70pS (typ.)
- Configurable spread spectrum selectable at each output
- Operates from a low-cost, fixed frequency crystal: 25 or 27MHz
- Supports static phase offset
- Programmable rise/fall time control
- Glitchless frequency changes
- Separate voltage supply pins provide level translation:
  - Core VDD: 2.5 or 3.3V
  - Output VDDO: 1.8, 2.5 or 3.3V
- Excellent PSRR eliminates external power supply filtering
- Very low power consumption
- Adjustable output delay
- Package type: MSOP10 or TDFN10
- PCIE Gen 1 compatible
- Supports HCSL compatible swing

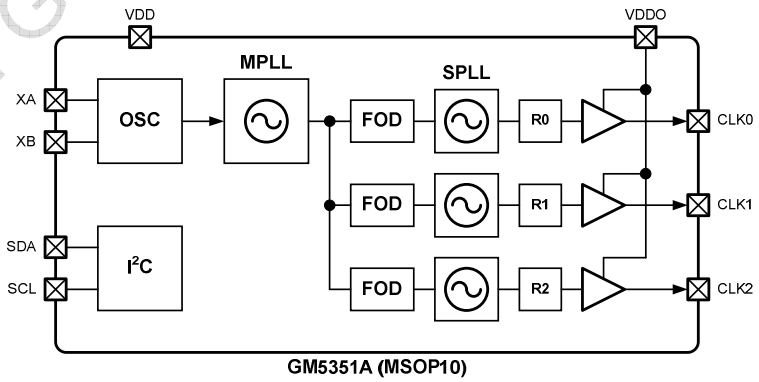
Applications

- HDTV, DVD/Blue-ray, Set-top box
- Audio/video equipment, gaming
- Printers, scanners, projectors
- Handheld Instrumentation
- Residential gateways
- Networking/Communication
- Servers, Storage
- XO Replacement

General Description

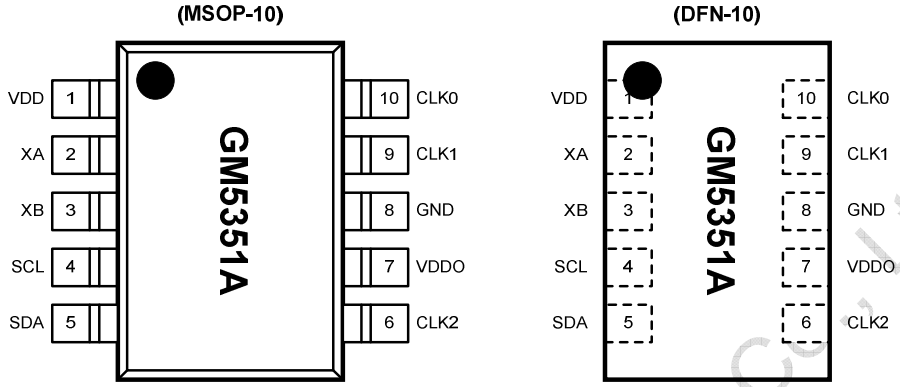
The GM5351A is an I2C configurable clock generator that is ideally suited for replacing crystals, crystal oscillators, phase-locked loops (PLLs), and fanout buffers in cost-sensitive applications. The GM5351A can generate any frequency up to 250MHz on each of its outputs with 0ppm error. The GM5351A generates up to 3 free-running clocks using an internal oscillator for replacing crystals and crystal oscillators.

Functional Block Diagram



GM5351A (MSOP10)

PIN DIAGRAM



PIN DIAGRAM (TOP VIEW)

PIN DESCRIPTION

Pin No.	Pin Name	Pin Type	Function
1	VDD	Power	Core voltage power supply pin.
2	XA	Input	Input pin for external crystal.
3	XB	Input	Input pin for external crystal.
4	SCL	Input	Serial clock input for the I2C bus. This pin must be pulled-up using a pull-up resistor of at least 1KΩ.
5	SDA	Input/Output	Serial data input for the I2C bus. This pin must be pulled-up using a pull-up resistor of at least 1KΩ.
6	CLK2	Output	Output clock 2.
7	VDDO	Power	Output voltage power supply pin for CLK0, CLK1 and CLK2.
8	GND	Ground	Ground.
9	CLK1	Output	Output clock 1.
10	CLK0	Output	Output clock 0.

ABSOLUTE MAXIMUM RATINGS

permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Test Conditions	Value	Unit
DC Supply Voltage	V_{DD_max}	VDD, VDDO	-0.3 to 3.8	V
Input Voltage	V_{IN_CLKIN}	SCL, SDA	-0.3 to 3.8	V
	$V_{IN\_XA/XB}$	XA, XB	-0.3 to 1.3V	V
Output Voltage	V_{OUT_CLK}	CLK0, CLK1, CLK2	-0.3 to V_{DDO}+0.3	V
ESD		--	±2.0	KV
Junction Temperature	T_J	--	-55 to 150	°C
Soldering Temperature	T_{PEAK}	--	260	°C
Soldering Temperature Time at T_{PEAK}	TP	--	20~40	S
Thermal Resistance Junction to Ambient of MSOP10	θ_{JA}	Still air	131	°C/W

RECOMMENDED OPERATING CONDITIONS

All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25°C unless otherwise noted. VDD and VDDO can be operated at independent voltages.
Power supply sequencing for VDD and VDDO requires that VDDO be powered up either before or at the same time as VDD.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Ambient Temperature	T_A	-40	25	85	°C
Core Supply Voltage	V_{DD}	3.0	3.3	3.6	V
		2.25	2.5	2.75	V
Output Buffer Voltage	V_{DDO}	1.71	1.8	1.89	V
		2.25	2.5	2.75	V
		3.0	3.3	3.6	V

DC CHARACTERISTICS

(VDD = 2.5V ± 10%, or 3.3V ± 10%， TA = -40 to 85°C)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Core Supply Current	I_{DD}	Enabled 3 outputs	--	22	35	mA
Output Buffer Supply Current(1)	I_{DDO}	C_L = 5pF	--	6.6	16.8	mA
Input Current	I_{IN}	SDA, SCL	--	--	10	µA
Output Impedance	Z_O	3.3V VDDO, default high driver	--	50	--	Ω

Note：

1) Output clocks less than or equal to 100MHz.

AC CHARACTERISTICS

(VDD = 2.5V ± 10%, or 3.3V ± 10%， TA = -40 to 85°C)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Power-up Time	T_{RDY}	From V_{DD} = V_{DDMIN} to valid output clock, C_L = 5pF, f_{CLKn} > 1MHz	--	2	10	mS
Power-up Time, PL Bypass Mode	T_{BYP}	From V_{DD} = V_{DDMIN} to valid output clock, C_L = 5pF, f_{CLKn} > 1MHz	--	0.5	1	mS
Output Frequency Transition Time	T_{FREQ}	f_{CLKn} > 1MHz	--	--	10	µS
Output Phase Offset	P_{STEP}	--	--	333	--	pS/step
Spread Spectrum Frequency Deviation	SS_{DEV}	Down spread. Selectable in 0.1% steps.	-0.1	--	-2.5	%
		Center spread. Selectable in 0.1% steps.	±0.1	--	±1.5	%
Spread Spectrum Modulation Rate	SS_{MOD}	--	30	31.5	33	KHz

INPUT CLOCK CHARACTERISTICS

(VDD = 2.5V ± 10%, or 3.3V ± 10%， TA = -40 to 85°C)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Crystal Frequency	f_{XTAL}	--	10	27	40	MHz

OUTPUT CLOCK CHARACTERISTICS

(VDD = 2.5V ± 10%, or 3.3V ± 10%， TA = -40 to 85°C)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Frequency Range(1)	F_{CLK}	--	0.0025	--	250	MHz
Load Capacitance	C_L	--	--	--	15	pF
Duty Cycle	DC	$F_{CLK} \le 160MHz$, measured at $V_{DD}/2$	45	50	55	%
		$F_{CLK} > 160MHz$, measured at $V_{DD}/2$	40	50	60	%
Rise/Fall Time	t_r	20%~80%, C_L = 5pF, Default high drive strength	--	1	1.5	nS
	t_f		--	1	1.5	nS
Output High Voltage	V_{OH}	C_L = 5pF	V_{DD} -0.6	--	--	V
Output Low Voltage	V_{OL}				0.6	V
Period Jitter(2,3)	J_{PER}	3 outputs running	--	70	155	pS, pk-pk
Cycle-to-Cycle Jitter(2,3)	J_{CC}	3 outputs running	--	70	150	pS, pk-pk

Note:

1) Only two unique frequencies above 112.5MHz can be simultaneously output.
2) Measured over 10K cycles. Jitter is only specified at the default high drive strength (50Ω output impedance).
3) Jitter is highly dependent on device frequency configuration. Specifications represent a “worst case, real world” frequency plan; actual performance may be substantially better. Three-output 10 MSOP package measured with clock outputs of 74.25, 24.576 and 48MHz.

CRYSTAL REQUIREMENTS(1)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Crystal Frequency	f_{XTAL}	--	10	27	40	MHz
Load Capacitance	C_L	--	6	--	12	pF
Equivalent Series Resistance	r_{ESR}	--	--	--	150	Ω
Crystal Max Drive Level	d_L	--	100	--	--	μW

Note：

1) Crystals which require load capacitances of 6, 8, or 10pF should use the device's internal load capacitance for optimum performance. See register 183 bits 7:6. A crystal with a 12pF load capacitance requirement should use a combination of the internal 10pF load capacitance in addition to external 2pF load capacitance (e.g., by using 4pF capacitors on XA and XB).

I²C SPECIFICATIONS (SCL, SDA)

Parameter	Symbol	Test Conditions	Standard Mode 100Ksps		Fast Mode 400Ksps		Unit
			Min	Max	Min	Max	
Low Level Input Voltage	V_{ILI2C}	--	-0.3	0.3x V_{DDI2C}	-0.3	0.3x V_{DDI2C}	V
High Level Input Voltage	V_{IHI2C}	--	0.7x V_{DDI2C}	3.6	0.7x V_{DDI2C}	3.6	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	--	--	--	0.1	--	V
Low Level Output Voltage (open drain or open collector) at 3mA sink current	V_{OLI2C}[1]	V_{DDI2C}[1]=2.5/ 3.3V	0	0.4	0	0.4	V
Input Current	I_{II2C}	--	-10	10	-10	10	μA
Capacitance for Each I/O Pin	C_{II2C}	V_{IN} = -0.1 to V_{DDI2C}	--	4	--	4	pF
I²C Bus Timeout	T_{TO}	Timeout Enabled	25	35	25	35	mS

Note：

1) Only I²C pull-up voltage (V_{DDI2C}) of 2.25 to 3.6V are supported.

1. FUNCTIONAL DESCRIPTION

The GM5351A is a versatile I²C programmable clock generator that is ideally suited for replacing crystals, crystal oscillators. A block diagram showing the general architecture of the GM5351A is shown in Figure 1. The device consists of an input stage, two synthesis stages, and an output stage.

The input stage accepts an external crystal (XTAL) or a clock input (CLKIN). The first stage of synthesis is an integer-N PLL (MPLL) which multiplies the input frequencies to a high-frequency intermediate clock1. The second stage uses fractional dividers (FOD) to generate low-frequency intermediate clock2, then an integer PLL (SPLL) is followed to decrease clock jitter. The output of SPLL is integer multiple of desired output frequency. Additional integer division is provided at the output stage for generating output frequencies as low as 2.5 kHz. Crosspoint switches at each of the synthesis stages allows total flexibility in routing any of the inputs to any of the outputs.

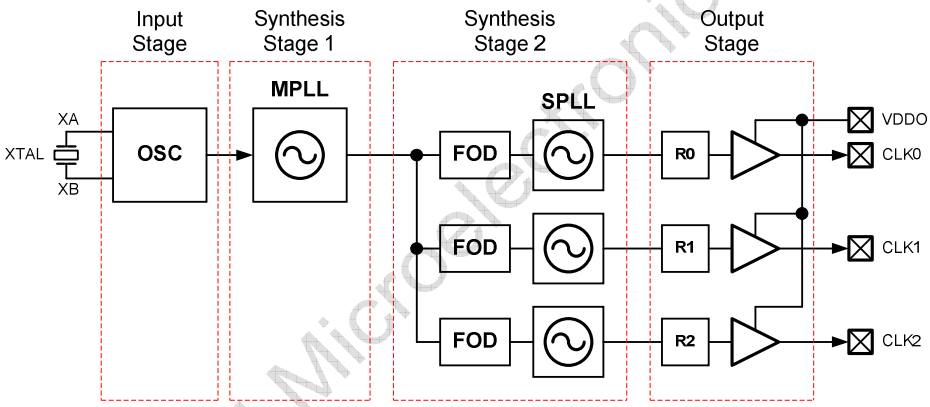


Figure 1, GM5351A Block Diagram

1.1 Input Stage

1.1.1 Crystal Inputs (XA, XB)

The GM5351A uses a fixed-frequency standard AT-cut crystal as a reference to the internal oscillator. The output of the oscillator can be used to provide a free-running reference to the MPLL for generating asynchronous clocks. The output frequency of the oscillator will operate at the crystal frequency, from 10MHz to 40MHz.

Internal load capacitors are provided to eliminate the need for external components when connecting a crystal to the GM5351A. The total internal XTAL load capacitance (C_L) can be selected to be 0, 6, 8, or 10pF. Crystals with alternate load capacitance requirements are supported using additional external load capacitance ≤ 2pF (e.g., by using ≤ 4pF capacitors on XA and XB) as shown in Figure 2.

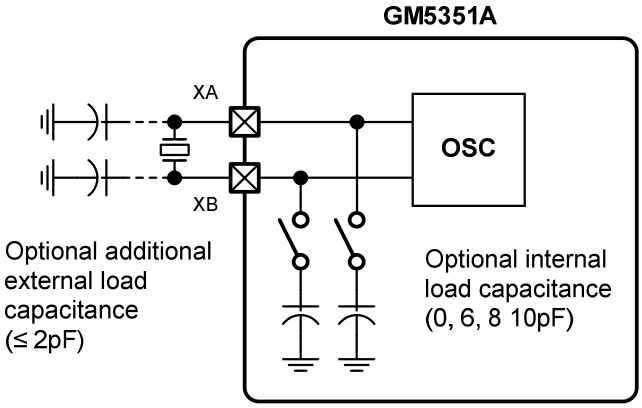


Figure 2, External Crystal with optional load capacitors

1.1.2 External Clock Input

The GM5351A can be driven with a clock signal through the XA input pin. This is especially useful when in need of generating clock outputs in two synchronization domains. With the GM5351A, one reference clock can be provided at XA as shown in figure 3. The external clock input from 10 to 40MHz is used as a clock reference for the MPLL when generating synchronous clock outputs.

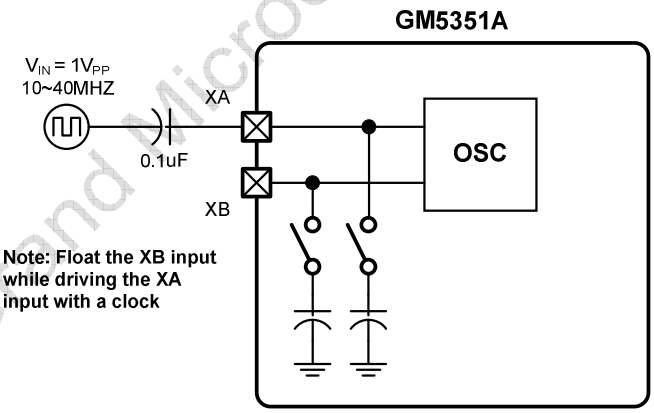


Figure 3, GM5351A driven by a clock signal

1.2 Synthesis Stage

1.3 Output Stage

An additional level of division (R) is available at the output stage for generating clocks as low as 2.5 kHz. All output drivers generate CMOS level outputs with separate output voltage supply pins (VDDO) allowing a different voltage signal level (1.8, 2.5, or 3.3 V).

1.4 Spread Spectrum

Spread spectrum can be enabled on any of the clock outputs that use MPLL as its reference. Spread spectrum is useful for reducing electromagnetic interference (EMI). Enabling spread spectrum on an output clock modulates its frequency, which effectively reduces the overall amplitude of its radiated energy.

The GM5351A supports several levels of spread spectrum allowing the designer to choose an ideal compromise between system performance and EMI compliance.

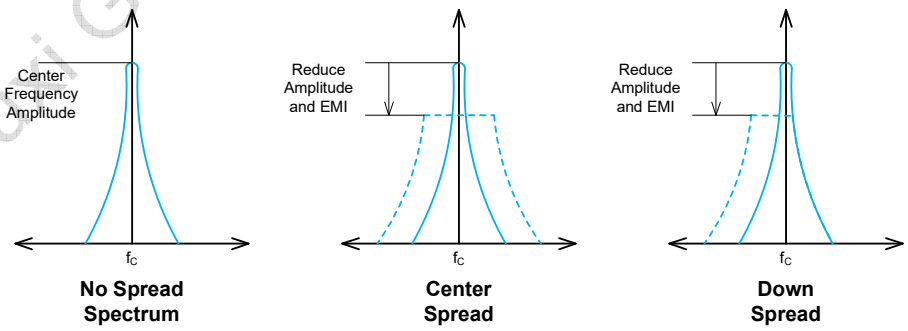


Figure X, Available Spread Spectrum Profiles

2. I²C INTERFACE

Many of the functions and features of the GM5351A are controlled by reading and writing to the RAM space using the I²C interface. The following is a list of the common features that are controllable through the I²C interface. For a complete listing of available I²C registers and programming steps, please see “AN5351-1: Manually Generating an GM5351A Register Map.”

Read Status Indicators:
- Crystal Reference Loss of signal, LOS_XTAL, reg0[3]
- MPLL and/or SPLL Loss of lock, LOL_M or LOL_S, reg0[6:5]

- Configuration of multiplication and divider values for the PLLs, dividers
- Configuration of the Spread Spectrum profile (down or center spread, modulation percentage)
- Control of the cross point switch selection for each of the PLLs and dividers
- Set output clock options
  - Enable/disable for each clock output
  - Invert/non-invert for each clock output
  - Output divider values (2n, n=1...7)
  - Output state when disabled (stop Hi, stop Low, Hi-Z)
  - Output phase offset

The I²C interface operates in slave mode with 7-bit addressing and can operate in Standard-Mode (100 kbps) or Fast-Mode (400 kbps) and supports burst data transfer with auto address increments.

The I²C bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL) as shown in Figure 7. Both the SDA and SCL pins must be connected to the VDD supply via an external pull-up as recommended by the I²C specification.

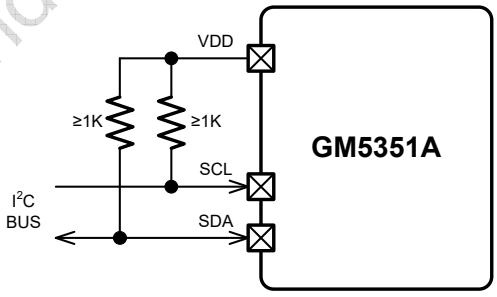


Figure 7, I²C Interface

The 7-bit device (slave) address of the GM5351A consist of a 6-bit fixed address plus a user selectable LSB bit as shown in Figure 8. The LSB bit is selectable as 0 or 1 using the optional A0 pin which is useful for applications that require more than one GM5351A on a single I²C bus.

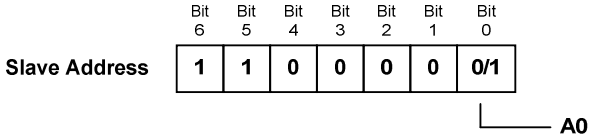


Figure 8, GM5351A I²C Slave Address

2.1 Write Data Access

In write data access, there are some bytes transmitted from master to slave as following:

slave address byte: slv_addr[6:0], r/wn;
register index byte: reg_index[7:0];
write data bytes: write data.

slv_addr[6:0] is the I²C address to select an I²C device.
r/wn is the read/write bit. If "1", selects read access; if "0", selects write access. Here for write data access, it is "0".
reg_index[7:0] is used to select register index.
write data are the data for write data access.

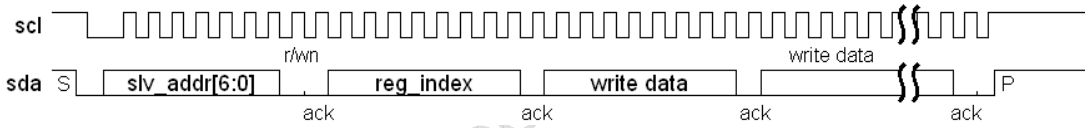


Figure 9, I²C Write Data Access

The above figure 9 shows the timing of writing data access. The first byte is slave_addr[6:0] to select one slave node; the next byte is reg_index to define the register index; the next bytes are some bytes data for write.

The first write address is reg_index. Once one byte data is written successful, the internal register address will be +1 automatically so that the next bytes data will be written in continuous address registers.

2.2 Read Data Access

For the read data access, there are two cases: one is with setting reg_index; the other is without setting reg_index.

In read data access with setting reg_index, there are some bytes transmitted as following:

slave address byte from master to slave: slv_addr[6:0], r/wn;
register index byte from master to slave: reg_index[7:0];
read data bytes from slave to master: read data.

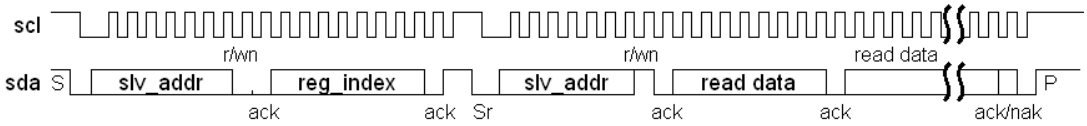


Figure 10，I²C Read Data Access with setting reg_index

The above figure 10 shows the read data access with setting reg_index. First is the slave address to select one slave device; then is reg_index to select the register index; then is repeated start; then is slave address again, next are some bytes read data from slave device.

For the first byte read-out data is from the register index set in this access; then the register address will be +1 automatically so that the next read out data are from the continuous address registers.

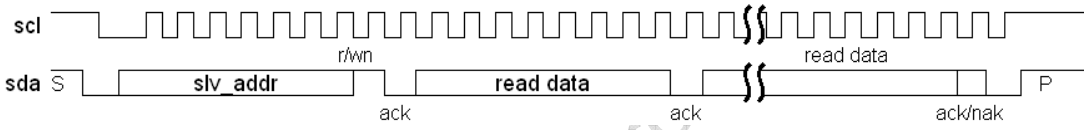


Figure 11, I²C Read Data Access without setting reg_index

The above figure 11 shows the read data access without setting reg_index. The first byte is the slave address to select one slave device; the next are some bytes read data from slave device.

For the first byte read-out data is from the latest register address which is updated by the last write data access or read data access. Once a byte data is successful read out, the register address will be +1 automatically so that the next read out data are from the continuous address registers.

2.3 I²C Timeout Detect

For the reliability consideration, if SDA line is kept low for more than 25ms, the I²C timeout is detected to reset I²C engine so that GM5351A will not to drive the SDA to low.

As long as SDA line is low, the I²C timeout will be detected no matter whether the I²C device address is matched or not.

3. CONFIGURING THE GM5351A

The GM5351A is a highly flexible clock generator which is entirely configurable through its I²C interface. The device's default configuration is stored in non-volatile memory (NVM) as shown in Figure 12. The NVM is a one time programmable memory (OTP) which can store a custom user configuration at power-up. This is a useful feature for applications that need a clock present at power-up (e.g., for providing a clock to a processor).

During a power cycle the contents of the NVM are copied into random access memory (RAM), which sets the device configuration that will be used during normal operation. Any changes to the device configuration after power-up are made by reading and writing to registers in the RAM space through the I²C interface.

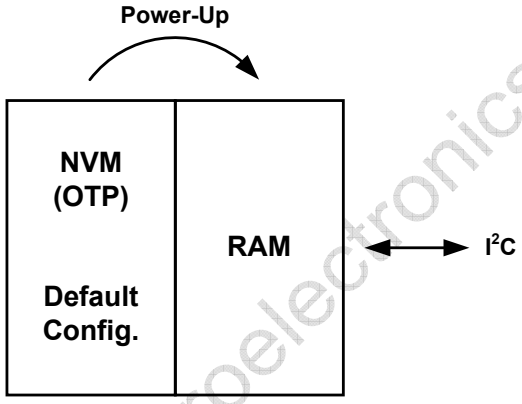


Figure 12, GM5351A Memory Configuration

3.1 Write a Custom Configuration to RAM

GM5351A can be programmed via I²C by following the steps shown in Figure 13.

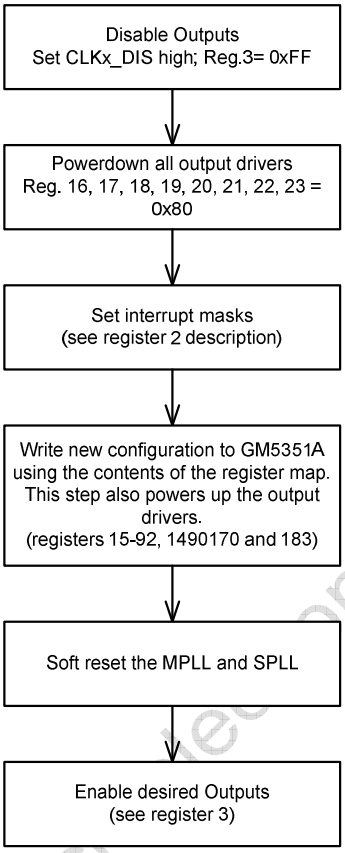


Figure 13, I^2C Programming procedure

4. TYPICAL APPLICATION

4.1 GM5351A replaces Multiple Clocks and XOs

The GM5351A is a user-definable custom clock generator that is ideally suited for replacing crystals and crystal oscillators in cost-sensitive applications. An example application is shown in figure 14.

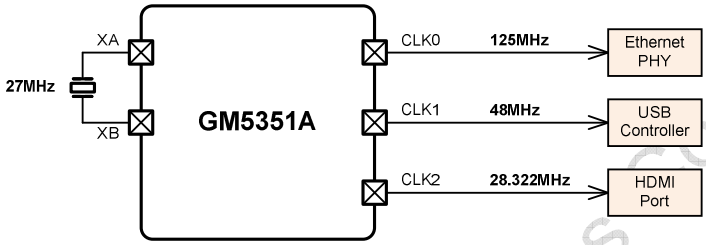


Figure 14, Using GM5351A to replace multiple crystals, crystal oscilators

4.2 HCSL Compatible Outputs

The GM5351A can be configured to support HCSL compatible swing when the VDDO of the output power supply is set to 2.5 V.

The circuit in the figure 15 below must be applied to each of the two clocks used, and one of the clocks in the pair must also be inverted to generate a differential pair. See register setting CLKx_INV.

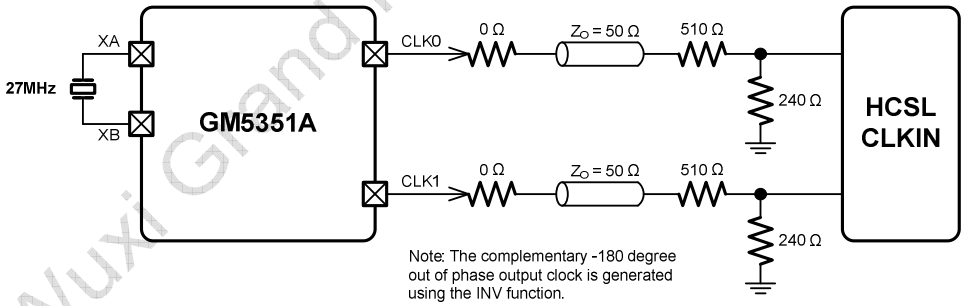


Figure 15, GM5351A Output is HSCL compatible

5. DESIGN CONSIDERATIONS

The GM5351A is a self-contained clock generator that requires very few external components. The following general guidelines are recommended to ensure optimum performance.

5.1 Power Supply Decoupling/Filtering

The GM5351A has built-in power supply filtering circuitry and extensive internal Low Drop Out (LDO) voltage regulators to help minimize the number of external bypass components. All that is recommended is one 0.1 to 1.0 μF decoupling capacitor per power supply pin. This capacitor should be mounted as close to the VDD and VDDO pins as possible without using vias.

5.2 Power Supply Sequence

The VDD and VDDO power supply pins have been separated to allow flexibility in output signal levels. Power supply sequencing for VDD and VDDO requires that all VDDO be powered up either before or at the same time as VDD.

5.3 External Crystal

The external crystal should be mounted as close to the pins as possible using short PCB traces. The XA and XB traces should be kept away from other high-speed signal traces.

5.4 External Crystal Load Capacitors

The GM5351A provides the option of using internal and external crystal load capacitors. If internal load capacitance is insufficient, capacitors of value less than 2pF may be used to increased equivalent load capacitance. If external load capacitors are used, they should be placed as close to the XA/XB pads as possible.

5.5 Unused Pins

Unused XA/XB pins should be left floating.
Unused output pins (CLK0~CLK2) should be left floating.

5.6 Trace Characteristics

The GM5351A features various output current drive strengths. It is recommended to configure the trace characteristics as shown in figure 16 when the default high drive strength is used.

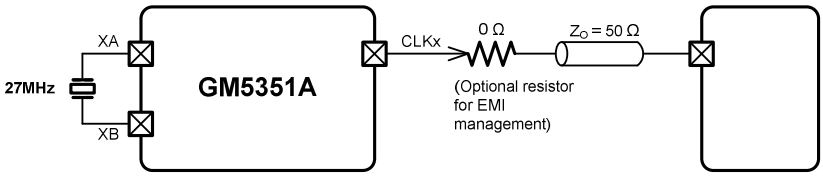


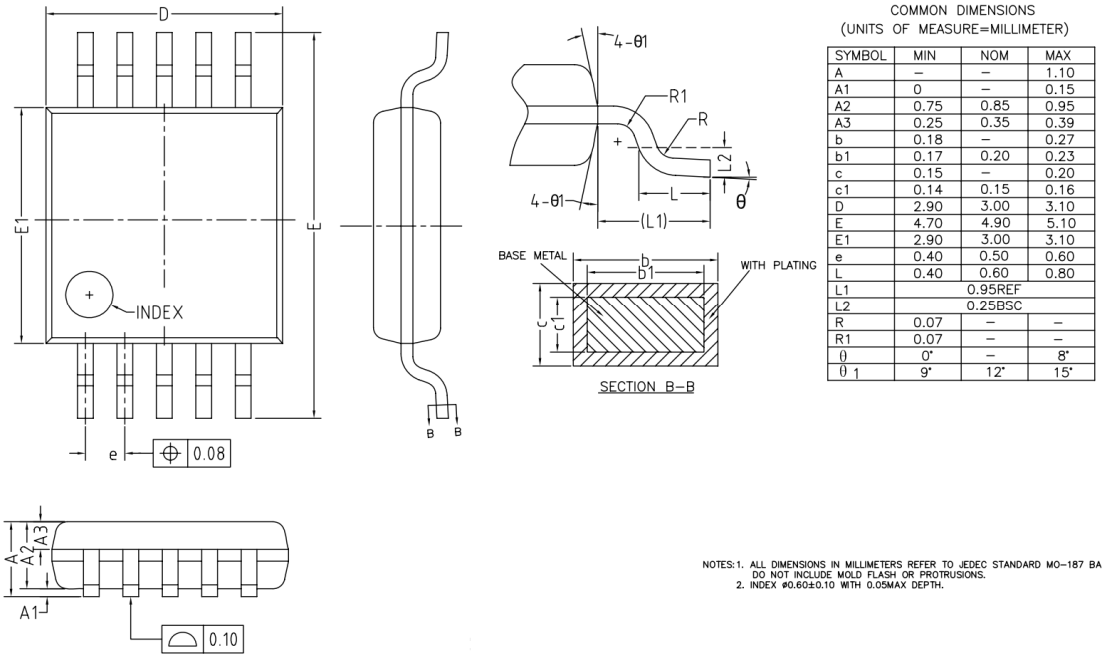
Figure 16, Recommended trace characteristics with default drive strength setting

6. REGISTER MAP

Refer to “AN5351-1: Manually Generating an GM5351A Register Map” for a detailed description of GM5351A registers.

PACKAGE OUTLINE (MSOP10)

10-Pin MSOP Package Outine Diagram



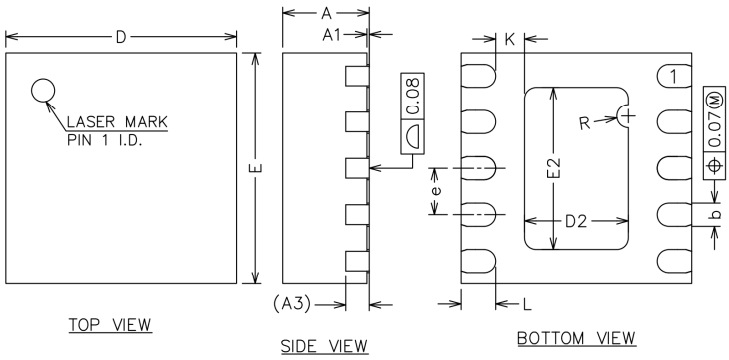
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.10
A1	0	–	0.15
A2	0.75	0.85	0.95
A3	0.25	0.35	0.39
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.15	–	0.20
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.40	0.50	0.60
L	0.40	0.60	0.80
L1	0.95REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
θ	0°	–	8°
θ 1	9°	12°	15°

NOTES: 1. ALL DIMENSIONS IN MILLIMETERS REFER TO JEDEC STANDARD MO-187 BA
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. INDEX ø0.60±0.10 WITH 0.05MAX DEPTH.

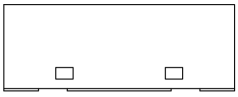
PACKAGE OUTLINE (DFN10)

10-Pin DFN Package Outline Diagram



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		020REF	
b	0.15	0.20	0.25
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.80	0.90	1.00
E2	1.30	1.40	1.50
e	0.30	0.40	0.50
K	0.15	0.25	0.35
L	0.25	0.30	0.35
R		0.10REF	



SIDE VIEW

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO-229
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

产品订购信息

器件编号	产品丝印	工作温度范围	封装信息	包装方法
GM5351A-MS -XXXXX(1)	5351A YYWW(2)	-40°C 至 +85°C	MSOP10	卷带和卷盘 (每卷 3000 只)
GM5351A-DF -XXXXX(1)	5351A YYWW(2)	-40°C 至 +85°C	DFN10-2x2	卷带和卷盘 (每卷 3000 只)

注：(1) XXXXX 表示唯一的客户编码；(2) YY 表示年号，WW 表示周号。