

DPLL for 46/49MHz Cordless Telephone

GM6533

Preliminary

Rev. 2.0

June. 1995

This specification is subject to change without notice. LG Semicon Co., Ltd. assumes no responsibility for any errors contained herein.

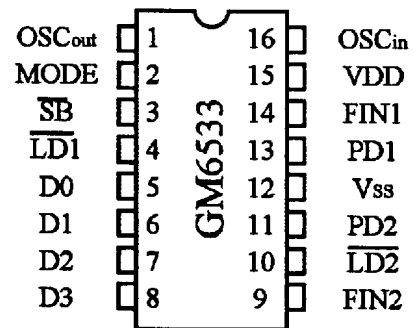
Copyright by LG Semicon Co., Ltd. all rights reserved.

Description

The GM6533 is dual phase-locked frequency synthesizer intended for use primarily in 46/49 MHz band cordless phone with up to 10 channels. This part contains two ROM programmable counters for receive and transmit loops with two independent phase detect circuits. A common reference oscillator and reference divider are shared by the receive and transmit circuits.

Other features include two lock detect circuits for transmit loop and receive loop, illegal code default, a buffered oscillator output for mixing purposes in the system, and 4 bit binary code interface with MCU for channel pair programming.

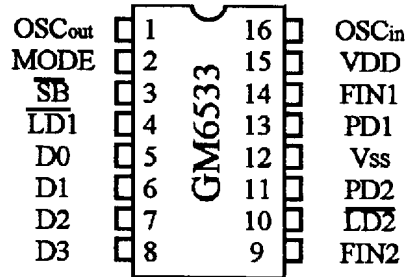
Pin Configuration



16 DIP

Features

- 10 channel ROM for 46/49 MHz cordless phone
- On-chip oscillator circuit supports external crystal
- Operating power consumption (3.0mA @2.5V)
- 2.5V to 5.5V supply range
- Two Lock detect signals :
 - LD1 - Lock detect signal for receive loop
 - LD2 - Lock detect signal for transmit loop
- Standby mode for power saving (1.5mA @2.5V)
- 16 Pin DIP (300mil), 16 Pin SOP (300mil)



16 SOP

Absolute Maximum Ratings (Voltage Referenced to Vss)

SYMBOL	RATING	VALUE	UNIT
VDD	DC Supply Voltage	-0.5 to 6	V
VIN	Input Voltage, All Input	-0.5 to VDD +0.5	V
IN, IOUT	DC Current Drain per Pin	10.0	mA
IDD, Iss	DC Current Drain VDD or Vss Pins	30.0	mA
TSTG	Storage Temperature Range	-65 to 150	°C

* The device contains circuitry to protect the inputs against damage due to high static voltages or electric fields ; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

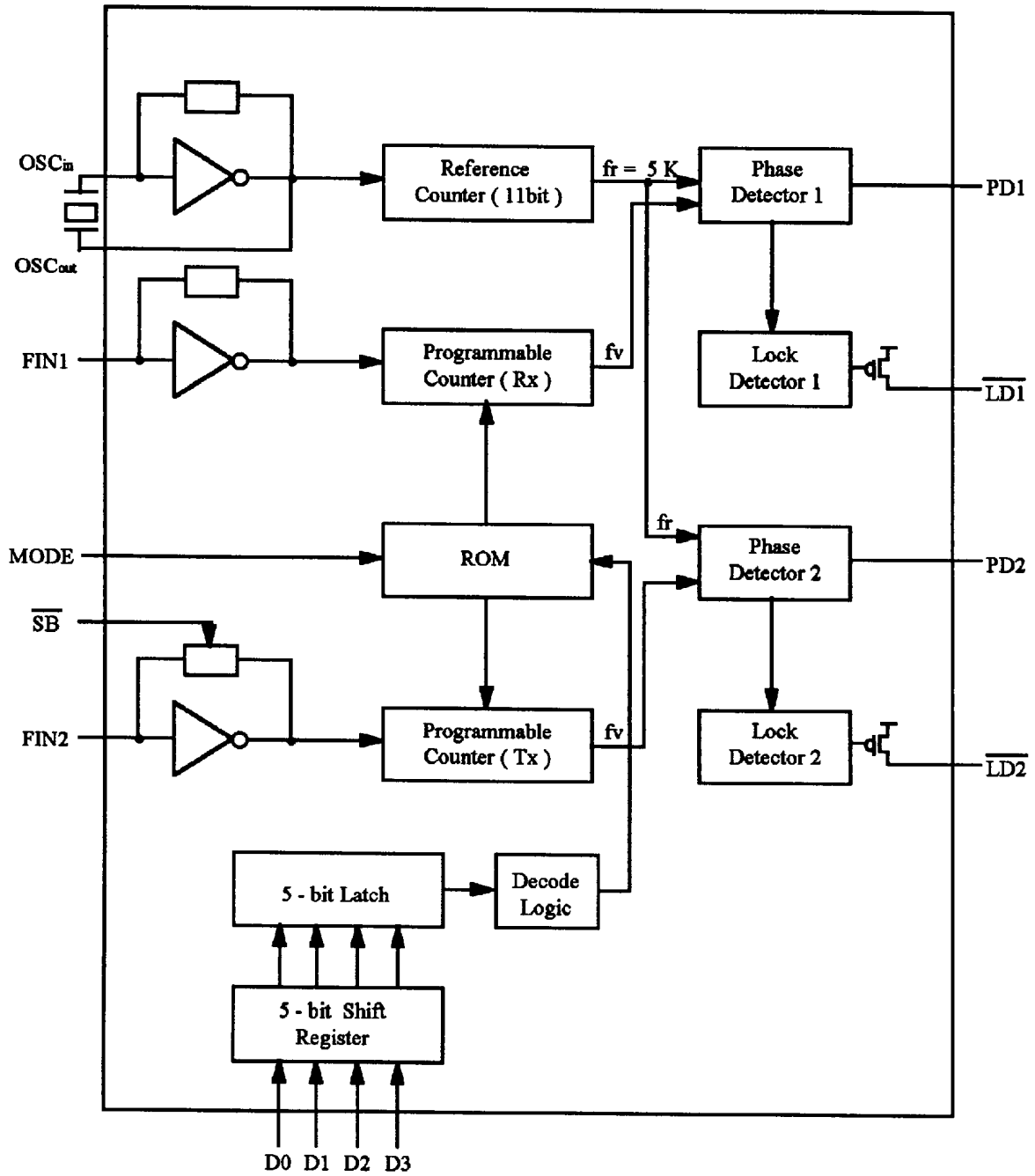
For proper operation it is recommended that VIN and VOUT be constrained to the range Vss < (VIN or VOUT) < VDD.

Unused inputs must always be tied to an appropriate logic voltage level (Vss or VDD).

Operating Range

SYMBOL	VALUE	UNIT
VDD	2.5 ~ 5.5	V
TA	- 40 ~ 75	°C

Block Diagram



Pin Description

PIN NO.	TERMINAL NAME	INPUT OUTPUT	FUNCTION
15	VDD	Power Supply	This pin is positive supply potential and may be ranged from 2.5 to 5.5 volt with respect to Vss.
12	Vss		This pin is negative supply potential and usually grounded.
16	OSC _{in}	Input	These pins form a reference oscillator when connected to an external parallel-resonant crystal. For a 46/49 MHz cordless phone application, a 10.24 MHz crystal is needed. OSC _{IN} may also serve as an input for externally generated reference signal. This signal is typically ac coupled to OSC _{IN} , but for larger signals (standard CMOS logic levels) dc coupling may also be used. In external reference mode, no connection is required for OSC _{OUT} .
1	OSC _{out}		
14	FIN1	Input	These pins are inputs to the divide-by-N receive and transmit counters, respectively. These signals are typically derived from the loop VCO and are ac coupled. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used. The minimum input level is 200mV _{P-P} (@60MHz).
9	FIN2		
13	PD1	Output	These pins are three-state outputs of the transmit and receive phase detectors for use as loop error signals. Frequency $f_v > f_r$ or f_v leading, Output = Negative pulses Frequency $f_v < f_r$ or f_v lagging, Output = Positive pulses Frequency $f_v = f_r$ and phase coincidence, Output = High - Impedance state.
11	PD2		
2	MODE	Input	Mode is for determining whether the part is to be used in the Base-set or Hand-set of a cordless phone. Internally, this pin is used in the decoding logic for selecting the ROM address. When high, the device is set in the Base-set mode, and when low, the device is set in the Hand-set mode. This input has an internal pull down.

Pin Description (continued)

PIN NO.	TERMINAL NAME	INPUT OUTPUT	FUNCTION
3	\overline{SB}	Input	The standby pin is used to save power when not transmitting. When high, the transmit and receive loops are in operation. When low, the transmit loop is disabled, thereby reducing power consumption. This input has an internal pull down device.
4	$\overline{LD1}$	Output	This lock detect signal is associated with the receive loop. The lock output goes high to indicate an output-of-lock condition. This is a P-channel open drain output.
4	$\overline{LD2}$	Output	This lock detect signal is associated with the transmit loop. The lock output goes high to indicate an output-of-lock condition. This is a P-channel open drain output.
5~8	D0~D3	Input	<p>These pins provide the 4-bit binary code for selecting the one of 10 channels to be locked in both the transmit and receive loop.</p> <p>Other input combinations will be defaulted the channel 10 by the decode logic. The frequency assignment with reference to Mode and D0~D3 is shown in table 1.2. These inputs have internal pull down devices.</p>

Electrical Characteristics
DC Characteristics (Voltages Referenced to V_{SS}, T_A = 25°C)

CHARACTERISTIC		SYMBOL	V _{DD}	Min.	Typ.	Max.	UNIT
Power Supply Voltage Range		V _{DD}		2.5		5.5	V
Output Voltages I _{OUT} = 0 V _{IN} = V _{DD} or 0	0 level	V _{OL}	2.5 5.5			0.05 0.05	V
	1 level	V _{OH}	2.5 5.5	2.45 5.45			
Input Voltages V _{OUT} = 0.5 or V _{DD} - 0.5	0 level	V _{IL}	2.5 5.5			0.75 1.65	V
	1 level	V _{IH}	2.5 5.5	1.75 3.85			
Output Current	source	V _{OH} = 2.2 V _{OH} = 5.0	I _{OH}	2.5 5.5	0.18 0.55		-mA
	sink	V _{OL} = 0.3 V _{OL} = 0.5	I _{OL}	2.5 5.5	0.18 0.55		mA
Input Current V _{IL} = 0 V _{IH} = V _{DD} - 0.5	OSC _{in} , FIN1, FIN2	I _{IL}	2.5 5.5			30 66	-μA
	SB, $\overline{\text{Mode}}$, D0~D3		2.5 5.5			1.0 1.0	
	OSC _{in} , FIN1, FIN2	I _{IH}	2.5 5.5			30 66	μA
	SB, $\overline{\text{Mode}}$, D0~D3		2.5 5.5			50 121	
Input Capacitance		C _{IN}				8.0	pF
Output Capacitance		C _{OUT}				8.0	pF
Standby Current		I _{DS}	2.5 5.5			1.5 3.5	mA
Operating Current (200mV _{PP} input at FIN1, FIN2)		I _{DD}	2.5 5.5			3.0 6.0	mA
3-State Leakage Current (V _{OUT} = 0 or 5.5V)		I _{OZ}	5.5			+/-1.0	μA

Switching Characteristics ($T_A = 25^\circ\text{C}$, $C_L = 50 \text{ pF}$)

CHARACTERISTIC		SYMBOL	V_{DD}	Min.	Typ.	Max.	UNIT
Output Rise Time		t_{TLH}	2.5 5.5			200 100	ns
Output Fall Time		t_{THL}	2.5 5.5			200 100	ns
Input Rise and Fall Time OSC _{in}		t_r, t_f	2.5 5.5			5.0 4.0	ns
Maximum Frequency Input = 250mV _{PP} sine wave	OSC _{in}	f_{max}	2.5 - 5.5			16	MHz
	FIN1		2.5 - 5.5			60	
	FIN2		2.5 - 5.5			60	

Table 1. Input Frequencies of Each Channel at Handset

CHANNEL					RX-FREQ (MHz)	RECEIVE		TX-FREQ (MHz)	TRANSMIT		MODE
D3	D2	D1	D0	CH		FIN1(MHz)	N(A)		FIN2(MHz)	N(B)	
0	0	0	1	1	46.610	35.915	7183	49.670	49.670	9934	0
0	0	1	0	2	46.630	35.935	7187	49.845	49.845	9969	0
0	0	1	1	3	46.670	35.975	7195	49.860	49.860	9972	0
0	1	0	0	4	46.710	36.015	7203	49.770	49.770	9954	0
0	1	0	1	5	46.730	36.035	7207	49.875	49.875	9975	0
0	1	1	0	6	46.770	36.075	7215	49.830	49.830	9966	0
0	1	1	1	7	46.830	36.135	7227	49.890	49.890	9978	0
1	0	0	0	8	46.870	36.175	7235	49.930	49.930	9986	0
1	0	0	1	9	46.930	36.235	7247	49.990	49.990	9998	0
1	0	1	0	10	46.970	36.275	7255	49.970	49.970	9994	0

- Note : 1. Power up and other illegal input will be defaulted to channel 10 in GM6533.
 2. 1st IF frequency of receive is 10.695MHz, 2nd IF is 455KHz.
 3. $N = \text{FIN (KHz)} / 5\text{KHz}$.

Table 2. Input Frequencies of Each Channel at Baseset

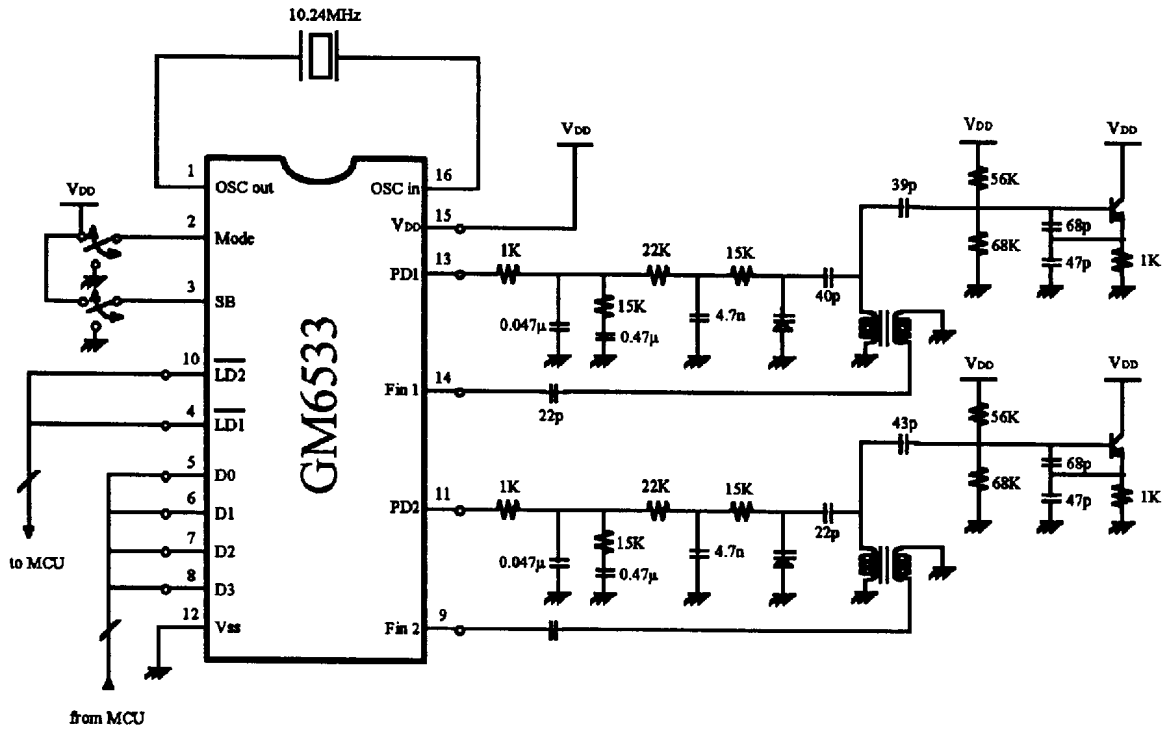
CHANNEL					RX-FREQ (MHz)	RECEIVE		TX-FREQ (MHz)	TRANSMIT		MODE
D3	D2	D1	D0	CH		FIN1(MHz)	N(A)		FIN2(MHz)	N(B)	
0	0	0	1	1	49.670	38.975	7795	46.610	46.610	9322	1
0	0	1	0	2	49.845	39.150	7830	46.630	46.630	9326	1
0	0	1	1	3	49.860	39.165	7833	46.670	46.670	9334	1
0	1	0	0	4	49.770	39.075	7815	46.710	46.710	9342	1
0	1	0	1	5	49.875	39.180	7836	46.730	46.730	9346	1
0	1	1	0	6	49.830	39.135	7827	46.770	46.770	9354	1
0	1	1	1	7	49.890	39.195	7839	46.830	46.830	9366	1
1	0	0	0	8	49.930	39.235	7847	46.870	46.870	9374	1
1	0	0	1	9	49.990	39.295	7859	46.930	46.930	9386	1
1	0	1	0	10	49.970	39.275	7855	46.970	46.970	9394	1

Note : 1. Power up and other illegal input will be defaulted to channel 10 in GM6533.

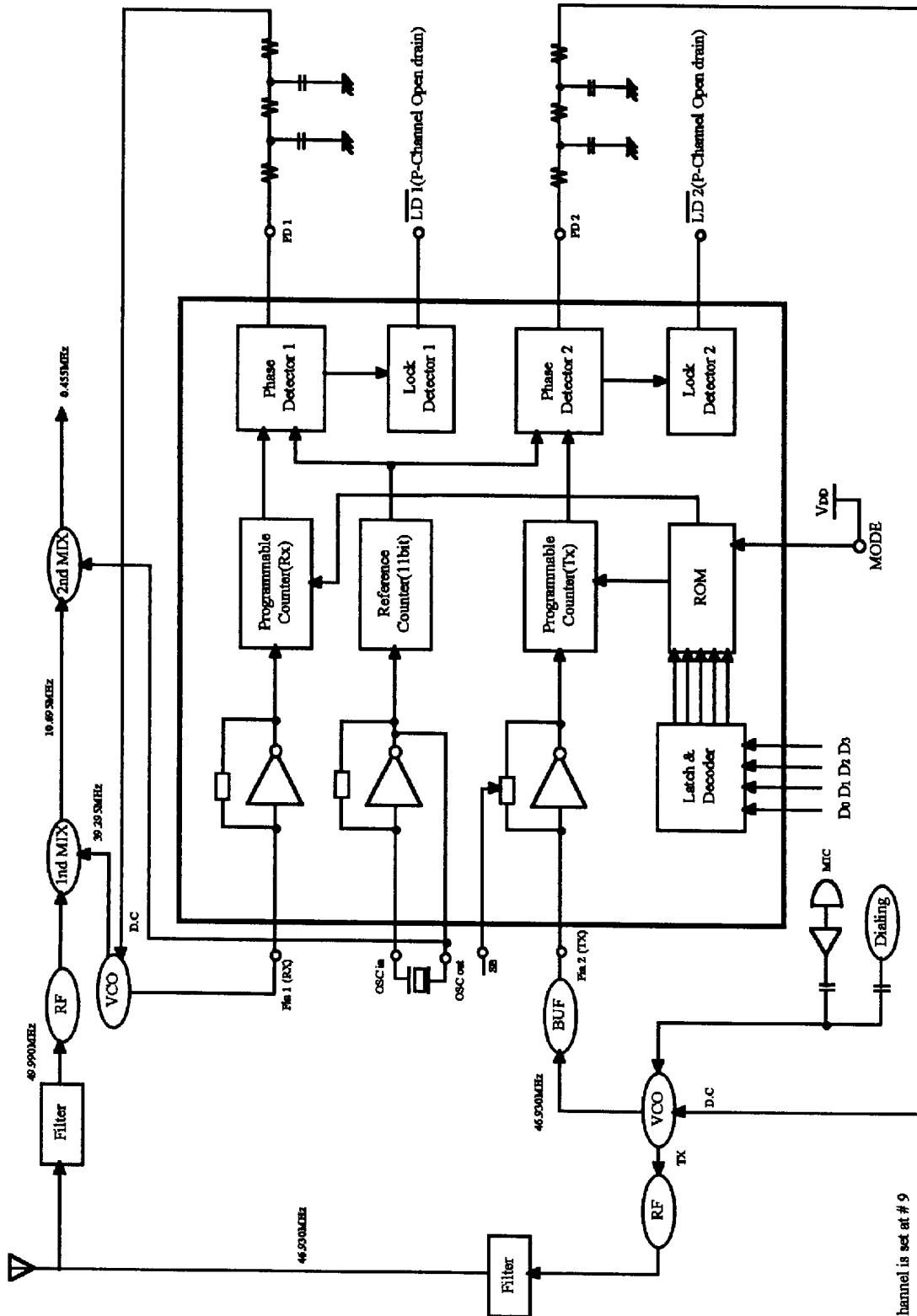
2. 1st IF frequency of receive is 10.695MHz, 2nd IF is 455KHz.

3. $N = \text{FIN (KHz)} / 5\text{KHz}$.

Low Pass Filter & VCO Test Circuit

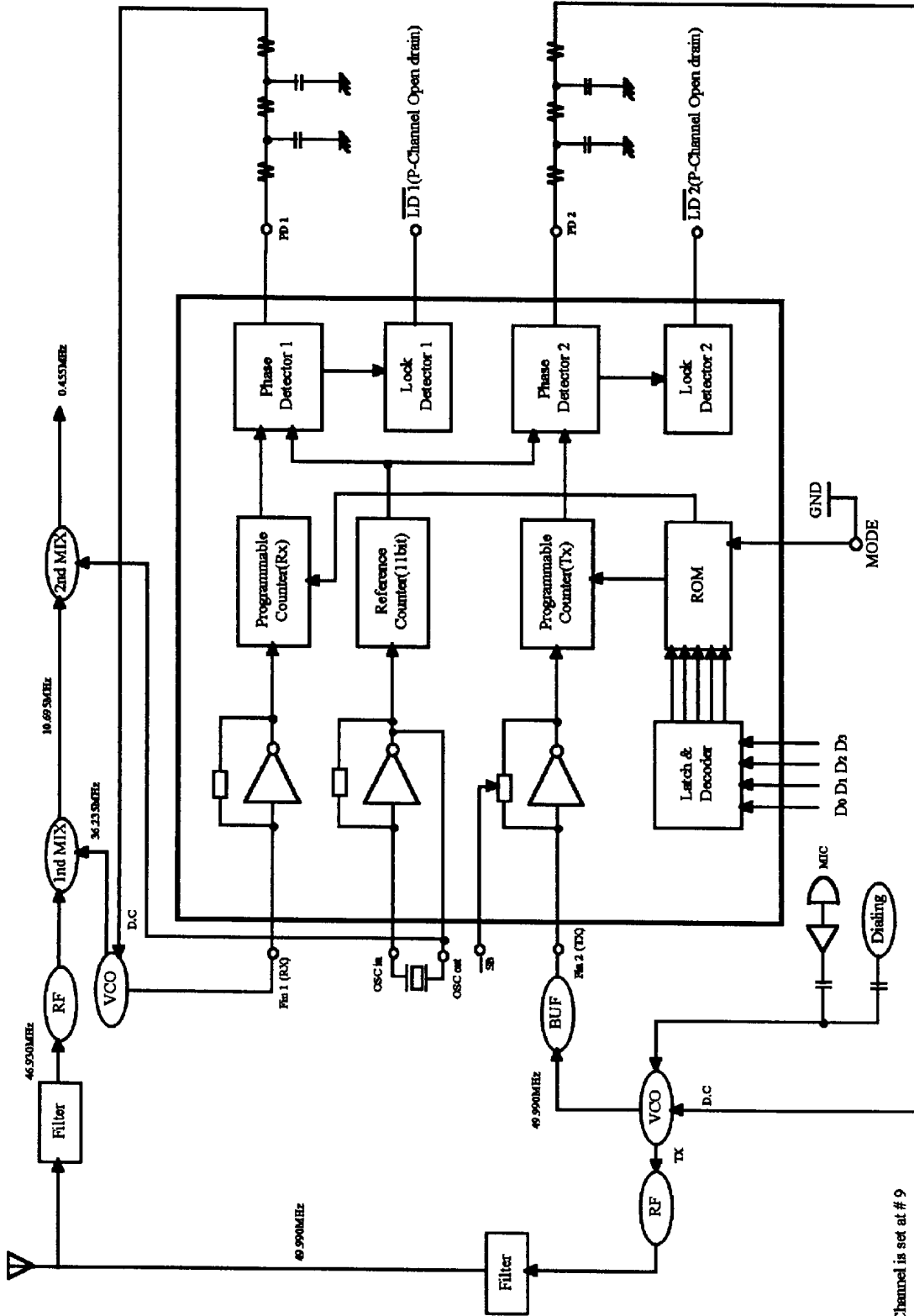


PLL Application In 46/49MHz Telephone 10 Channel Base Set



* Note Channel is set at # 9

PLL Application In 46/49MHz Telephone 10 Channel Hand Set



* Note Channel is set at # 9

Switching Waveform

