hynix

GM71V17803C
GM71VS17803CL

2,097,152 WORDS x 8 BIT
CMOS DYNAMIC RAM

Description

The GM71V(S)17803C/CL is the new generation dynamic RAM organized 2,097,152 x 8 bit. GM71V(S)17803C/CL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71V(S)17803C/CL offers Extended Data out(EDO) Page Mode as a high speed access mode. Multiplexed address inputs permit the GM71V(S)17803C/CL to be packaged in standard 400 mil 28pin plastic SOJ, and standard 400mil 28pin plastic TSOP II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

Features

* 2,097,152 Words x 8 Bit Organization
* Extended Data Out Mode Capability
* Single Power Supply (3.3V+/-0.3V)
* Fast Access Time & Cycle Time

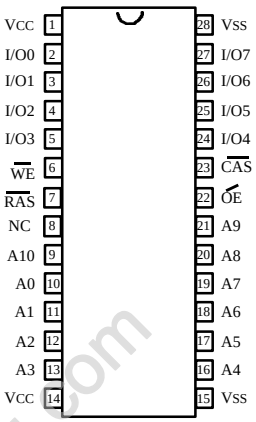
(Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
GM71V(S)17803C/CL-5	50	13	84	20
GM71V(S)17803C/CL-6	60	15	104	25
GM71V(S)17803C/CL-7	70	18	124	30

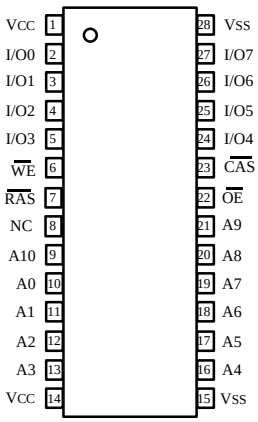
* Low Power
  Active : 396/360/324mW (MAX)
  Standby : 7.2mW (CMOS level : MAX)
  0.36mW (L-version : MAX)
* $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
* All inputs and outputs TTL Compatible
* 2048 Refresh Cycles/32ms
* 2048 Refresh Cycles/128ms (L-version)
* Self Refresh Operation (L-version)
* Battery Back Up Operation (L-version)

Pin Configuration

28 SOJ



28 TSOP II



(Top View)

Pin Description

Pin	Function	Pin	Function
A0-A10	Address Inputs	$\overline{WE}$	Read/Write Enable
A0-A10	Refresh Address Inputs	$\overline{OE}$	Output Enable
I/O0-I/O7	Data Input/ Data Output	V_{CC}	Power (+3.3V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	NC	No Connection

Ordering Information

Type No.	Access Time	Package
GM71V(S)17803CJ/CLJ -5 GM71V(S)17803CJ/CLJ -6 GM71V(S)17803CJ/CLJ -7	50ns 60ns 70ns	400 Mil 28 Pin Plastic SOJ
GM71V(S)17803CT/CLT -5 GM71V(S)17803CT/CLT -6 GM71V(S)17803CT/CLT -7	50ns 60ns 70ns	400 Mil 28 Pin Plastic TSOP II

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	C
T_{STG}	Storage Temperature	-55 ~ 125	C
$V_{IN/OUT}$	Voltage on any Pin Relative to V_{SS}	-0.5 ~ Vcc+0.5 (<=4.6V(MAX))	V
V_{CC}	Supply Voltage Relative to V_{SS}	-0.5 ~ 4.6	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Conditions (T_A = 0 ~ 70C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

Note: All voltage referred to Vss.

DC Electrical Characteristics (V_{CC} = 3.3V+/-0.3V, Vss = 0V, T_A = 0 ~ 70C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -2mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} min)	50ns	-	110	mA	1, 2
		60ns	-	100		
		70ns	-	90		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{OUT} = High-Z)		-	2	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current RAS Only Refresh Mode (t_{RC} = t_{RC} min)	50ns	-	110	mA	2
		60ns	-	100		
		70ns	-	90		
I_{CC4}	EDO Page Mode Current Average Power Supply Current EDO Page Mode (t_{HPC} = t_{HPC} min)	50ns	-	100	mA	1, 3
		60ns	-	90		
		70ns	-	85		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ >V_{CC} - 0.2V, D_{OUT} = High-Z)		-	1	mA	
			-	150	uA	5
I_{CC6}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	50ns	-	110	mA	
		60ns	-	100		
		70ns	-	90		
I_{CC7}	Battery Back Up Operating Current(Standby with CBR Ref.) (CBR refresh, t_{RC}= 62.5us, t_{RAS}<= 0.3us, D_{OUT}=High-Z, CMOS Interface)		-	400	uA	4,5
I_{CC8}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		-	5	mA	1
I_{CC9}	Self-Refresh Mode Current ($\overline{RAS}$, $\overline{CAS}$<= 0.2V, D_{OUT}=High-Z, CMOS interface)		-	250	uA	5
$I_{L(I)}$	Input Leakage Current Any Input (0V<= V_{IN}<= 4.6V)		-10	10	uA	
$I_{L(O)}$	Output Leakage Current (D_{OUT} is Disabled, 0V<= V_{OUT}<= 4.6V)		-10	10	uA	

Note: 1. I_{CC} depends on output load condition when the device is selected.
I_{CC}(max) is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. $\overline{CAS}$ = L (<=0.2V) while $\overline{RAS}$ = L (<=0.2V).
5. L -version.

Capacitance (V_{CC} = 3.3V+/-0.3V, T_A = 25C)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	-	5	pF	1
C_{I2}	Input Capacitance (Clocks)	-	7	pF	1
$C_{I/O}$	Output Capacitance (Data-In/Out)	-	7	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

AC Characteristics (V_{CC} = 3.3V+/-0.3V, T_A = 0 ~ +70C, Note 1, 2, 18)

Test Conditions

Input rise and fall times : 2 ns
Input levels : VIL = 0V, VIH = 3V
Input timing reference levels : 0.8V, 2.0V
Output timing reference levels : 0.8V, 2.0V
Output load : 1TTL gate + C_L (100 pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71V(S)17803 C/CL-5		GM71V(S)17803 C/CL-6		GM71V(S)17803 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	84	-	104	-	124	-	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	30	-	40	-	50	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	8	-	10	-	13	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	50	10,000	60	10,000	70	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	8	10,000	10	10,000	13	10,000	ns	
t_{ASR}	Row Address Set up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	8	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	8	-	10	-	13	-	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	12	37	14	45	14	52	ns	3
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	10	25	12	30	12	35	ns	4
t_{RSH}	$\overline{RAS}$ Hold Time	10	-	13	-	13	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	35	-	40	-	45	-	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	13	-	15	-	18	-	ns	5
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	-	0	-	0	-	ns	6
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	-	0	-	0	-	ns	6
t_T	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	7

Read Cycle

Symbol	Parameter	GM71V(S)17803C/CL-5		GM71V(S)17803C/CL-6		GM71V(S)17803C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	-	50	-	60	-	70	ns	8,9
t_{CAC}	Access Time from $\overline{CAS}$	-	13	-	15	-	18	ns	9,10,17
t_{AA}	Access Time from Address	-	25	-	30	-	35	ns	9,11,17
t_{OAC}	Access Time from $\overline{OE}$	-	13	-	15	-	18	ns	9
t_{RCS}	Read Command Setup Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	-	0	-	0	-	ns	12
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	-	5	-	5	-	ns	12
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25	-	30	-	35	-	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	15	-	18	-	23	-	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t_{OH}	Output Data Hold Time	3	-	3	-	3	-	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	3	-	3	-	3	-	ns	
t_{OFF}	Output Buffer Turn-off Time	-	13	-	15	-	15	ns	13
t_{OEZ}	Output Buffer Turn-off Time to $\overline{OE}$	-	13	-	15	-	15	ns	13
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	13	-	15	-	18	-	ns	5
t_{RCHR}	Read Command Hold Time from $\overline{RAS}$	50	-	60	-	70	-	ns	
t_{OHR}	Output Data hold Time from $\overline{RAS}$	3	-	3	-	3	-	ns	
t_{OFR}	Output Buffer turn off to $\overline{RAS}$	-	13	-	15	-	15	ns	
t_{WEZ}	Output Buffer turn off to $\overline{WE}$	-	13	-	15	-	15	ns	
t_{WDD}	$\overline{WE}$ to D_{IN} Delay Time	13	-	15	-	18	-	ns	
t_{RDD}	$\overline{RAS}$ to D_{IN} Delay Time	13	-	15	-	18	-	ns	

Write Cycle

Symbol	Parameter	GM71V(S)17803 C/CL-5		GM71V(S)17803 C/CL-6		GM71V(S)17803 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Setup Time	0	-	0	-	0	-	ns	14
t_{WCH}	Write Command Hold Time	8	-	10	-	13	-	ns	
t_{WP}	Write Command Pulse Width	8	-	10	-	10	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	8	-	10	-	13	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	8	-	10	-	13	-	ns	
t_{DS}	Data-in Setup Time	0	-	0	-	0	-	ns	15
t_{DH}	Data-in Hold Time	8	-	10	-	13	-	ns	15

Read- Modify-Write Cycle

Symbol	Parameter	GM71V(S)17803 C/CL-5		GM71V(S)17803 C/CL-6		GM71V(S)17803 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	111	-	136	-	161	-	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	67	-	79	-	92	-	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	30	-	34	-	40	-	ns	14
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	42	-	49	-	57	-	ns	14
t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$	13	-	15	-	18	-	ns	

Refresh Cycle

Symbol	Parameter	GM71V(S)17803 C/CL-5		GM71V(S)17803 C/CL-6		GM71V(S)17803 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	5	-	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	8	-	10	-	10	-	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	0	-	0	-	0	-	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	-	10	-	10	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	-	5	-	5	-	ns	

EDO Page Mode Cycle

Symbol	Parameter	GM71V(S)17803 C/CL-5		GM71V(S)17803 C/CL-6		GM71V(S)17803 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{HPC}	EDO Page Mode Cycle Time	20	-	25	-	30	-	ns	19
t_{RASP}	EDO Page Mode $\overline{RAS}$ Pulse Width	-	100,000	-	100,000	-	100,000	ns	16
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	-	30	-	35	-	40	ns	9,17
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	30	-	35	-	40	-	ns	
t_{DOH}	Output data Hold Time from $\overline{CAS}$ low	3	-	3	-	3		ns	9,17
t_{COL}	$\overline{CAS}$ Hold Time referred $\overline{OE}$	8	-	10	-	13		ns	
t_{COP}	$\overline{CAS}$ to $\overline{OE}$ Setup Time	5	-	5	-	5		ns	
t_{RCHP}	Read command Hold Time from $\overline{CAS}$ Precharge	30	-	35	-	40		ns	

EDO Page Mode Read-Modify-Write Cycle

Symbol	Parameter	GM71V(S)17803 C/CL-5		GM71V(S)17803 C/CL-6		GM71V(S)17803 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{HPRWC}	EDO Page Mode Read-Modify-Write Cycle Time	57	-	68	-	79	-	ns	
t_{CPW}	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	45	-	54	-	62	-	ns	14

Refresh

Symbol	Parameter	GM71V(S)17803 C/CL-5		GM71V(S)17803 C/CL-6		GM71V(S)17803 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{REF}	Refresh period	-	32	-	32	-	32	ms	2048 cycles
t_{REF}	Refresh period (L -version)	-	128	-	128	-	128	ms	2048 cycles

Self Refresh Mode (L-version)

Symbol	Parameter	GM71VS17400 CL-5		GM71VS17400 CL-6		GM71VS17400 CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RASS}	$\overline{RAS}$ Pulse Width(Self-Refresh)	100	-	100	-	100	-	us	
t_{RPS}	$\overline{RAS}$ Precharge Time(Self-Refresh)	90	-	110	-	130	-	ns	
t_{CHS}	$\overline{CAS}$ Hold Time(Self-Refresh)	-50	-	-50	-	-50	-	ns	

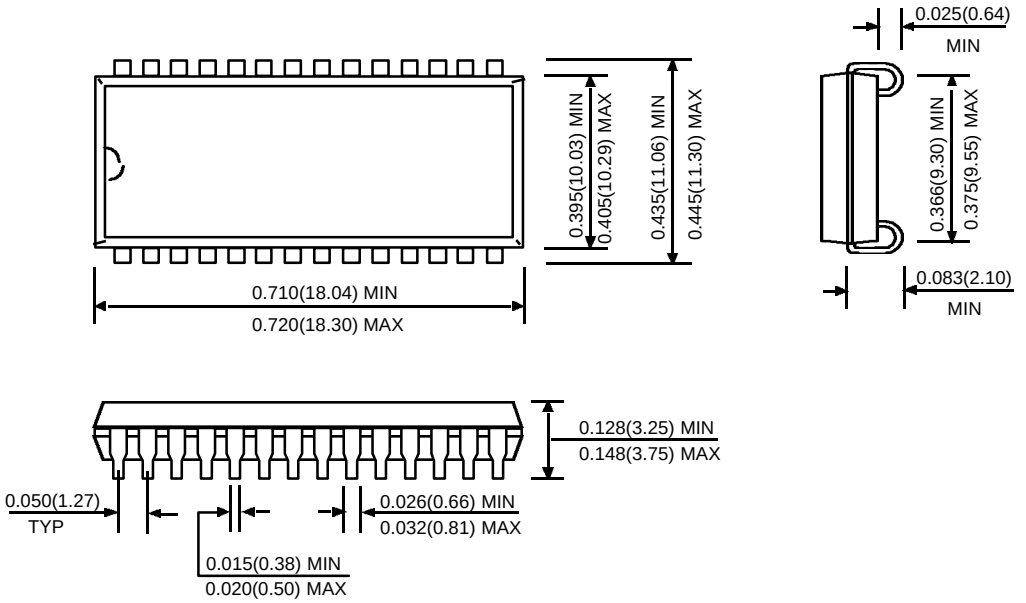
Notes:

1. AC Measurements assume t_T = 2ns.
2. An initial pause of 200us is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{ODD} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that t_{RCD} <= t_{RCD} (max) and t_{RAD} <= t_{RAD} (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1TTL loads and 100pF.
10. Assumes that t_{RCD} >= t_{RCD} (max) and t_{RAD} <= t_{RAD} (max).
11. Assumes that t_{RCD} <= t_{RCD} (max) and t_{RAD} >= t_{RAD} (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if t_{WCS} >=t_{WCS}(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if t_{RWD}>=t_{RWD}(min), t_{CWD}>=t_{CWD}(min) and t_{AWD}>=t_{AWD}(min), or t_{CWD}>=t_{CWD}(min), t_{AWD}>=t_{AWD}(min) and t_{CPW}>=t_{CPW}(min), the cycle is a read modify write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to $\overline{CAS}$ leading edge in early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read modify write cycle.
16. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.
17. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{ACP}.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if t_{OEH}>=t_{CWL}, the I/O pin will remain open circuit (high impedance): if t_{OEH}<=t_{CWL}, invalid data will be out at each I/O.
19. EDO Hi-Z control by $\overline{OE}$ or $\overline{WE}$. $\overline{OE}$ rising edge disables data outputs. When $\overline{OE}$ goes high during $\overline{CAS}$ high, the data will not come out until next $\overline{CAS}$ access. When $\overline{WE}$ goes low during $\overline{CAS}$ high, the data will not come out until next $\overline{CAS}$ access.
20. t_{HPC}(min) can be achieved during a series of EDO mode write cycles or EDO mode read cycles. If both write and read operation are mixed in a EDO mode $\overline{RAS}$ cycle(EDO mode mix cycle (1),(2)) minimum value of $\overline{CAS}$ cycle (t_{CAS} + t_{CP} + 2t_T) becomes greater than the specified t_{HPC}(min) value. The value of $\overline{CAS}$ cycle time of mixed EDO mode is shown in EDO mode mix cycle (1) and (2).

Package Dimensions

Unit: Inches (mm)

28 SOJ



28 TSOP (TYPE II)