



**Description**

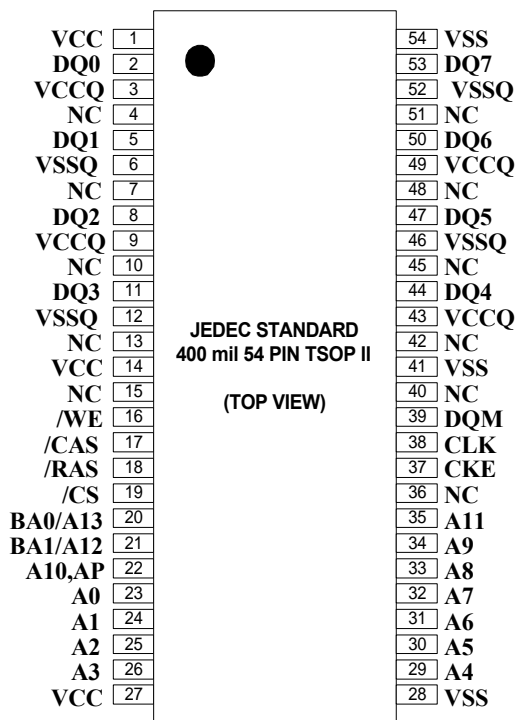
The GM72V66841CT/CLT is a synchronous dynamic random access memory comprised of 67,108,864 memory cells and logic including input and output circuits operating synchronously by referring to the positive edge of the externally provided Clock.

The GM72V66841CT/CLT provides four banks of 2,097,152 word by 8 bit to realize high bandwidth with the Clock frequency up to 125 Mhz.

**Features**

- \* PC100,PC66 Compatible  
7K(2-2-2), 7J(3-2-2), 10K(PC66)
- \* 3.3V single Power supply
- \* LVTTL interface
- \* Max Clock frequency  
100/125 MHz
- \* 4,096 refresh cycle per 64 ms
- \* Two kinds of refresh operation  
Auto refresh/ Self refresh
- \* Programmable burst access capability ;  
- Sequence:Sequential / Interleave  
- Length :1/2/4/8/FP
- \* Programmable CAS latency : 2/3
- \* 4 Banks can operate independently or simultaneously
- \* Burst read/burst write or burst read/single write operation capability
- \* Input and output masking by DQM input
- \* One Clock of back to back read or write command interval
- \* Synchronous Power down and Clock suspend capability with one Clock latency for both entry and exit
- \* JEDEC Standard 54Pin 400mil TSOP II Package

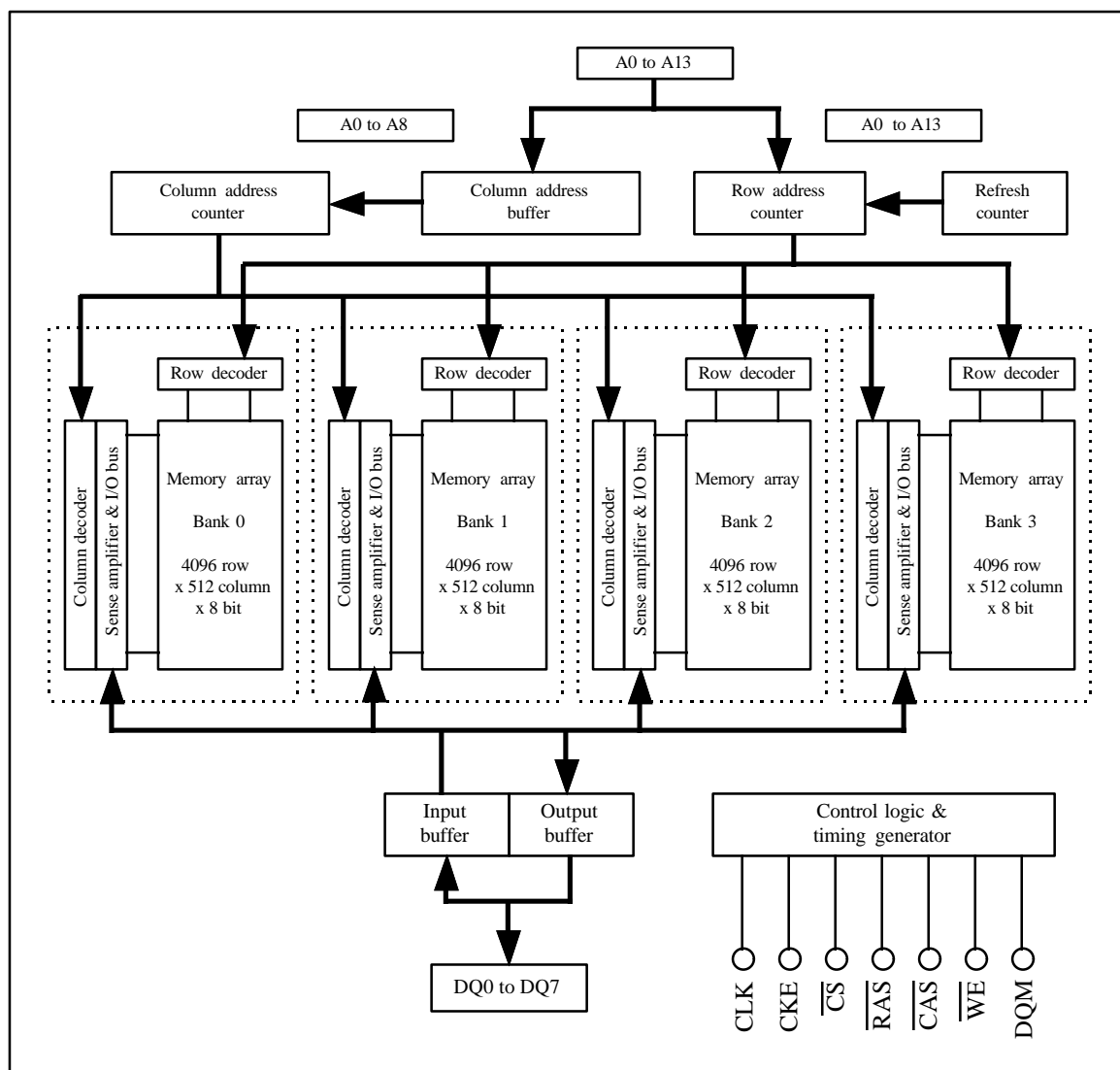
**Pin Configuration**



**Pin Name**

|                     |                                 |
|---------------------|---------------------------------|
| CLK                 | Clock                           |
| <u>CKE</u>          | Clock Enable                    |
| <u>CS</u>           | Chip Select                     |
| <u>RAS</u>          | Row Address Strobe              |
| <u>CAS</u>          | Column Address Strobe           |
| <u>WE</u>           | Write Enable                    |
| A0~A9,A11           | Address input                   |
| A10 / AP            | Address input or Auto Precharge |
| BA0/A13<br>~BA1/A12 | Bank select                     |
| DQ0~DQ7             | Data input / Data output        |
| DQM                 | Data input / output Mask        |
| VCCQ                | Vcc for DQ                      |
| VSSQ                | Vss for DQ                      |
| VCC                 | Power for internal circuit      |
| VSS                 | Ground for internal circuit     |
| NC                  | No Connection                   |

### Block Diagram



### Pin Description

| Pin Name  | DESCRIPTION  |
|---|--|
| CLK<br>(input pin)  | CLK is the master Clock input to this pin. The other input signals are referred at CLK rising edge.  |
| CKE<br>(input pin)  | This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for Power-down and Clock suspend modes.  |
| $\overline{CS}$<br>(input pin)  | When $\overline{CS}$ is Low, the command input cycle becomes valid. When $\overline{CS}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.   |
| $\overline{RAS}$ , $\overline{CAS}$ , and $\overline{WE}$<br>(input pins) | Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.  |
| A0 ~ A11<br>(input pins)  | Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CLK rising edge. Column address(AY0 to AY8; GM72V66841CT/CLT) is determined by A0 to A8 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the Precharge mode. When A10 = High at the Precharge command cycle, all banks are Precharged. But when A10 = Low at the Precharge command cycle, only the bank that is selected by A12/A13 (BS) is Precharged. |
| A12/A13<br>(input pin)  | A12/A13 are bank select signal (BS). The memory array of the GM72V66841CT/CLT is divided into bank 0, bank 1, bank2 and bank 3. GM72V66841CT/CLT contain 4096-row x 512-column x 8-bits. If A12 is Low and if A13 is Low, bank 0 is selected. If A12 is High and A13 is Low, bank 1 is selected. If A12 is Low and A13 is High, bank 2 is selected. If A12 is High and A13 is High, bank 3 is selected.  |
| DQM,<br>DQMU/DQML<br>(input pins)   | DQM, DQMU/DQML controls input/output buffers.<br>* Read operation: If DQM, DQMU/DQML is High, The output buffer becomes High-Z. If the DQM, DQMU/DQML is Low, the output buffer becomes Low-Z.<br>* Write operation: If DQM, DQMU/DQML is High, the previous data is held (the new data is not written). If DQM, DQMU/DQML is Low, the data is written.  |

### Pin Description(Continued)

| Pin Name  | DESCRIPTION   |
|---|---|
| DQ0 ~ DQ7<br>(I/O pins)                                     | Data is input and output from these pins. These pins are the same as those of a conventional DRAM.                |
| V <sub>CC</sub> and V <sub>CCQ</sub><br>(Power supply pins) | 3.3 V is applied. (V <sub>CC</sub> is for the internal circuit and V <sub>CCQ</sub> is for the output buffer.)    |
| V <sub>SS</sub> and V <sub>SSQ</sub><br>(Power supply pins) | Ground is connected. (V <sub>SS</sub> is for the internal circuit and V <sub>SSQ</sub> is for the output buffer.) |
| NC  | No Connection pins.   |

### Command Operation

#### Command Truth Table

The synchronous DRAM recognizes the following commands specified by the  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$  and address pins.

| Function                           | Symbol   | CKE |   | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | A12~<br>A13 | A10 | A0~<br>A11 |
|------------------------------------|----------|-----|---|-----------------|------------------|------------------|-----------------|-------------|-----|------------|
|                                    |          | n-1 | n |                 |                  |                  |                 |             |     |            |
| Ignore command                     | DESL     | H   | X | H               | X                | X                | X               | X           | X   | X          |
| No Operation                       | NOP      | H   | X | L               | H                | H                | H               | X           | X   | X          |
| Burst stop in full page            | BST      | H   | X | L               | H                | H                | L               | X           | X   | X          |
| Column address and read command    | READ     | H   | X | L               | H                | L                | H               | V           | L   | V          |
| Read with auto-Precharge           | READ A   | H   | X | L               | H                | L                | H               | V           | H   | V          |
| Column address and write command   | WRIT     | H   | X | L               | H                | L                | L               | V           | L   | V          |
| Write with auto-Precharge          | WRIT A   | H   | X | L               | H                | L                | L               | V           | H   | V          |
| Row address strobe and bank active | ACTV     | H   | X | L               | L                | H                | H               | V           | V   | V          |
| Precharge select bank              | PRE      | H   | X | L               | L                | H                | L               | V           | L   | X          |
| Precharge all banks                | PALL     | H   | X | L               | L                | H                | L               | X           | H   | X          |
| Refresh                            | REF/SELF | H   | V | L               | L                | L                | H               | X           | X   | X          |
| Mode register set                  | MRS      | H   | X | L               | L                | L                | L               | V           | V   | V          |

\* Notes : H: V<sub>IH</sub>, L: V<sub>IL</sub>, X: V<sub>IH</sub> or V<sub>IL</sub>, V: Valid address input

**Ignore command [DESL]:** When this command is set (CS is High), the synchronous DRAM ignores command input at the Clock. However, the internal status is held.

**No operation [NOP]:** This command is not an execution command. However, the internal operations continue.

**Burst stop in full page [BST] :** This command stops a full-page burst operation (burst length = full-page(512;GM72V66841CT/CLT) and is illegal otherwise. Full page burst continues until this command is input. When data input/output is completed for full-page of data, it automatically returns to the start address, and input/output is performed repeatedly.

**Column address strobe and read command [READ]:** This command starts a read operation. In addition, the start address of burst read is determined by the column address (AY0 to AY8; GM72V66841CT/CLT) and the bank select address (A12/A13). After the read operation, the output buffer becomes High-Z.

**Read with auto-Precharge [READ A]:** This command automatically performs a Precharge operation after a burst read with a burst length of 1, 2, 4 or 8. When the burst length is full-page, this command is illegal.

**Column address strobe and write command [WRIT]:** This command starts a write operation. When the burst write mode is selected, the column address (AY0 to AY8; GM72V66841CT/CLT) and the bank select address (A12/A13) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (AY0 to AY8;GM72V66841CT/CLT) and the bank select address (A12/A13).

**Write with auto-Precharge [WRIT A]:** This command automatically performs a Precharge operation after a burst write with a length of 1, 2, 4 or 8, or after a single write operation. When the burst length is full-page, this command is illegal.

**Row address strobe and bank activate [ACTV]:** This command activates the bank that is selected by A12/A13(BS) and determines the row address (AX0 to AX11). If A12 is Low and if A13 is Low, bank 0 is activated. If A12 is High and A13 is Low, bank 1 is activated. If A12 is Low and A13 is High, bank 2 is activated. If A12 is High and A13 is High, bank 3 is activated.

**Precharge selected bank [PRE]:** This command starts Precharge operation for the bank selected by A12/A13. If A12 is Low and if A13 is Low, bank 0 is selected. If A12 is High and A13 is Low, bank 1 is selected. If A12 is Low and A13 is High, bank 2 is selected. If A12 is High and A13 is High, bank 3 is selected.

**Precharge all banks [PALL]:** This command starts a Precharge operation for all banks.

**Refresh [REF/SELF]:** This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self-refresh. For details, refer to the CKE truth table section.

**Mode register set [MRS]:** Synchronous DRAM has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to A11) at the mode register set cycle. For details, refer to the mode register configuration. After Power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

### DQM Truth Table

| Function                     | Symbol | CKE | n | DQM |
|------------------------------|--------|-----|---|-----|
|                              |        | n-1 |   |     |
| Write enable/output enable   | ENB    | H   | X | L   |
| Write inhibit/output disable | MASK   | H   | X | H   |

\* Notes : H: VIH, L: VIL, X: VIH or VIL.

Write : lDID is needed.

Read : lDOD is needed.

The GM72V66841CT/CLT can mask input/output data by means of DQM.

During reading, the output buffer is set to Low-Z by setting DQM to Low, enabling data output. On the other hand, when DQM is set to High, the output buffer becomes High-Z, disabling data output.

During writing, data is written by setting DQM to Low. When DQM is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQM. For details, refer to the DQM control section of the GM72V66841CT/CLT operating instructions.

### CKE Truth Table

| Current State | Function                   | CKE  |   | $\overline{\text{CS}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | Address |
|---------------|----------------------------|------|---|------------------------|-------------------------|-------------------------|------------------------|---------|
|               |                            | n -1 | n |                        |                         |                         |                        |         |
| Active        | Clock suspend mode entry   | H    | L | H                      | X                       | X                       | X                      | X       |
| Any           | Clock suspend              | L    | L | X                      | X                       | X                       | X                      | X       |
| Clock Suspend | Clock suspend mode exit    | L    | H | X                      | X                       | X                       | X                      | X       |
| Idle          | Auto-refresh command (REF) | H    | H | L                      | L                       | L                       | H                      | X       |
| Idle          | Self-refresh entry (SELF)  | H    | L | L                      | L                       | L                       | H                      | X       |
| Idle          | Power down entry           | H    | L | L                      | H                       | H                       | H                      | X       |
|               |                            | H    | L | H                      | X                       | X                       | X                      | X       |
| Self refresh  | Self refresh exit (SELFX)  | L    | H | L                      | H                       | H                       | H                      | X       |
|               |                            | L    | H | H                      | X                       | X                       | X                      | X       |
| Power down    | Power down Exit            | L    | H | L                      | H                       | H                       | H                      | X       |
|               |                            | L    | H | H                      | X                       | X                       | X                      | X       |

\* Notes : H: VIH, L: VIL, X: VIH or VIL.

**Clock suspend mode entry:** The synchronous DRAM enters Clock suspend mode from active mode by setting CKE to Low. The Clock suspend mode changes depending on the current status (1 Clock before) as shown below.

**ACTIVE Clock suspend:** This suspend mode ignores inputs after the next Clock by internally maintaining the bank active status.

**READ suspend and READ A suspend:** The data being output is held (and continues to be output).

**WRITE suspend and WRIT A suspend:** In this mode, external signals are not accepted. However, the internal state is held.

**Clock suspend:** During Clock suspend mode, keep the CKE to Low.

**Clock suspend mode exit :** The synchronous DRAM exits from Clock suspend mode by setting CKE to High during the Clock suspend state.

**IDLE:** In this state, all banks are not selected, and completed Precharge operation.

**Auto-refresh command[REF]:** When this command is input from the IDLE state, the synchronous DRAM starts auto-refresh operation. (The auto-refresh is the same as the CBR refresh of conventional DRAMs.) During the auto-refresh operation, refresh address and bank select address are generated inside the synchronous DRAM. For every auto-refresh cycle, the internal address counter is updated. Accordingly, 4,096 times are required to refresh the entire memory. Before executing the auto-refresh command, all the banks must be in the IDLE state. In addition, since the Precharge for all banks is automatically performed after auto-refresh, no Precharge command is required after auto-refresh.

**Self-refresh entry[SELF]:** When this command is input during the IDLE state, the synchronous DRAM starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is Low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

**Self-refresh exit[SELFX]:** When this command is executed during self-refresh mode, the synchronous DRAM can exit from self-refresh mode. After exiting from self-refresh mode, the synchronous DRAM enters the IDLE state.

**Power down mode entry:** When this command is executed during the IDLE state, the synchronous DRAM enters Power down mode. In Power down mode, Power consumption is suppressed by cutting off the initial input circuit.

**Power down exit:** When this command is executed at the Power down mode, the synchronous DRAM can exit from Power down mode. After exiting from Power down mode, the synchronous DRAM enters the IDLE state.

### Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the synchronous DRAM.

| Current state | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | Address     | Command     | Operation                 |
|---------------|-----------------|------------------|------------------|-----------------|-------------|-------------|---------------------------|
| Precharge     | H               | X                | X                | X               | X           | DESL        | Enter IDLE after $t_{RP}$ |
|               | L               | H                | H                | H               | X           | NOP         | Enter IDLE after $t_{RP}$ |
|               | L               | H                | H                | L               | X           | BST         | NOP                       |
|               | L               | H                | L                | H               | BA, CA, A10 | READ/READ A | ILLEGAL                   |
|               | L               | H                | L                | L               | BA, CA, A10 | WRIT/WRIT A | ILLEGAL                   |
|               | L               | L                | H                | H               | BA, RA      | ACTV        | ILLEGAL                   |
|               | L               | L                | H                | L               | BA, A10     | PRE, PALL   | NOP                       |



**Function Truth Table (Continued)**

| Current state | $\overline{\text{CS}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | Address     | Command     | Operation   |
|---------------|------------------------|-------------------------|-------------------------|------------------------|-------------|-------------|---|
| Precharge     | L                      | L                       | L                       | H                      | X           | REF, SELF   | ILLEGAL   |
|               | L                      | L                       | L                       | L                      | MODE        | MRS         | ILLEGAL   |
| Idle          | H                      | X                       | X                       | X                      | X           | DESL        | NOP   |
|               | L                      | H                       | H                       | H                      | X           | NOP         | NOP   |
|               | L                      | H                       | H                       | L                      | X           | BST         | NOP   |
|               | L                      | H                       | L                       | H                      | BA, CA, A10 | READ/READ A | ILLEGAL   |
|               | L                      | H                       | L                       | L                      | BA, CA, A10 | WRIT/WRIT A | ILLEGAL   |
|               | L                      | L                       | H                       | H                      | BA, RA      | ACTV        | Bank and row active                                     |
|               | L                      | L                       | H                       | L                      | BA, A10     | PRE, PALL   | NOP   |
|               | L                      | L                       | L                       | H                      | X           | REF, SELF   | Refresh   |
|               | L                      | L                       | L                       | L                      | MODE        | MRS         | Mode register set                                       |
|               | Row active             | H                       | X                       | X                      | X           | X           | DESL  |
| L             |                        | H                       | H                       | H                      | X           | NOP         | NOP   |
| L             |                        | H                       | H                       | L                      | X           | BST         | NOP   |
| L             |                        | H                       | L                       | H                      | BA, CA, A10 | READ/READ A | Begin read  |
| L             |                        | H                       | L                       | L                      | BA, CA, A10 | WRIT/WRIT A | Begin write   |
| L             |                        | L                       | H                       | H                      | BA, RA      | ACTV        | Other bank active<br>ILLEGAL on same bank <sup>*3</sup> |
| L             |                        | L                       | H                       | L                      | BA, A10     | PRE, PALL   | Precharge   |
| L             |                        | L                       | L                       | H                      | X           | REF, SELF   | ILLEGAL   |
| L             |                        | L                       | L                       | L                      | MODE        | MRS         | ILLEGAL   |

**Function Truth Table (Continued)**

| Current state            | $\overline{\text{CS}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | Address     | Command     | Operation   |
|--------------------------|------------------------|-------------------------|-------------------------|------------------------|-------------|-------------|---|
| Read                     | H                      | X                       | X                       | X                      | X           | DESL        | Continue burst to end   |
|                          | L                      | H                       | H                       | H                      | X           | NOP         | Continue burst to end   |
|                          | L                      | H                       | H                       | L                      | X           | BST         | Burst stop to full page   |
|                          | L                      | H                       | L                       | H                      | BA, CA, A10 | READ/READ A | Continue burst read to $\overline{\text{CAS}}$ latency and New read |
|                          | L                      | H                       | L                       | L                      | BA, CA, A10 | WRIT/WRIT A | Term burst read/start write   |
|                          | L                      | L                       | H                       | H                      | BA, RA      | ACTV        | Other bank active <sup>*3</sup><br>ILLEGAL on same bank             |
|                          | L                      | L                       | H                       | L                      | BA, A10     | PRE, PALL   | Term burst read and Precharge                                       |
|                          | L                      | L                       | L                       | H                      | X           | REF, SELF   | ILLEGAL   |
|                          | L                      | L                       | L                       | L                      | MODE        | MRS         | ILLEGAL   |
| Read with auto-Precharge | H                      | X                       | X                       | X                      | X           | DESL        | Continue burst to end and Precharge                                 |
|                          | L                      | H                       | H                       | H                      | X           | NOP         | Continue burst to end and Precharge                                 |
|                          | L                      | H                       | H                       | L                      | X           | BST         | ILLEGAL   |
|                          | L                      | H                       | L                       | H                      | BA, CA, A10 | READ/READ A | ILLEGAL   |
|                          | L                      | H                       | L                       | L                      | BA, CA, A10 | WRIT/WRIT A | ILLEGAL   |
|                          | L                      | L                       | H                       | H                      | BA, RA      | ACTV        | Other bank active <sup>*3</sup><br>ILLEGAL on same bank             |
|                          | L                      | L                       | H                       | L                      | BA, A10     | PRE, PALL   | ILLEGAL   |
|                          | L                      | L                       | L                       | H                      | X           | REF, SELF   | ILLEGAL   |
|                          | L                      | L                       | L                       | L                      | MODE        | MRS         | ILLEGAL   |

**Function Truth Table (Continued)**

| Current state             | $\overline{\text{CS}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | Address     | Command     | Operation   |
|---------------------------|------------------------|-------------------------|-------------------------|------------------------|-------------|-------------|---|
| Write                     | H                      | X                       | X                       | X                      | X           | DESL        | Continue burst to end                                   |
|                           | L                      | H                       | H                       | H                      | X           | NOP         | Continue burst to end                                   |
|                           | L                      | H                       | H                       | L                      | X           | BST         | Burst stop on full page                                 |
|                           | L                      | H                       | L                       | H                      | BA, CA, A10 | READ/READ A | Term burst and New read                                 |
|                           | L                      | H                       | L                       | L                      | BA, CA, A10 | WRIT/WRIT A | Term burst and New write                                |
|                           | L                      | L                       | H                       | H                      | BA, RA      | ACTV        | Other bank active <sup>*3</sup><br>ILLEGAL on same bank |
|                           | L                      | L                       | H                       | L                      | BA, A10     | PRE, PALL   | Term burst write and Precharge <sup>*2</sup>            |
|                           | L                      | L                       | L                       | H                      | X           | REF, SELF   | ILLEGAL   |
|                           | L                      | L                       | L                       | L                      | MODE        | MRS         | ILLEGAL   |
| Write with auto-Precharge | H                      | X                       | X                       | X                      | X           | DESL        | Continue burst to end and Precharge                     |
|                           | L                      | H                       | H                       | H                      | X           | NOP         | Continue burst to end and Precharge                     |
|                           | L                      | H                       | H                       | L                      | X           | BST         | ILLEGAL   |
|                           | L                      | H                       | L                       | H                      | BA, CA, A10 | READ/READ A | ILLEGAL   |
|                           | L                      | H                       | L                       | L                      | BA, CA, A10 | WRIT/WRIT A | ILLEGAL   |
|                           | L                      | L                       | H                       | H                      | BA, RA      | ACTV        | Other bank active <sup>*3</sup><br>ILLEGAL on same bank |
|                           | L                      | L                       | H                       | L                      | BA, A10     | PRE, PALL   | ILLEGAL   |
|                           | L                      | L                       | L                       | H                      | X           | REF, SELF   | ILLEGAL   |
|                           | L                      | L                       | L                       | L                      | MODE        | MRS         | ILLEGAL   |

**Function Truth Table (Continued)**

| Current state          | $\overline{\text{CS}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | Address     | Command     | Operation                 |
|------------------------|------------------------|-------------------------|-------------------------|------------------------|-------------|-------------|---------------------------|
| Refresh (auto-refresh) | H                      | X                       | X                       | X                      | X           | DESL        | Enter IDLE after $t_{RC}$ |
|                        | L                      | H                       | H                       | H                      | X           | NOP         | Enter IDLE after $t_{RC}$ |
|                        | L                      | H                       | H                       | L                      | X           | BST         | Enter IDLE after $t_{RC}$ |
|                        | L                      | H                       | L                       | H                      | BA, CA, A10 | READ/READ A | ILLEGAL                   |
|                        | L                      | H                       | L                       | L                      | BA, CA, A10 | WRIT/WRIT A | ILLEGAL                   |
|                        | L                      | L                       | H                       | H                      | BA, RA      | ACTV        | ILLEGAL                   |
|                        | L                      | L                       | H                       | L                      | BA, A10     | PRE, PALL   | ILLEGAL                   |
|                        | L                      | L                       | L                       | H                      | X           | REF, SELF   | ILLEGAL                   |
|                        | L                      | L                       | L                       | L                      | MODE        | MRS         | ILLEGAL                   |

- \* Notes :
1. H:  $V_{IH}$ , L:  $V_{IL}$ , X:  $V_{IH}$  or  $V_{IL}$ .  
The other combinations are inhibit.
  2. An interval of  $t_{RWL}$  is required between the final valid data input and the Precharge command.
  3. If  $t_{RRD}$  is not satisfied, this operation is illegal.
  4. BA:Bank Address, RA:Row Address, CA:Column Address

**From [Precharge]**

**To [DESL], [NOP] or [BST]:** When these commands are executed, the synchronous DRAM enters the IDLE state after  $t_{RP}$  has elapsed from the completion of Precharge

**From [IDLE]**

**To [DESL], [NOP], [BST], [PRE] or [PALL]:** These commands result in no operation.

**To [ACTV]:** The bank specified by the address pins and the ROW address is activated.

**To [REF], [SELF]:** The synchronous DRAM enters refresh mode (auto-refresh or self-refresh).

**To [MRS]:** The synchronous DRAM enters the mode register set cycle.

**From [ROW ACTIVE]**

**To [DESL], [NOP] or [BST]:** These commands result in no operation.

**To [READ], [READ A]:** A read operation starts. (However, an interval of  $t_{RCD}$  is required.)

**To [WRIT], [WRIT A]:** A write operation starts. (However, an interval of  $t_{RCD}$  is required.)

**To [ACTV]:** This command makes the other bank active. (However, an interval of  $t_{RRD}$  is required.) Attempting to make the currently active bank active results in an illegal command.

**To [PRE], [PALL]:** These commands set the synchronous DRAM to Precharge mode. (However, an interval of  $t_{RAS}$  is required.)

**From [READ]**

**To [DESL], [NOP]:** These commands continue read operations until the burst operation is completed.

**To [BST]:** This command stops a full-page burst.

**To [READ], [READ A]:** Data output by the previous read command continues to be output. After CAS latency, the data output resulting from the next command will start.

**To [WRIT], [WRIT A]:** These commands stop a burst read, and start a write cycle.

**To [ACTV]:** This command makes other banks bank-active. (However, an interval of  $t_{RRD}$  is required.) Attempting to make the currently active bank active results in an illegal command.

**To [PRE], [PALL]:** These commands stop a burst read, and the synchronous DRAM enters Precharge mode.

**From [READ with AUTO-Precharge]**

**To [DESL], [NOP]:** These commands continue read operations until the burst operation is completed, and the synchronous DRAM then enters Precharge mode.

**To [ACTV]:** This command makes other banks bank-active. (However, an interval of  $t_{RRD}$  is required.) Attempting to make the currently active bank active results in an illegal command.

**From [WRITE]**

**To [DESL], [NOP]:** These commands continue write operations until the burst operation is completed.

**To [BST]:** This command stops a full-page burst.

**To [READ], [READ A]:** These commands stop a burst and start a read cycle.

**To [WRIT], [WRIT A]:** These commands stop a burst and start the next write cycle.

**To [ACTV]:** This command makes the other bank active. (However, an interval of  $t_{RRD}$  is required.) Attempting to make the currently active bank active results in an illegal command.

**To [PRE], [PALL]:** These commands stop burst write and the synchronous DRAM then enters Precharge mode.

**From [WRITE with AUTO-Precharge]**

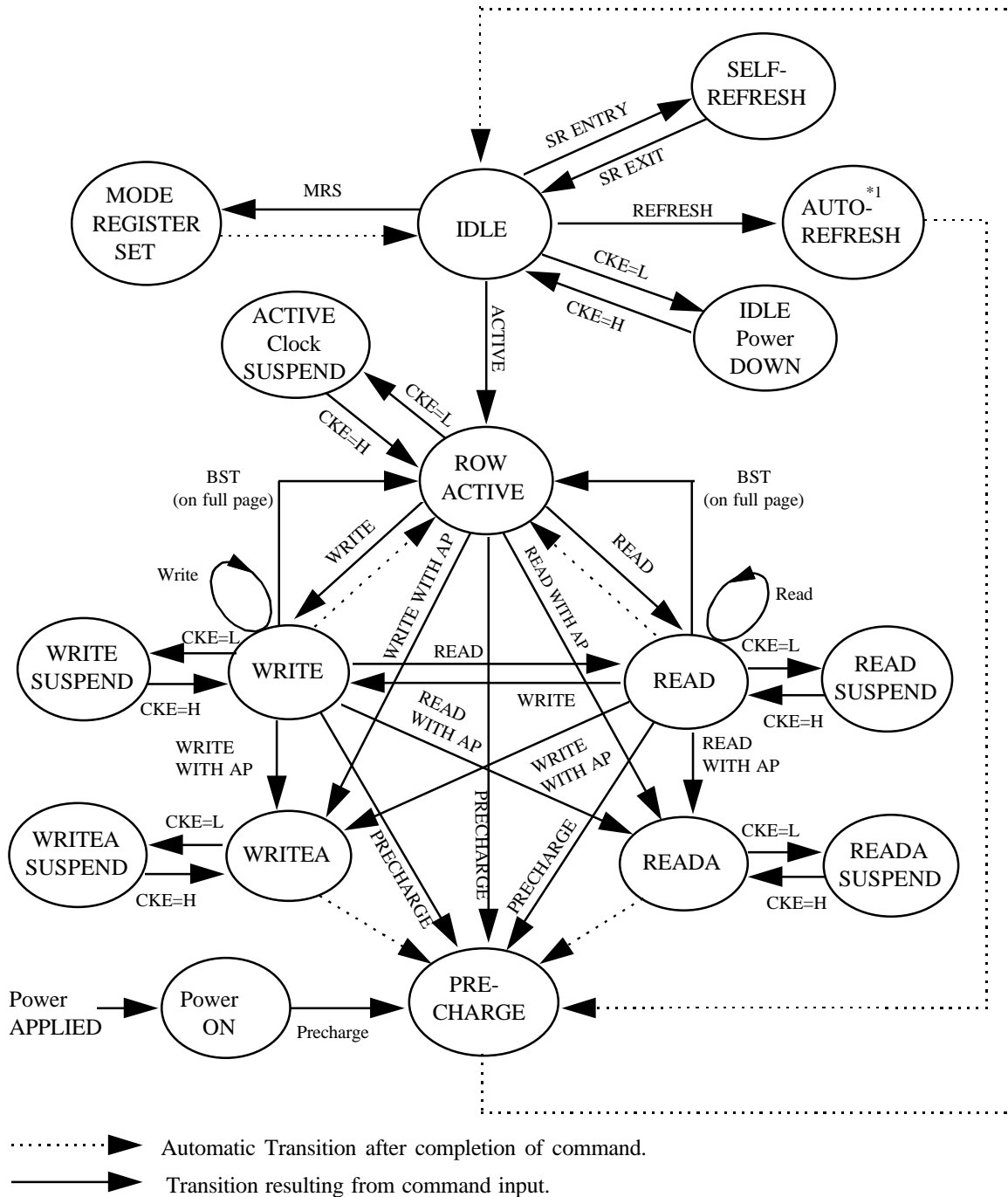
**To [DESL], [NOP]:** These commands continue write operations until the burst operation is completed, and the synchronous DRAM then enters Precharge mode.

**To [ACTV]:** This command makes the other bank active. (However, an interval of  $t_{RC}$  is required.) Attempting to make the currently active bank active results in an illegal command.

**From [REFRESH]**

**To [DESL], [NOP], [BST]:** After an auto-refresh cycle (after  $t_{RC}$ ), the synchronous DRAM automatically enters the Idle state.

### 64M SDRAM Function State Diagram



Note: 1. After the auto-refresh operation, Precharge is performed automatically and enter the IDLE state.

### Mode Register Configuration

The mode register is set by the input to the address pins (A0 to A13) during mode register set cycles. The mode register consists of five sections, each of which is assigned to address pins.

**A13, A12, A11, A10, A9, A8: (OPCODE):**

The synchronous DRAM has two types of write modes. One is the burst write mode, and the other is the single write mode. These bits specify write mode.

**Burst read and BURST WRITE:**

Burst write is performed for the specified burst length starting from the column address specified in the write cycle.

**Burst read and SINGLE WRITE:**

Data is only written to the column address specified during the write cycle, regardless of the burst length.

**A7:**

Keep this bit Low at the mode register set cycle.

**A6, A5, A4: (LMODE):**

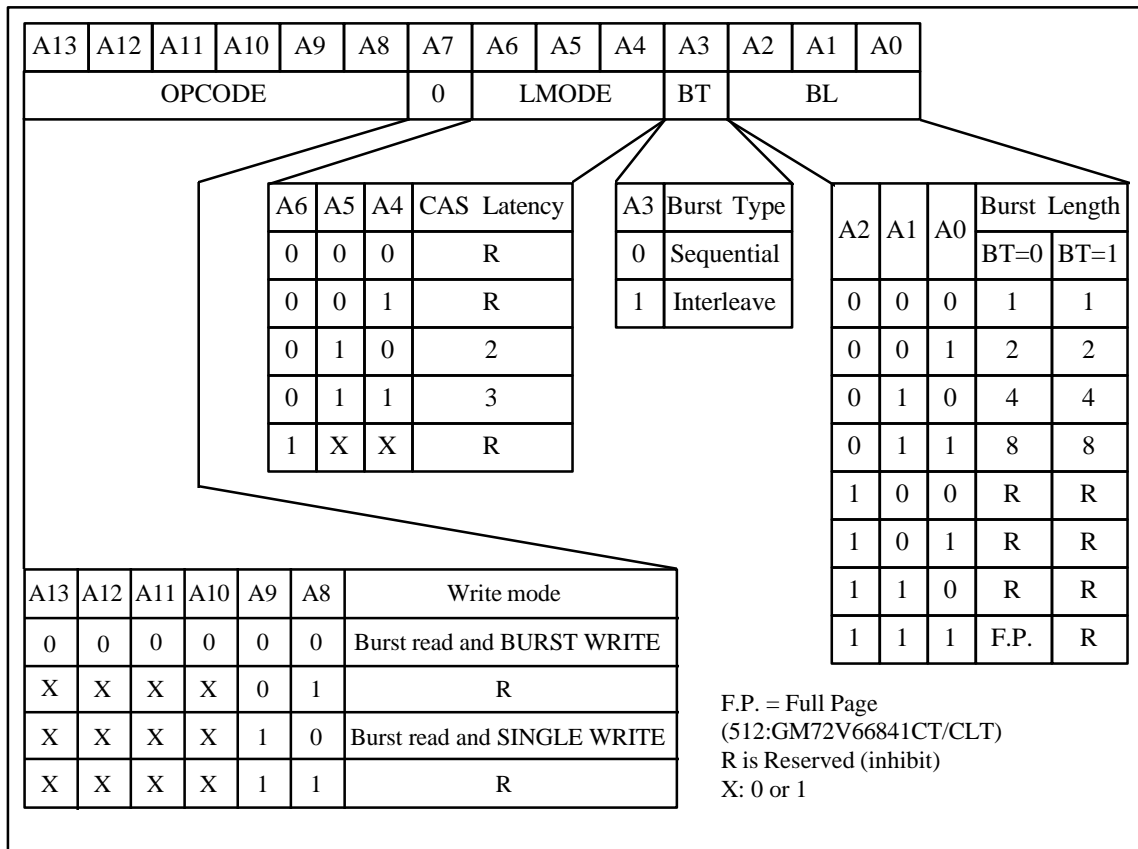
These pins specify the  $\overline{\text{CAS}}$  latency.

**A3: (BT):**

A burst type is specified. When full-page burst is performed, only "sequential" can be selected.

**A2, A1, A0: (BL):**

These pins specify the burst length.



**Burst Sequence**

| Burst Length | Starting Column Address |    |    | Addressing(decimal)           |                               |
|--------------|-------------------------|----|----|-------------------------------|-------------------------------|
|              | A2                      | A1 | A0 | Sequential                    | Interleave                    |
| 2            | V                       | V  | 0  | 0 - 1                         | 0 - 1                         |
|              | V                       | V  | 1  | 1 - 0                         | 1 - 0                         |
| 4            | V                       | 0  | 0  | 0 - 1 - 2 - 3                 | 0 - 1 - 2 - 3                 |
|              | V                       | 0  | 1  | 1 - 2 - 3 - 0                 | 1 - 0 - 3 - 2                 |
|              | V                       | 1  | 0  | 2 - 3 - 0 - 1                 | 2 - 3 - 0 - 1                 |
|              | V                       | 1  | 1  | 3 - 0 - 1 - 2                 | 3 - 2 - 1 - 0                 |
| 8            | 0                       | 0  | 0  | 0 - 1 - 2 - 3 - 4 - 5 - 6 - 7 | 0 - 1 - 2 - 3 - 4 - 5 - 6 - 7 |
|              | 0                       | 0  | 1  | 1 - 2 - 3 - 4 - 5 - 6 - 7 - 0 | 1 - 0 - 3 - 2 - 5 - 4 - 7 - 6 |
|              | 0                       | 1  | 0  | 2 - 3 - 4 - 5 - 6 - 7 - 0 - 1 | 2 - 3 - 0 - 1 - 6 - 7 - 4 - 5 |
|              | 0                       | 1  | 1  | 3 - 4 - 5 - 6 - 7 - 0 - 1 - 2 | 3 - 2 - 1 - 0 - 7 - 6 - 5 - 4 |
|              | 1                       | 0  | 0  | 4 - 5 - 6 - 7 - 0 - 1 - 2 - 3 | 4 - 5 - 6 - 7 - 0 - 1 - 2 - 3 |
|              | 1                       | 0  | 1  | 5 - 6 - 7 - 0 - 1 - 2 - 3 - 4 | 5 - 4 - 7 - 6 - 1 - 0 - 3 - 2 |
|              | 1                       | 1  | 0  | 6 - 7 - 0 - 1 - 2 - 3 - 4 - 5 | 6 - 7 - 4 - 5 - 2 - 3 - 0 - 1 |
|              | 1                       | 1  | 1  | 7 - 0 - 1 - 2 - 3 - 4 - 5 - 6 | 7 - 6 - 5 - 4 - 3 - 2 - 1 - 0 |

\* Notes : V : Valid Address



## Operation of GM72V661641CT/CLT, GM72V66841CT/CLT, GM72V66441CT/CLT Series

### Read / Write Operation

**Bank active:** Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACTV) command. Bank 0, bank 1, bank 2 or bank 3 is activated according to the status of the A12/A13 pin, and the row address (AX0 to AX11) is activated by the A0 to A11 pins at the bank active command cycle. An interval of  $t_{RCD}$  is required between the bank active command input and the following read/write command input.

**Read operation:** A read operation starts when a read command is input. Output buffer becomes Low-Z in the  $\overline{CAS}$  Latency - 1) cycle after read command set. GM72V66841CT/CLT can perform a burst read operation.

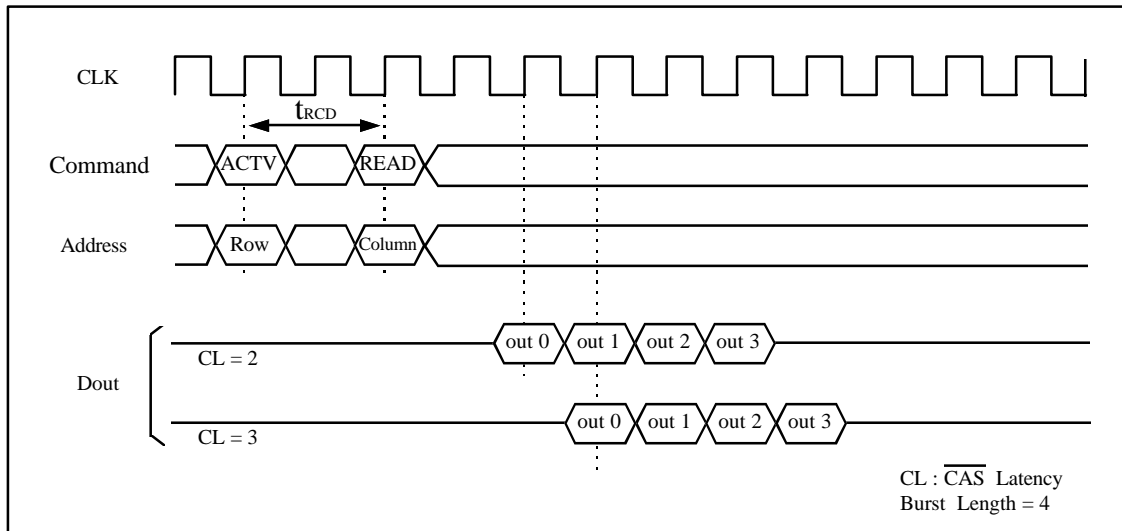
The burst length can be set to 1, 2, 4, 8 or full page(512;GM72V66841CT/CLT). The start address for a burst read is specified by the column address (AY0 to AY8; GM72V66841CT/CLT) and the bank select address (A12/A13) at the read command set cycle. In a read operation, data output starts after the number of cycles specified by the  $\overline{CAS}$  Latency. The  $\overline{CAS}$  Latency can be set to 2 or 3.

When the burst length is 1, 2, 4, or 8, the Dout buffer automatically becomes High-Z at the next cycle after the successive burst-length data has been output.

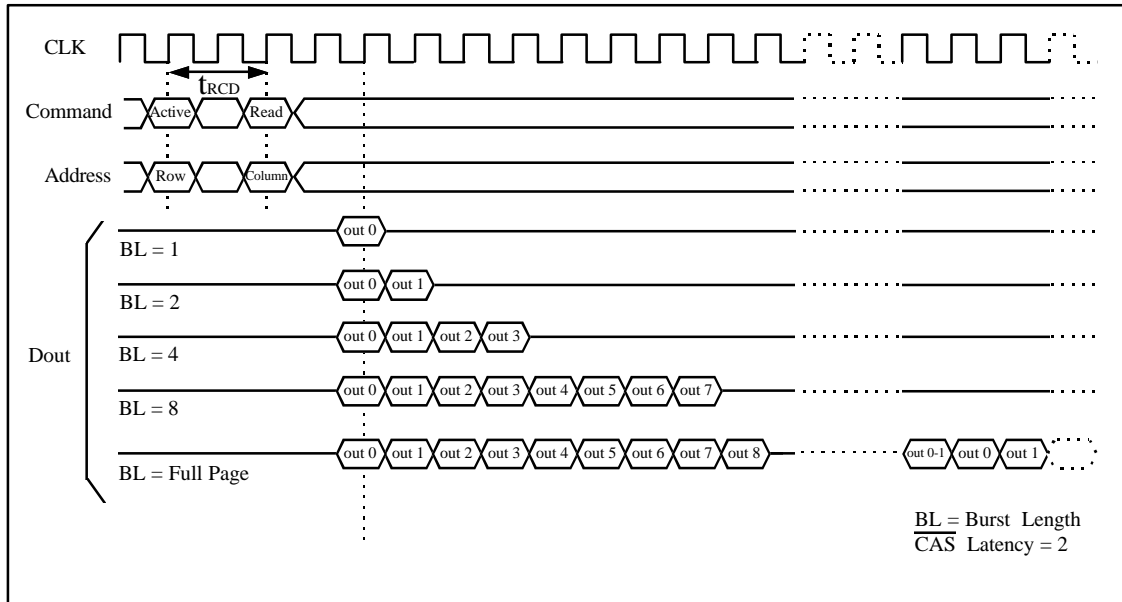
When the burst length is full-page (512;GM72V66841CT/CLT) data is repeatedly output until the burst stop command is input.

The  $\overline{CAS}$  latency and burst length must be specified at the mode register.

$\overline{CAS}$  Latency



Burst Length



**Write Operation**

Burst write or single write mode is selected by the OPCODE(A13, A12,A11, A10, A9, A8) of the mode register.

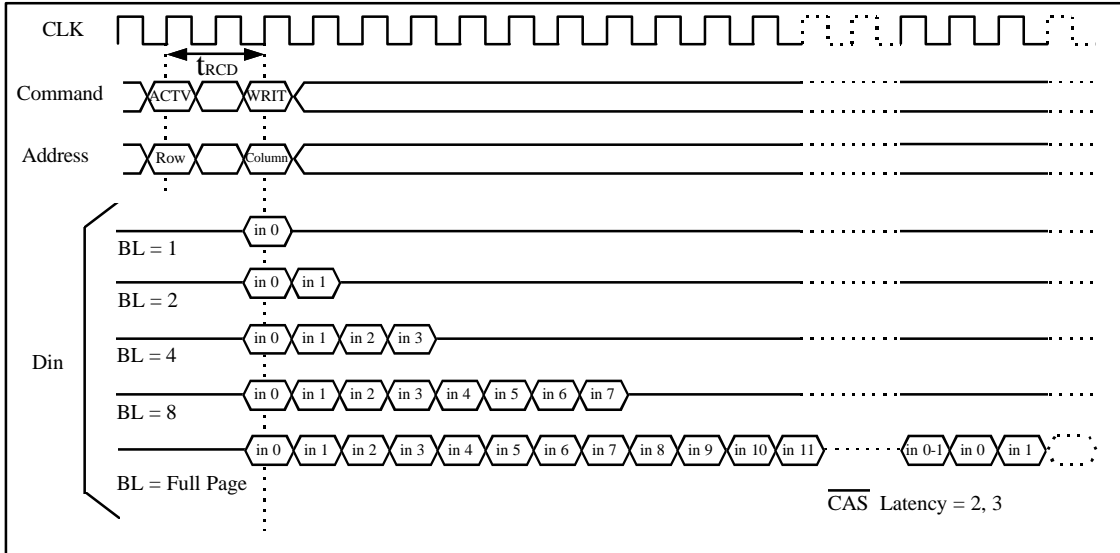
**1. Burst write:**

A burst write operation is enabled by setting OPCODE(A9, A8) to (0, 0). A burst write starts in the same cycle as a write command set. (The latency of data input is 0.) The burst length can be set to 1, 2, 4, 8 and full page, like burst read operations. The write start address is specified by the column address (AY0 to AY8; GM72V66841CT/CLT) and the bank select address (A12/A13) at the write command set cycle.

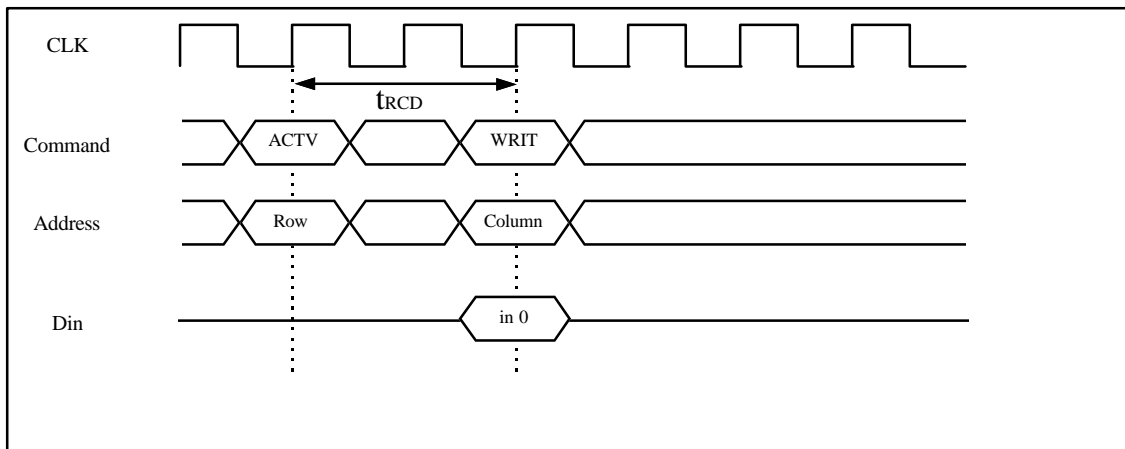
**2. Single write:**

A single write operation is enabled by setting OPCODE (A9, A8) to (1, 0). In a single write operation, data is only written to the column address (AY0 to AY8; GM72V66841CT/CLT) and the bank select address (A12/A13) specified by the write command set cycle without regard to the burst length setting. (The latency of data input is 0.)

Burst Write



Single Write



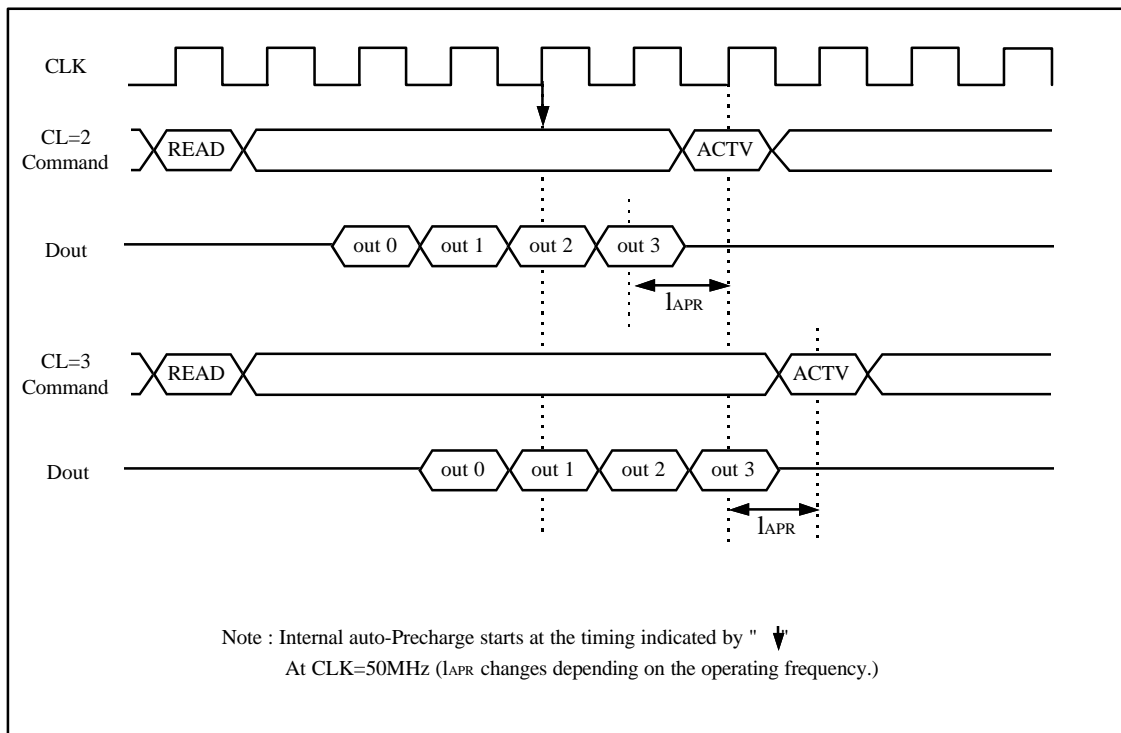
**Auto Precharge**

**Read with auto-Precharge:** In this operation, since Precharge is automatically performed after completing a read operation, a Precharge command need not be executed after each read operation.

The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval defined by  $t_{APR}$  is required before execution of the next command.

| $\overline{\text{CAS}}$ Latency | Precharge start cycle                   |
|---------------------------------|---|
| 3                               | 2 cycle before the final data is output |
| 2                               | 1 cycle before the final data is output |

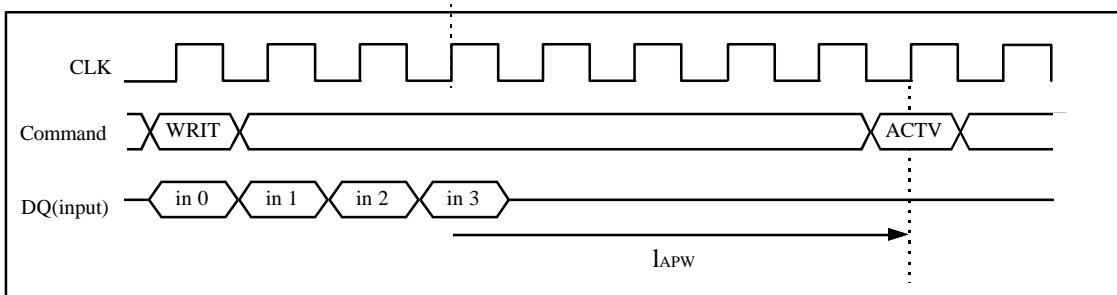
**Burst Read with Auto-Precharge**



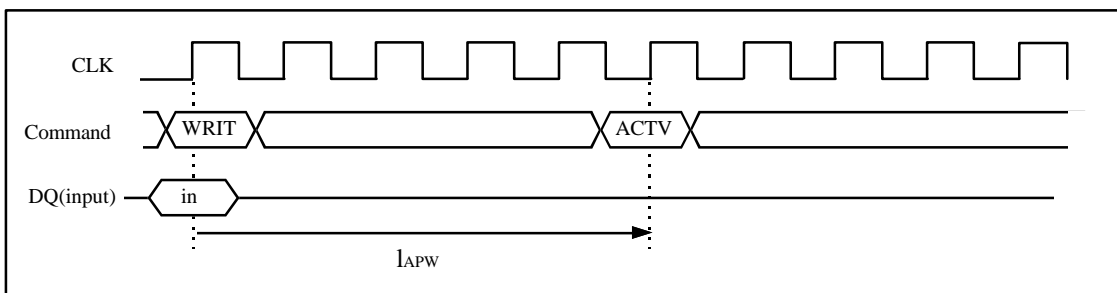
**Write with auto-Precharge:** In this operation, since Precharge is automatically performed after completing a burst write or single write operation, a Precharge command need not be executed after each write operation.

The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval of  $t_{APW}$  is required between the final valid data input and input of the next command.

Burst Write (Burst Length = 4)



Single Write



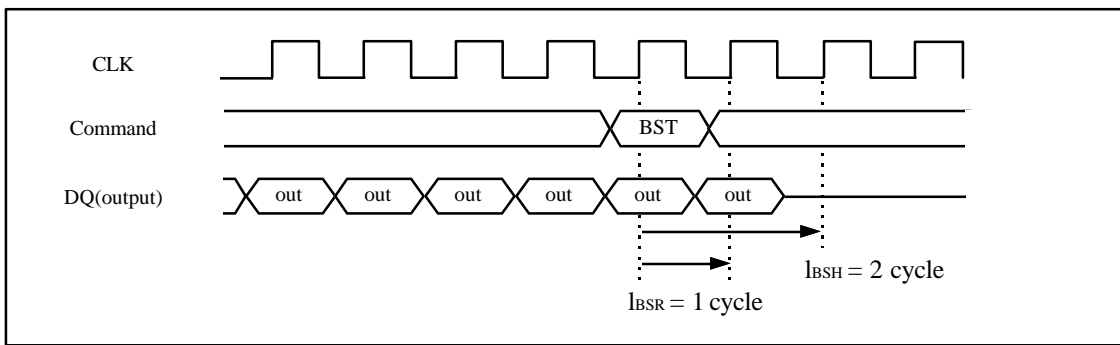
**Full-page Burst Stop**

**Burst stop command during burst read:** The burst stop (BST) command is used to stop data output during a full-page burst. The BST command sets the output buffer to High-Z and stops the full-page burst read.

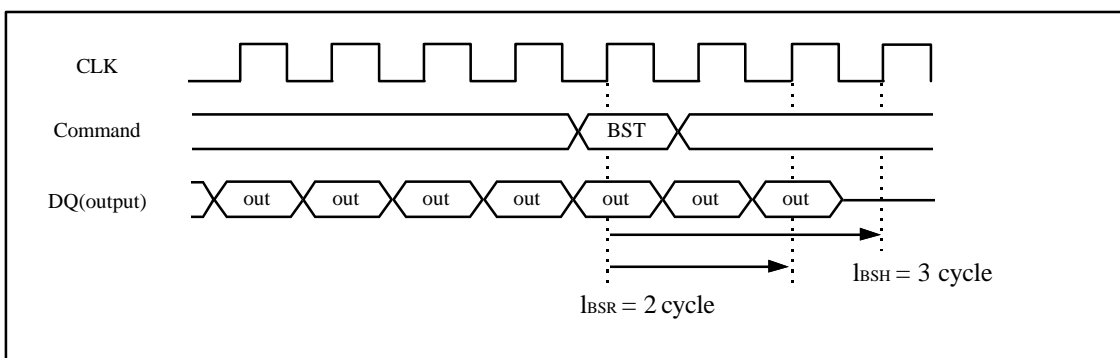
The timing from command input to the last data changes depending on the  $\overline{\text{CAS}}$  latency setting. In addition, the BST command is valid only during full-page burst mode, and is invalid with burst lengths 1, 2, 4, and 8.

| $\overline{\text{CAS}}$ Latency | BST to valid data | BST to high impedance |
|---------------------------------|-------------------|-----------------------|
| 2                               | 1                 | 2                     |
| 3                               | 2                 | 3                     |

$\overline{\text{CAS}}$  Latency=2, Burst Length = full page



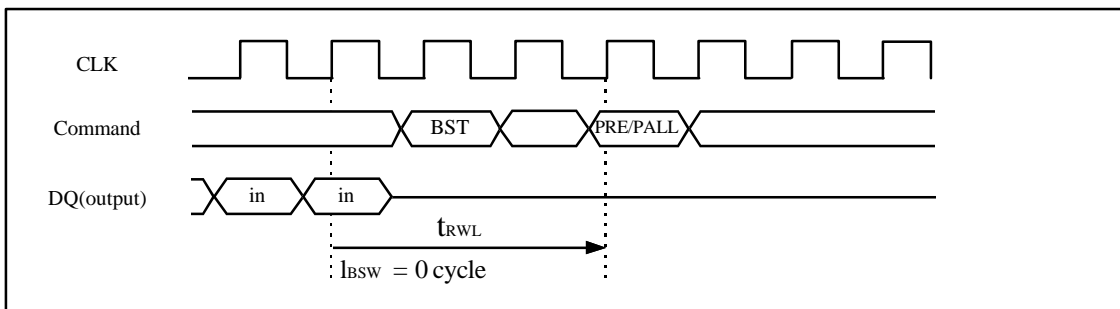
$\overline{\text{CAS}}$  Latency = 3, Burst Length = full page



**Burst stop command at burst write:** The burst stop command (BST command) is used to stop data input during a full-page burst write. No data is written in the same cycle as the BST command, and in subsequent cycles.

In addition, the BST command is only valid during full-page burst mode, and is invalid with burst lengths of 1, 2, 4, and 8. And an interval of  $t_{RWL}$  is required between the last data-in and the next Precharge command.

Burst Length = full page



**Command Intervals**

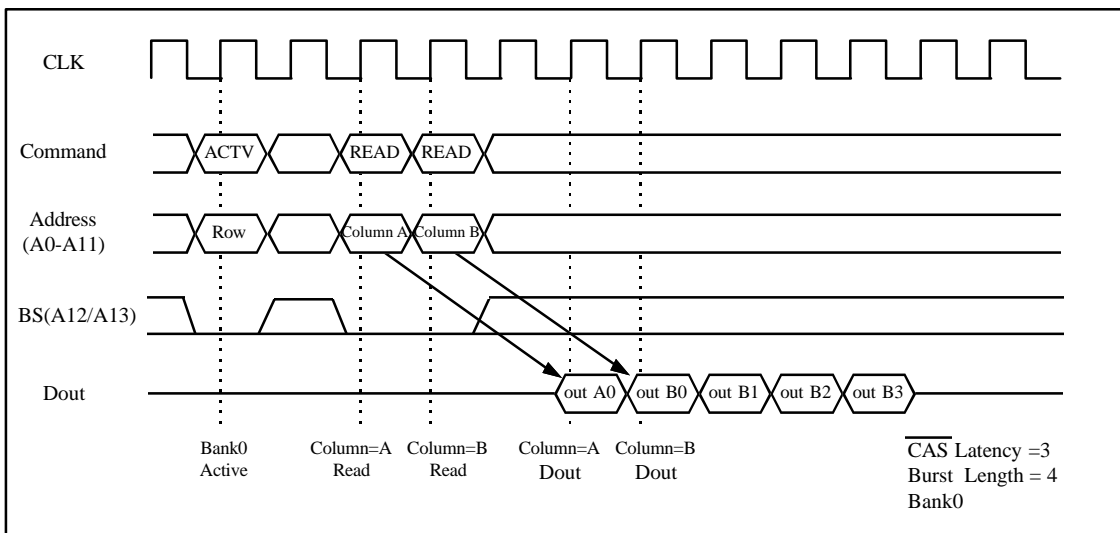
Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

**Read command to Read command interval:**

**1. Same bank, same ROW address:**

When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 cycle.

READ to READ Command Interval (Same Row Address in Same Bank)



**2. Same bank, different ROW address:**

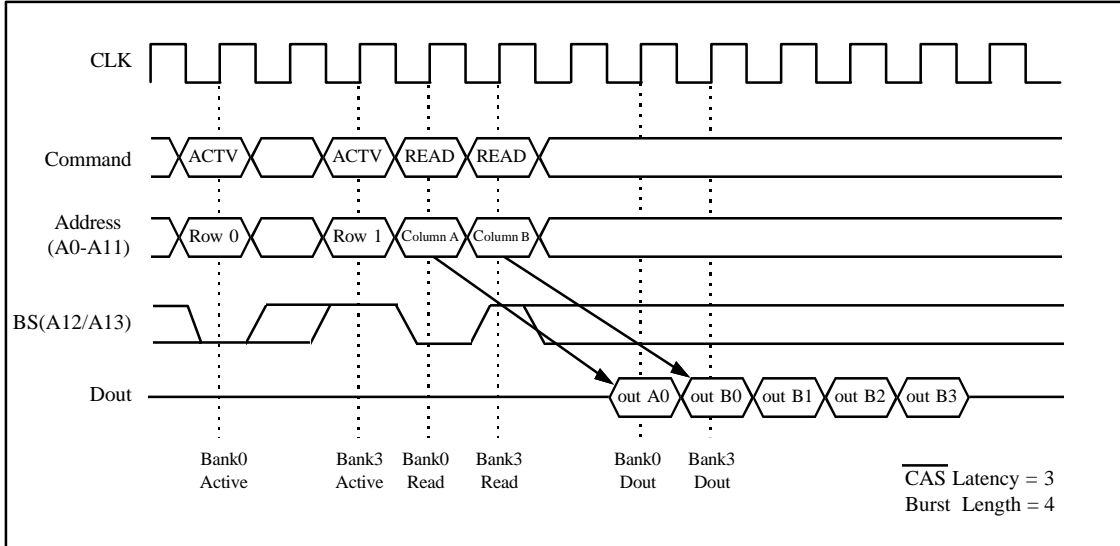
When the ROW address changes on same bank, consecutive read commands cannot be executed; it is necessary to separate the two read commands with a Precharge command and a bank-active command.

**3. Different bank:**

When the bank changes, the second read can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.



READ to READ Command Interval (different bank)



**Command Intervals**

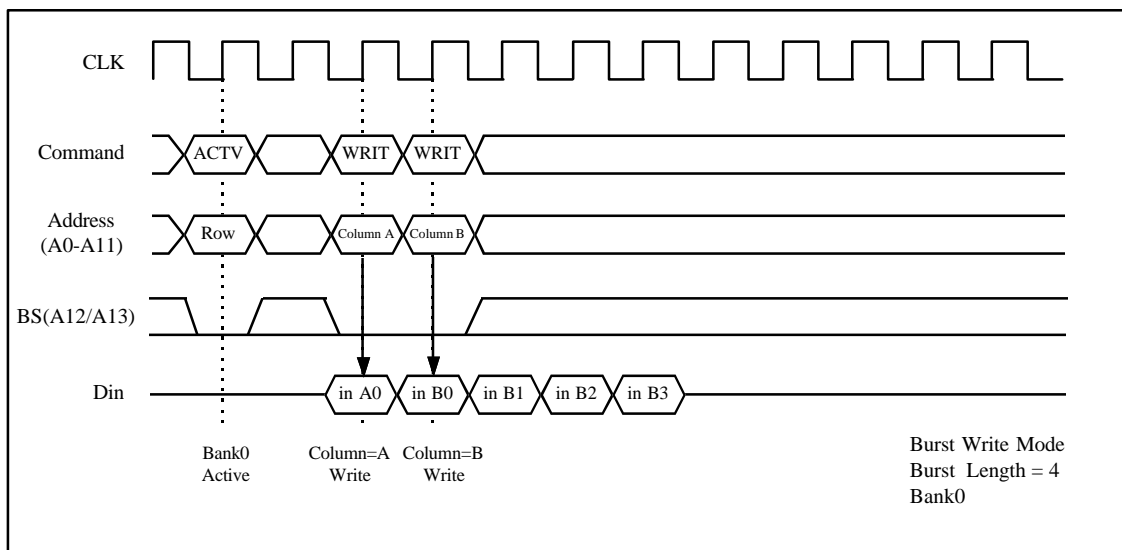
In the case of burst writes, the second write command has priority.

**Write command to Write command interval:**

**1. Same bank, same ROW address:**

When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after an interval of no less than 1 cycle.

WRITE to WRITE Command Interval (same ROW address in same bank)



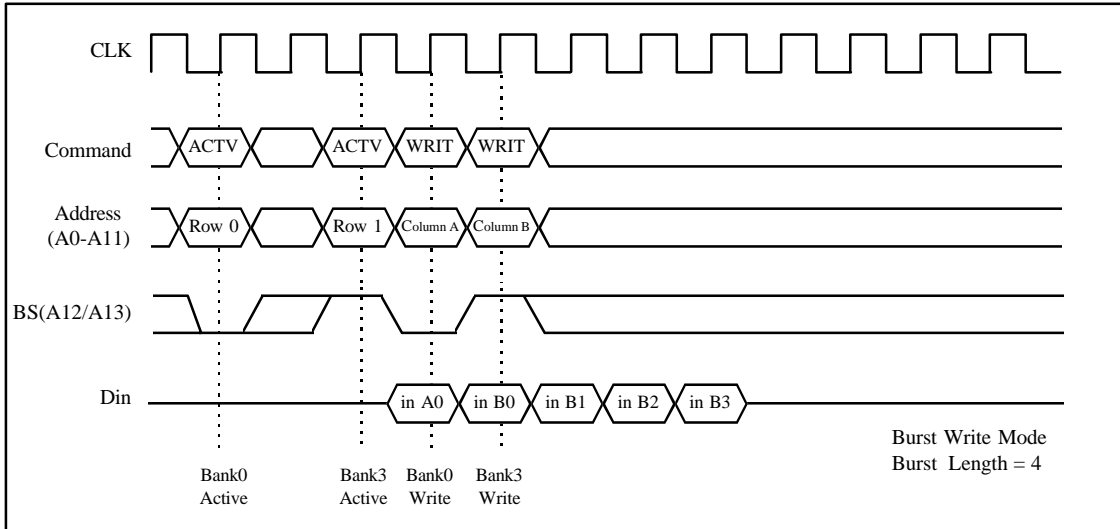
**2. Same bank, different ROW address:**

When the ROW address changes, consecutive read commands cannot be executed; it is necessary to separate the two write commands with a Precharge command and a bank-active command.

**3. Different bank:**

When the bank changes, the second write can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. In the case of burst write, the second write command has priority.

WRITE to WRITE Command Interval (different bank)



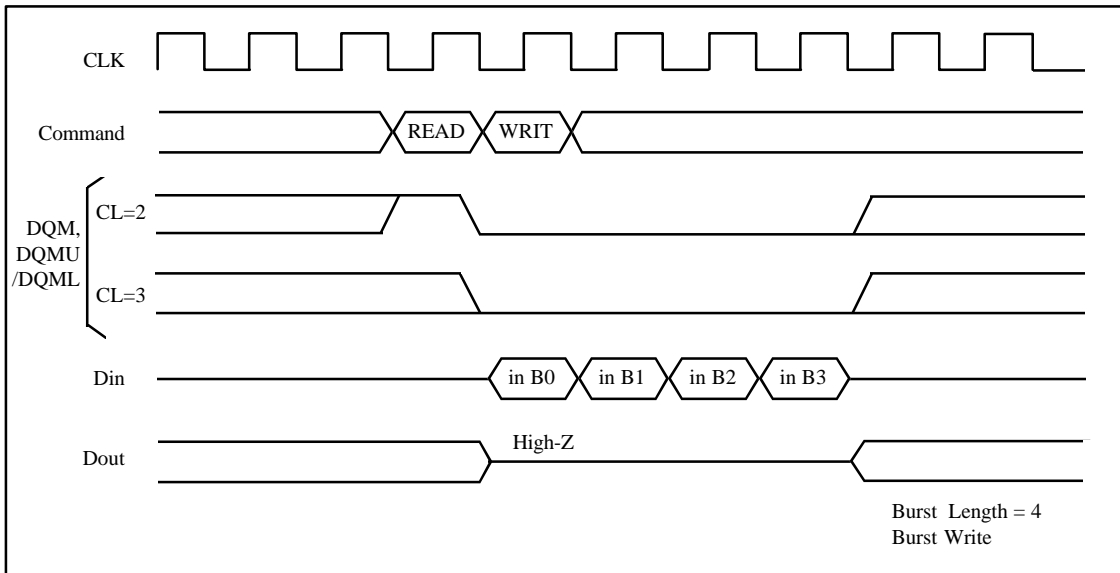
**Read command to Write command interval:**

**1. Same bank, same Row address:**

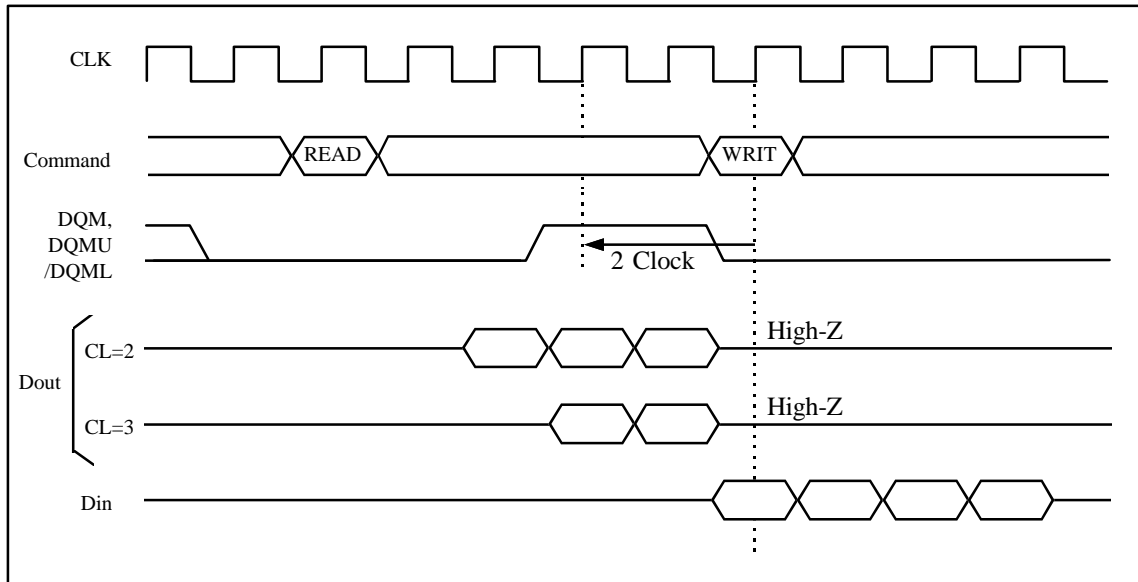
When the write command is executed at the same ROW address of the same bank as the preceding

read command, the write command can be performed after an interval of no less than 1 cycle. However, DQM, DQMU/DQML must be set High-Z so that the output buffer becomes High-Z before data input.

READ to WRITE Command Interval (1)



READ to WRITE Command Interval (2)



**2. Same bank, different ROW address:**

When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a Precharge command or a bank-active command.

**3. Different bank:**

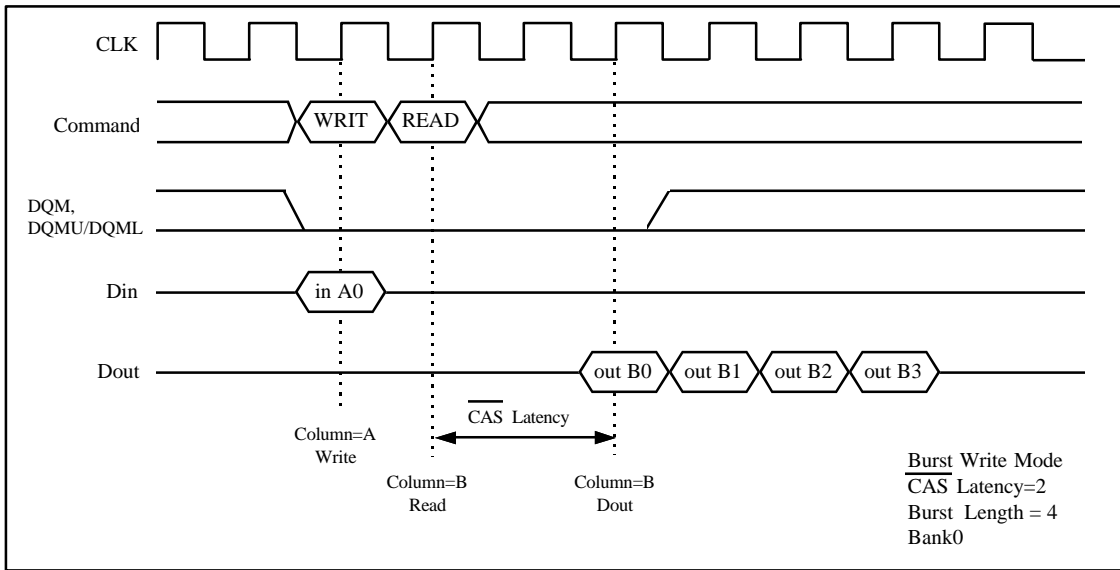
When the bank changes, the write can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, DQM, DQMU/DQML must be set High so that the output buffer becomes High-Z before data input.

**Write Command to Read Command Interval:**

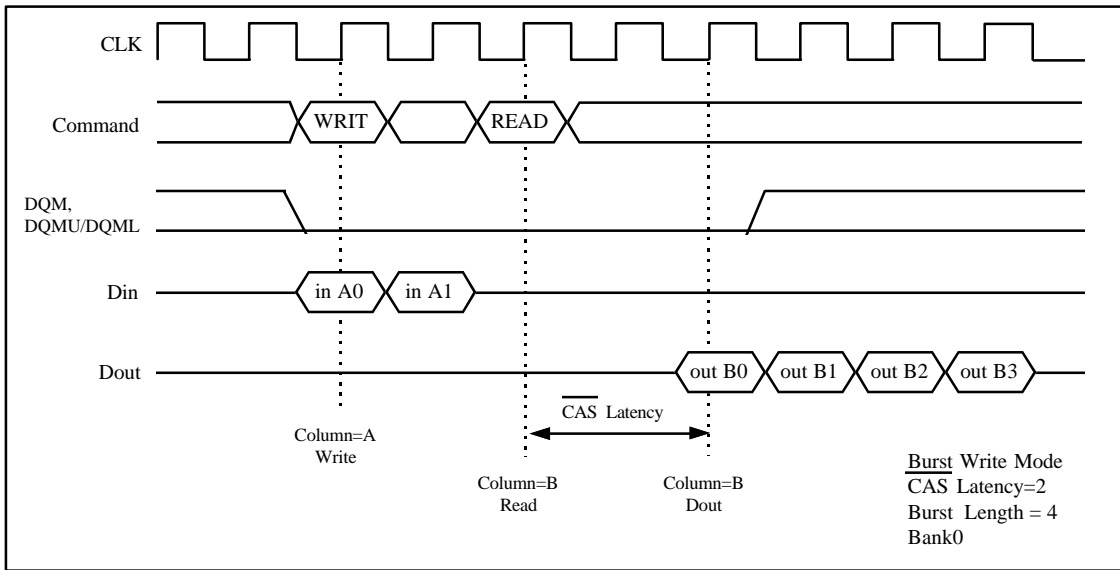
1. **Same bank, same Row address:** When the read command is executed at the same ROW address of the same bank as the preceding write command, the write command can be performed after an interval of no less than 1 cycle.

However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed.

WRITE to READ Command Interval (1)



WRITE to READ Command Interval (2)



**2. Same bank, different ROW address:** When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a Precharge command and a bank-active command.

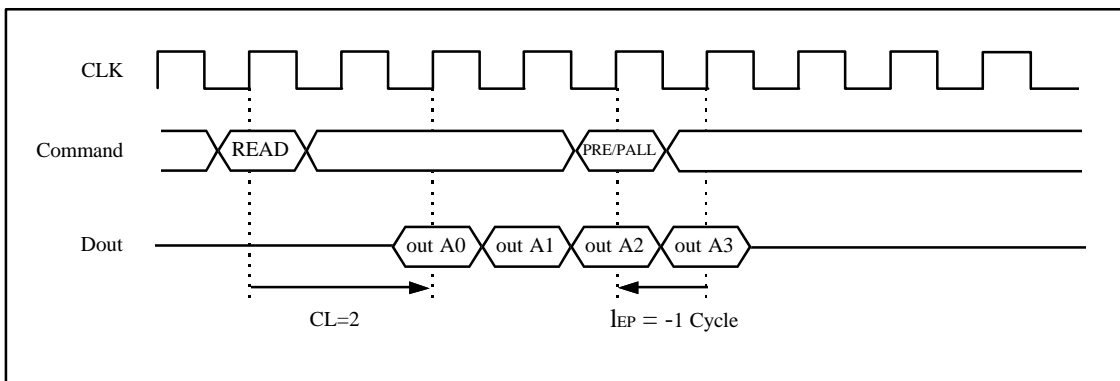
**3. Different bank:** When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed(as in the case of the same bank and the same address).

**Read command to Precharge interval (same bank):** When the Precharge command is executed for the same bank as the read command that preceded it, the minimum interval between the two commands is one cycle. However, since the output buffer then becomes High-Z after the cycles defined by  $t_{HZP}$ , there is a possibility that burst read data output will be interrupted, if the Precharge command is input during burst read.

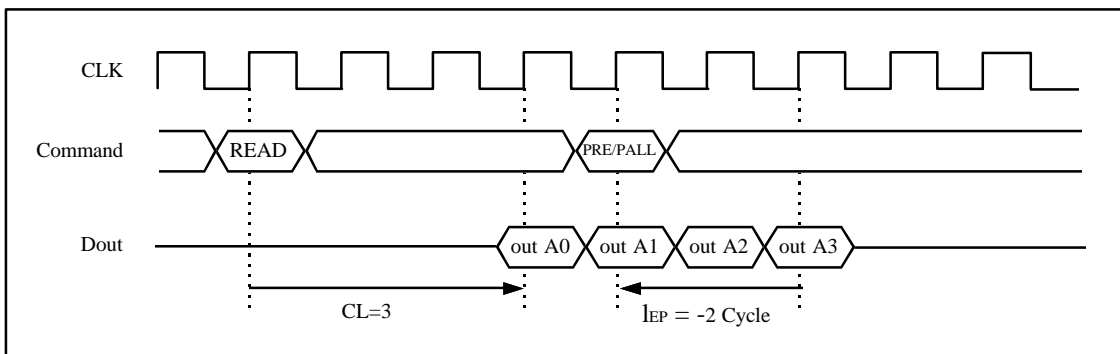
To read all data by burst read, the cycles defined by  $t_{EP}$  must be assured as an interval from the final data output to Precharge command execution.

READ to Precharge Command Interval (same bank) : To output all data

CAS Latency = 2, Burst Length = 4

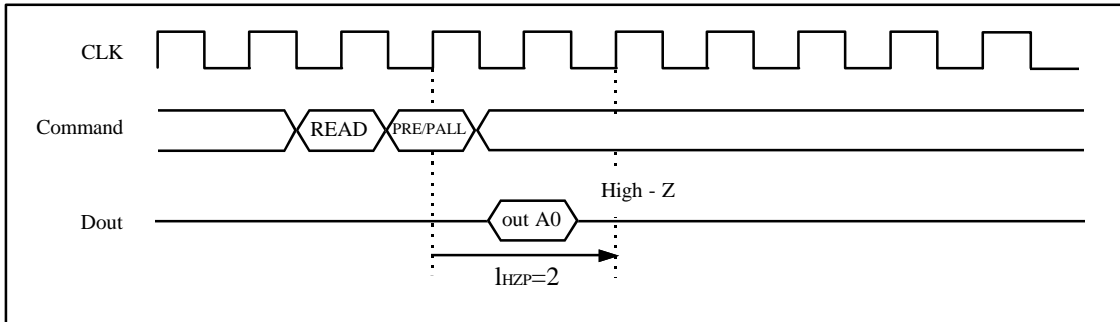


CAS Latency = 3, Burst Length = 4

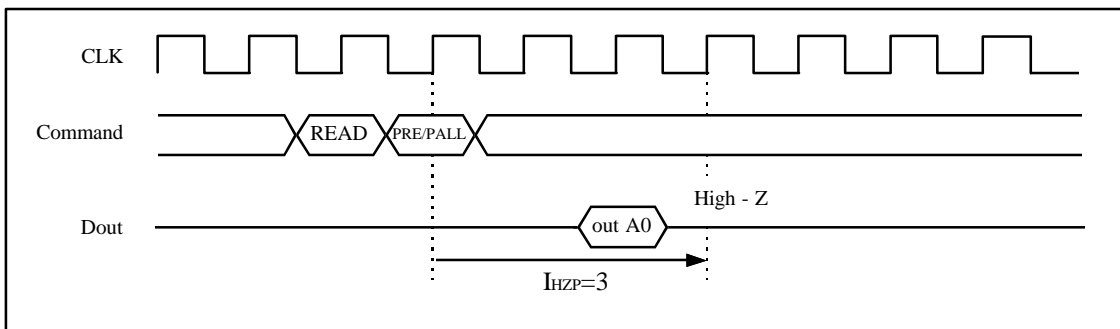


READ to Precharge Command Interval (same bank) : To stop output data

$\overline{\text{CAS}}$  Latency = 2, Burst Length = 1, 2, 4, 8



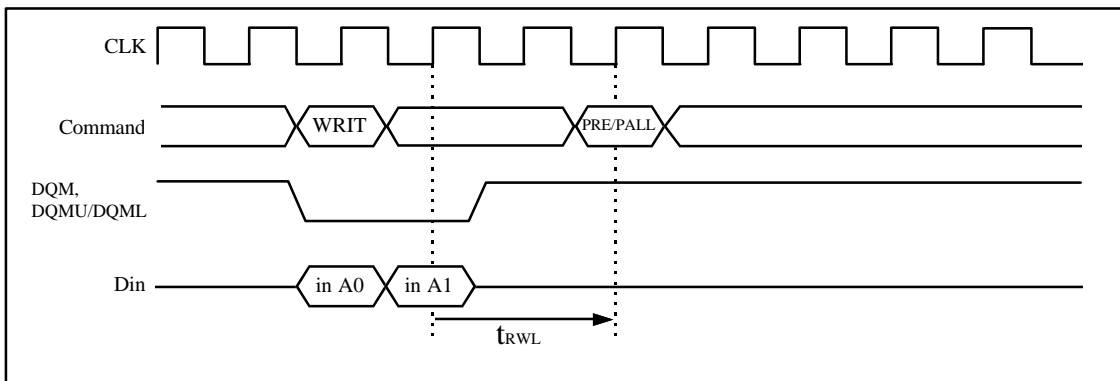
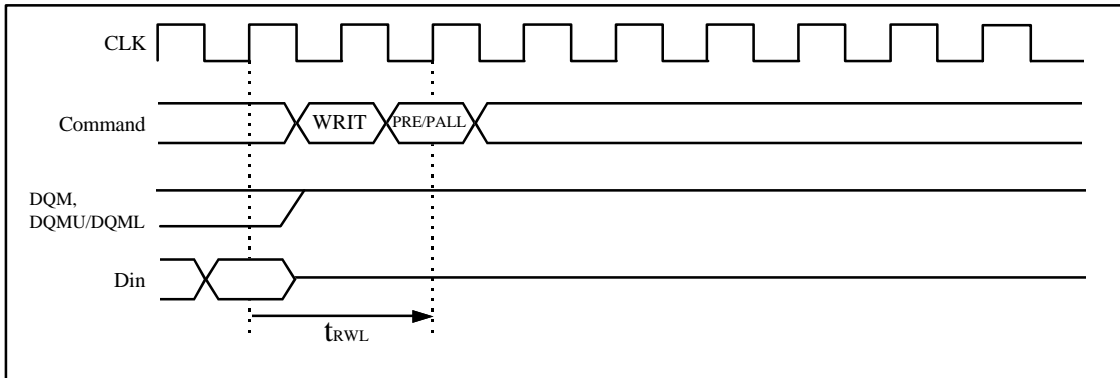
$\overline{\text{CAS}}$  Latency = 3, Burst Length = 1, 2, 4, 8



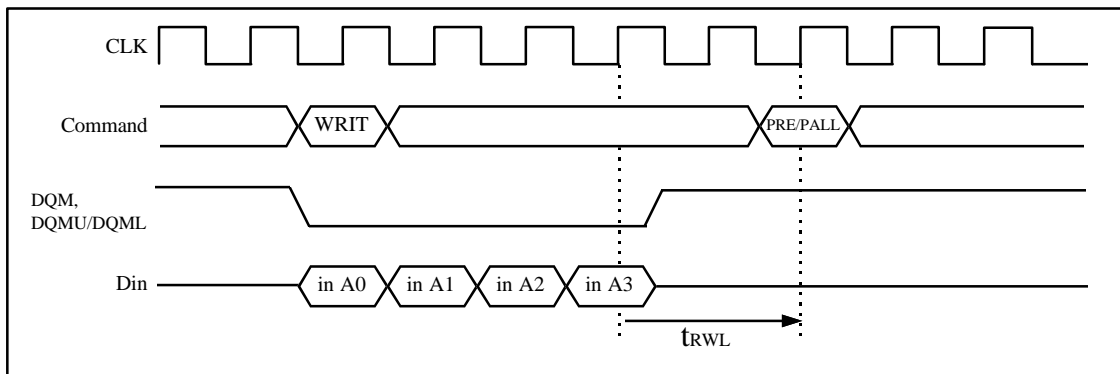
**Write Command to Precharge Command Interval (same bank):** When the Precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 cycle.

However, if the burst write operation is unfinished, the input data must be masked by means of DQM, DQMU/DQML for assurance of the cycle defined by  $t_{RWL}$ .

Burst Length = 4 ( To stop write operation)



Burst Length = 4 (To write all data)



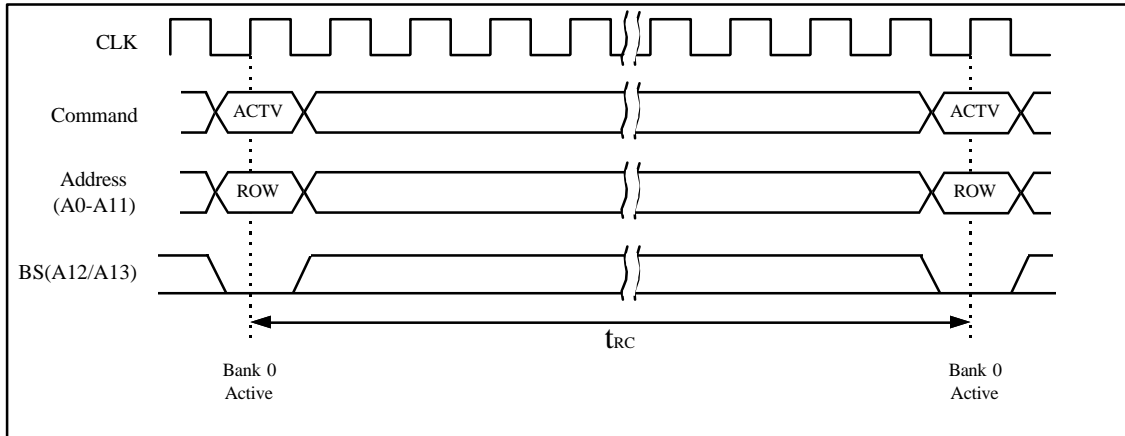


**Bank Active Command Interval**

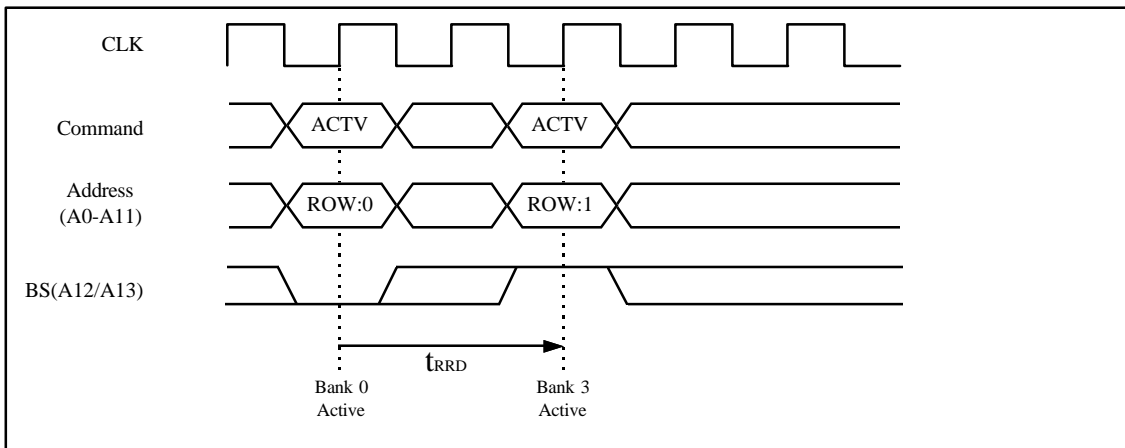
1. **Same bank:** The interval between the two bank-active commands must be no less than  $t_{RC}$ .

2. **In the case of different bank-active commands:** The interval between the bank-active commands must be no less than  $t_{RRD}$ .

Bank Active to Bank Active Command Interval for Same Bank

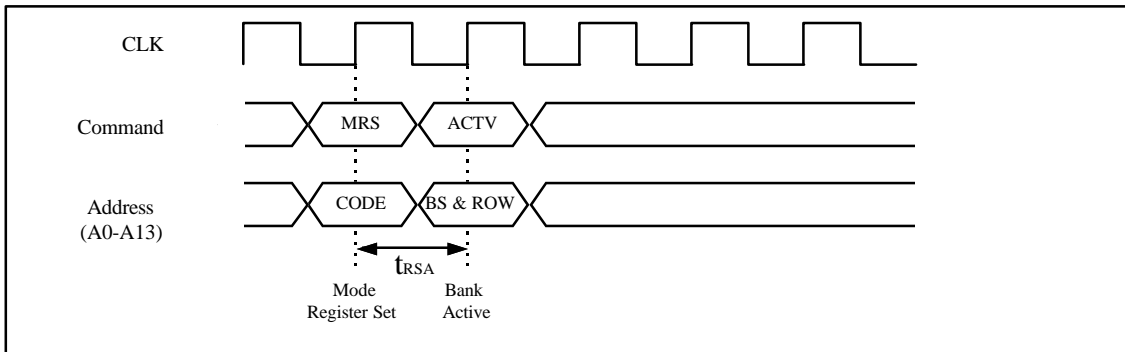


Bank Active to Bank Active for different bank



**Mode Register Set to Bank-Active Command**

**Interval :** The interval between setting the mode register and executing a bank-active command must be no less than  $t_{RSA}$ .



**DQM Control (GM72V661641CT/CLT)**

The DQMU and DQML mask the upper and lower bytes of DQ data, respectively. The timing of DQMU/DQML is different during reading and writing.

**Reading:** When data is read, the output buffer can be controlled by DQMU/DQML. By setting DQMU/DQML to Low, the output buffer becomes Low-Z, enabling data output. By setting DQMU/DQML to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of DQMU/DQML during reading is 2.

**Writing:** Input data can be masked by DQMU/DQML. By setting DQMU/DQML to Low, data can be written. In addition, when DQMU/DQML is set to High, the corresponding data is not written, and the previous data is held. The latency of DQMU/DQML during writing is 0.

**DQM Control**

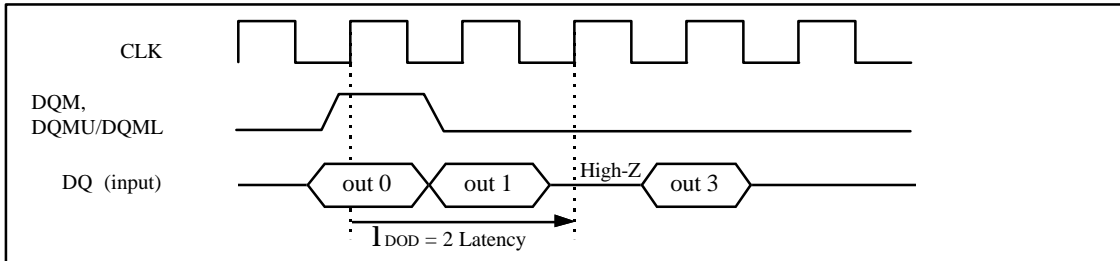
(GM72V66841CT/CLT,GM72V66441CT)

The DQM mask DQ data. The timing of DQM is different during reading and writing.

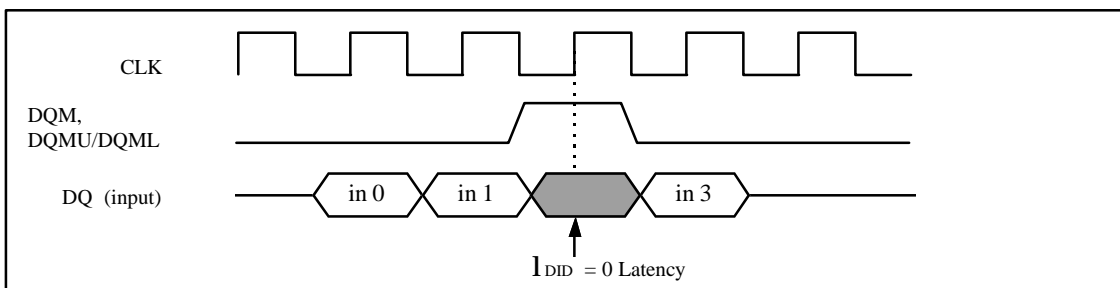
**Reading:** When data is read, the output buffer can be controlled by DQM. By setting DQM to Low, the output buffer becomes Low-Z, enabling data output. By setting DQM to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of DQM during reading is 2.

**Writing:** Input data can be masked by DQM. By setting DQM to Low, data can be written. In addition, when DQM is set to High, the corresponding data is not written, and the previous data is held. The latency of DQM during writing is 0.

Reading



Writing



**Refresh****Auto refresh:**

All the banks must be Precharged before executing an auto-refresh command. Since the auto-refresh command updates the internal counter every time it is executed and determines the banks and the ROW addresses to be refreshed, external address specification is not required. The refresh cycle is 4,096 cycles/64ms. (4,096 cycles are required to refresh all the ROW addresses.) The output buffer becomes High-Z after auto-refresh start. In addition, since a Precharge has been completed by an internal operation after the auto-refresh, an additional Precharge operation by the Precharge command is not required.

**Self refresh:**

After executing a self-refresh command, the self-refresh operation continues while CKE is held Low. During self-refresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. If you use distributed auto-refresh mode with 15.6us interval in normal read/write cycle, auto-refresh should be executed within 15.6 us immediately after exiting from and before entering into self refresh mode. If you use address refresh or burst auto-refresh mode in normal read/write cycle, 4096 cycles of distributed auto-refresh with 15.6us interval should be executed within 64 ms immediately after exiting from and before entering into self refresh mode.

**Others****Power down mode:**

The synchronous DRAM enters Power down mode when CKE goes Low in the IDLE state. In Power down mode, Power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE is held Low. In addition, by setting CKE to High, the synchronous DRAM exits from the Power down mode, and command input is enabled from the next cycle. In this mode, internal refresh is not performed.

**Clock suspend (Active Power down) mode:**

By driving CKE to Low during a bank-active or read/write operation, the synchronous DRAM enters Clock suspend mode. During Clock suspend mode, external input signals are ignored and the internal state is maintained. When CKE is driven High, the synchronous DRAM terminates Clock suspend mode, and command input is enabled from the next cycle. For details, refer to the "CKE Truth Table".

**Power-up sequence:**

During Power-up sequence, the DQM and the CKE must be set to High. When 200 $\mu$ s has past after Power on, all banks must be Precharged using the Precharge command. After  $t_{RP}$  delay, set 8 or more auto refresh commands. And set the mode register set command to initialize the mode register.

### Absolute Maximum Ratings

| Parameter                          | Symbol           | Value   | Unit | Note |
|------------------------------------|------------------|---|------|------|
| Voltage on any pin relative to Vss | V <sub>T</sub>   | -0.5 to V <sub>CC</sub> +0.5<br>(≤ 4.6 (max)) | V    | 1    |
| Supply voltage relative to Vss     | V <sub>CC</sub>  | -0.5 to +4.6                                  | V    | 1    |
| Short circuit output current       | I <sub>OUT</sub> | 50  | mA   |      |
| Power dissipation                  | P <sub>T</sub>   | 1.0   | W    |      |
| Operating temperature              | T <sub>opr</sub> | 0 to +70                                      | C    |      |
| Storage temperature                | T <sub>stg</sub> | -55 to +125                                   | C    |      |

Notes : 1. Respect to Vss

### Recommended DC Operating Conditions (T<sub>a</sub> = 0 to + 70C)

| Parameter          | Symbol                             | Min  | Max                   | Unit | Note |
|--------------------|------------------------------------|------|-----------------------|------|------|
| Supply voltage     | V <sub>CC</sub> , V <sub>CCQ</sub> | 3.0  | 3.6                   | V    | 1    |
|                    | V <sub>SS</sub> , V <sub>SSQ</sub> | 0    | 0                     | V    |      |
| Input high voltage | V <sub>IH</sub>                    | 2.0  | V <sub>CC</sub> + 0.3 | V    | 1, 2 |
| Input low voltage  | V <sub>IL</sub>                    | -0.3 | 0.8                   | V    | 1,3  |

- Notes : 1. All voltage referred to Vss.  
 2. V<sub>IH</sub> (max) = 4.6V for pulse width ≤ 5ns  
 3. V<sub>IL</sub> (min) = -1.5V for pulse width ≤ 5ns

**DC Characteristics** (Ta = 0 to 70C, VCC, VCCQ = 3.3 V +/- 0.3 V, VSS, VSSQ = 0 V)

| Parameter  | Symbol    | - 7K | - 7J | - 8 | - 10K | Unit | Test conditions   | Notes                           |       |
|--|-----------|------|------|-----|-------|------|---|---------------------------------|-------|
|  |           | Max  | Max  | Max | Max   |      |   |                                 |       |
| Operating current  | ICC1      | 80   | 80   | 80  | 70    | mA   | Burst length= 1<br>t <sub>RC</sub> = min                              | 1, 2, 3                         |       |
| Standby current in power down                                  | ICC2P     | 2    | 2    | 2   | 2     | mA   | CKE = V <sub>IL</sub> ,<br>t <sub>CK</sub> = 12 ns                    | 5                               |       |
| Standby current in power down (input signal stable)            | ICC2PS    | 2    | 2    | 2   | 2     | mA   | CKE=V <sub>IL</sub> ,<br>t <sub>CK</sub> = Infinity                   | 6                               |       |
|  |           | 0.4  | 0.4  | 0.4 | 0.4   |      |   | 6,8                             |       |
| Standby current in non power down (CAS Latency=2)              | ICC2N     | 15   | 15   | 15  | 15    | mA   | CKE,CS = V <sub>IH</sub> ,<br>t <sub>CK</sub> = 12ns                  | 4                               |       |
|  |           | 10   | 10   | 10  | 10    |      |   | 4,8                             |       |
| Standby current in non power down (input signal stable)        | ICC2NS    | 5    | 5    | 5   | 5     | mA   | CKE = V <sub>IH</sub> ,<br>t <sub>CK</sub> = Infinity                 | 4                               |       |
| Active standby current in power down                           | ICC3P     | 6    | 6    | 6   | 6     | mA   | CKE = V <sub>IL</sub> ,<br>t <sub>CK</sub> = 12 ns,<br>DQ = High-Z    | 1,2,5                           |       |
|  |           | 5    | 5    | 5   | 5     |      |   | 1,2,5,8                         |       |
| Active standby current in power down (input signal stable)     | ICC3PS    | 5    | 5    | 5   | 5     | mA   | CKE = V <sub>IL</sub> ,<br>t <sub>CK</sub> = Infinity                 | 2,6                             |       |
|  |           | 4    | 4    | 4   | 4     |      |   | 2,6,8                           |       |
| Active standby current in non power down                       | ICC3N     | 30   | 30   | 30  | 30    | mA   | CKE,CS = V <sub>IH</sub> ,<br>t <sub>CK</sub> = 12 ns,<br>DQ = High-Z | 1,2,4                           |       |
|  |           | 25   | 25   | 25  | 25    |      |   | 1,2,4,8                         |       |
| Active standby current in non power down (input signal stable) | ICC3NS    | 20   | 20   | 20  | 20    | mA   | CKE = V <sub>IH</sub> ,<br>t <sub>CK</sub> = Infinity                 | 2,9                             |       |
|  |           | 10   | 10   | 10  | 10    |      |   | 2,8,9                           |       |
| Burst operating current  | ( CL= 2 ) | ICC4 | 120  | 80  | 100   | 80   | mA  | t <sub>CK</sub> = min<br>BL = 4 | 1,2,3 |
|  | ( CL= 3 ) | ICC4 | 120  | 120 | 155   | 120  |   |                                 |       |
| Refresh current  | ICC5      | 110  | 110  | 110 | 90    | mA   | t <sub>RC</sub> = min   | 3                               |       |
| Self refresh current   | ICC6      | 1    | 1    | 1   | 1     | mA   | V <sub>IH</sub> >=V <sub>CC</sub> - 0.2<br>V <sub>IL</sub> <=.2V      | 7                               |       |
|  |           | 0.4  | 0.4  | 0.4 | 0.4   |      |   | 7,8                             |       |

| Parameter              | Symbol          | - 7K, -7J, -8, -10K |     | Unit | Test conditions  | Notes |
|------------------------|-----------------|---------------------|-----|------|--|-------|
|                        |                 | Min                 | Max |      |  |       |
| Input leakage current  | I <sub>LI</sub> | -1                  | 1   | uA   | 0 ≤ V <sub>in</sub> ≤ V <sub>CC</sub>                  |       |
| Output leakage current | I <sub>LO</sub> | -1.5                | 1.5 | uA   | 0 ≤ V <sub>out</sub> ≤ V <sub>CC</sub><br>DQ = disable |       |
| Output high voltage    | V <sub>OH</sub> | 2.4                 | -   | V    | I <sub>OH</sub> = -2 mA                                |       |
| Output low voltage     | V <sub>OL</sub> | -                   | 0.4 | V    | I <sub>OL</sub> = 2 mA                                 |       |

Notes : 1. I<sub>CC</sub> depends on output load condition when the device is selected. I<sub>CC</sub> (max) is specified at the output open condition.

2. One bank operation.
3. Addresses are changed once per one cycle.
4. Addresses are changed once per two cycles.
5. After Power down mode, CLK operating current.
6. After Power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.
8. L-Version.
9. Input signals are V<sub>IH</sub> or V<sub>IL</sub> fixed.

**Capacitance** (T<sub>a</sub> = 25C, V<sub>CC</sub>, V<sub>CCQ</sub> = 3.3 V +/- 0.3 V)

| Parameter                   | Symbol          | Min. | Max. | Unit | Notes      |
|-----------------------------|-----------------|------|------|------|------------|
| Input capacitance (CLK)     | C <sub>I1</sub> | 2.5  | 4    | pF   | 1, 3, 4    |
| Input capacitance (Signals) | C <sub>I2</sub> | 2.5  | 5    | pF   | 1, 3, 4    |
| Output capacitance (DQ)     | C <sub>O</sub>  | 4.0  | 6.5  | pF   | 1, 2, 3, 4 |

- Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQM, DQMU/DQML = V<sub>IH</sub> to disable Dout.
  3. This parameter is sampled and not 100% tested.
  4. Measured with 1.4 V bias and 200mV swing at the pin under measurement.

AC Characteristics (Ta = 0 to 70C, Vcc, Vccq = 3.3 V +/- 0.3 V, Vss, Vssq = 0 V)

| Parameter   |        | Symbol            | - 7K |        | - 7J |        | - 8 |        | - 10K |        | Unit | Notes   |
|---|--------|-------------------|------|--------|------|--------|-----|--------|-------|--------|------|---------|
|   |        |                   | Min  | Max    | Min  | Max    | Min | Max    | Min   | Max    |      |         |
| System clock cycle time   | (CL=2) | t <sub>CK</sub>   | 10   | -      | 15   | -      | 12  | -      | 15    | -      | ns   | 1       |
|   | (CL=3) | t <sub>CK</sub>   | 10   | -      | 10   | -      | 8   | -      | 10    | -      |      |         |
| CLK high pulse width  |        | t <sub>CKH</sub>  | 3    | -      | 3    | -      | 3   | -      | 3     | -      | ns   | 1       |
| CLK low pulse width   |        | t <sub>CKL</sub>  | 3    | -      | 3    | -      | 3   | -      | 3     | -      | ns   | 1       |
| Access time from CLK  | (CL=2) | t <sub>AC</sub>   | -    | 6      | -    | 8      | -   | 8      | -     | 9      | ns   | 1, 2    |
|   | (CL=3) | t <sub>AC</sub>   | -    | 6      | -    | 6      | -   | 6      | -     | 8      |      |         |
| Data-out hold time  |        | t <sub>OH</sub>   | 3    | -      | 3    | -      | 3   | -      | 3     | -      | ns   | 1, 2    |
| CLK to Data-out low impedance   |        | t <sub>LZ</sub>   | 2    | -      | 2    | -      | 2   | -      | 2     | -      | ns   | 1, 2, 3 |
| CLK to Data-out high impedance (CL = 2,3)   |        | t <sub>HZ</sub>   | -    | 6      | -    | 6      | -   | 6      | -     | 7      | ns   | 1, 4    |
| Data-in setup time  |        | t <sub>DS</sub>   | 2    | -      | 2    | -      | 2   | -      | 2     | -      | ns   | 1       |
| Data-in hold time   |        | t <sub>DH</sub>   | 1    | -      | 1    | -      | 1   | -      | 1     | -      | ns   | 1       |
| Address setup time  |        | t <sub>AS</sub>   | 2    | -      | 2    | -      | 2   | -      | 2     | -      | ns   | 1       |
| Address hold time   |        | t <sub>AH</sub>   | 1    | -      | 1    | -      | 1   | -      | 1     | -      | ns   | 1       |
| CKE setup time  |        | t <sub>CES</sub>  | 2    | -      | 2    | -      | 2   | -      | 2     | -      | ns   | 1, 5    |
| CKE setup time for power down exit  |        | t <sub>CESP</sub> | 2    | -      | 2    | -      | 2   | -      | 2     | -      | ns   | 1       |
| CKE hold time   |        | t <sub>CEH</sub>  | 1    | -      | 1    | -      | 1   | -      | 1     | -      | ns   | 1       |
| Command ( $\overline{\text{CS}}$ , $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , DQM) setup time |        | t <sub>CS</sub>   | 2    | -      | 2    | -      | 2   | -      | 2     | -      | ns   | 1       |
| Command ( $\overline{\text{CS}}$ , $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , DQM) hold time  |        | t <sub>CH</sub>   | 1    | -      | 1    | -      | 1   | -      | 1     | -      | ns   | 1       |
| Ref/Active to Ref/Active command period   |        | t <sub>RC</sub>   | 70   | -      | 70   | -      | 72  | -      | 90    | -      | ns   | 1       |
| Active to Precharge command period  |        | t <sub>RAS</sub>  | 50   | 120000 | 50   | 120000 | 48  | 120000 | 60    | 120000 | ns   | 1       |
| Active command to column command (same bank)  |        | t <sub>RCd</sub>  | 20   | -      | 20   | -      | 24  | -      | 30    | -      | ns   | 1       |
| Precharge to active command period  |        | t <sub>RP</sub>   | 20   | -      | 20   | -      | 24  | -      | 30    | -      | ns   | 1       |



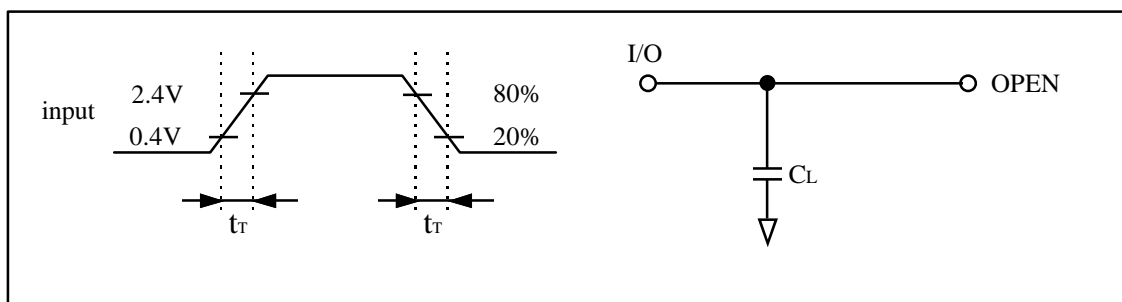
**AC Characteristics** (Ta = 0 to 70C, Vcc, Vccq = 3.3 V +/- 0.3 V, Vss, Vssq = 0 V)  
(Continued)

| Parameter  | Symbol           | - 7K |     | - 7J |     | - 8 |     | - 10K |     | Unit | Notes |
|--|------------------|------|-----|------|-----|-----|-----|-------|-----|------|-------|
|  |                  | Min  | Max | Min  | Max | Min | Max | Min   | Max |      |       |
| Write recovery or data-in to precharge lead time | t <sub>RWL</sub> | 10   | -   | 10   | -   | 10  | -   | 15    | -   | ns   | 1     |
| Active (a) to Active (b) command period          | t <sub>RRD</sub> | 20   | -   | 20   | -   | 16  | -   | 20    | -   | ns   | 1     |
| Transition time (rise to fall)                   | t <sub>T</sub>   | 1    | 5   | 1    | 5   | 1   | 5   | 1     | 5   | ns   |       |
| Refresh period                                   | t <sub>REF</sub> | -    | 64  | -    | 64  | -   | 64  | -     | 64  | ms   |       |

- Notes :
1. AC measurement assumes tr = 1ns. Reference level for timing of input signals is 1.40V.
  2. Access time is measured at 1.40V. Load condition is CL = 50pF without termination.
  3. tLZ (min) defines the time at which the outputs achieves the low impedance state.
  4. tHZ (max) defines the time at which the outputs achieves the high impedance state.
  5. tcES define CKE setup time to CKE rising edge except Power down exit command.

**Test Condition**

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



### Relationship Between Frequency and Minimum Latency

| Parameter   |        | Symbol                      | - 7K | - 7J |     | - 8 |     | - 10K |     | Notes  |
|---|--------|-----------------------------|------|------|-----|-----|-----|-------|-----|--|
| frequency(MHz)  | 100    |                             | 100  | 66   | 125 | 83  | 100 | 66    |     |  |
| t <sub>CK</sub> (ns)  | 10     |                             | 10   | 15   | 8   | 12  | 10  | 15    |     |  |
| Active command to column command (same bank)                    |        | I <sub>RCD</sub>            | 2    | 2    | 2   | 3   | 2   | 3     | 2   | 1  |
| Active command to active command (same bank)                    |        | I <sub>RC</sub>             | 7    | 7    | 6   | 9   | 6   | 9     | 6   | = [I <sub>IRAS</sub> + I <sub>IRP</sub> ], 1 |
| Active command to Precharge command (same bank)                 |        | I <sub>IRAS</sub>           | 5    | 5    | 4   | 6   | 4   | 6     | 4   | 1  |
| Precharge command to active command (same bank)                 |        | I <sub>IRP</sub>            | 2    | 2    | 2   | 3   | 2   | 3     | 2   | 1  |
| Write recovery or last data-in to Precharge command (same bank) |        | I <sub>IRWL</sub>           | 1    | 1    | 1   | 2   | 1   | 1     | 1   | 1  |
| Active command to active command (different bank)               |        | I <sub>IRRD</sub>           | 2    | 2    | 2   | 2   | 2   | 2     | 2   | 1  |
| Self refresh exit time  |        | I <sub>ISREX</sub>          | 1    | 1    | 1   | 1   | 1   | 1     | 1   |  |
| Last data in to active command (Auto Precharge, same bank)      |        | I <sub>IAPW</sub>           | 3    | 3    | 3   | 5   | 3   | 4     | 3   | = [I <sub>IRWL</sub> + I <sub>IRP</sub> ], 1 |
| Self refresh exit to command input                              |        | I <sub>ISEC</sub>           | 9    | 9    | 6   | 9   | 6   | 9     | 6   | = [I <sub>IRC</sub> ]                        |
| Precharge command to high impedance                             | (CL=2) | I <sub>IHZP</sub>           | 2    | -    | 2   | -   | 2   | -     | 2   |  |
|   | (CL=3) | I <sub>IHZP</sub>           | 3    | 3    | 3   | 3   | 3   | 3     | 3   |  |
| Last data out to active command (auto Precharge) (same bank)    |        | I <sub>IAPR</sub>           | 1    | 1    | 1   | 1   | 1   | 1     | 1   |  |
| Last data out to Precharge (early Precharge)                    | (CL=2) | I <sub>I<sub>EP</sub></sub> | - 1  | -    | - 1 | -   | - 1 | -     | - 1 |  |
|   | (CL=3) | I <sub>I<sub>EP</sub></sub> | - 2  | - 2  | - 2 | - 2 | - 2 | - 2   | - 2 |  |
| Column command to column command                                |        | I <sub>ICCD</sub>           | 1    | 1    | 1   | 1   | 1   | 1     | 1   |  |
| Write command to data in latency                                |        | I <sub>IWCD</sub>           | 0    | 0    | 0   | 0   | 0   | 0     | 0   |  |
| DQM to data in  |        | I <sub>IDID</sub>           | 0    | 0    | 0   | 0   | 0   | 0     | 0   |  |
| DQM to data out   |        | I <sub>IDOD</sub>           | 2    | 2    | 2   | 2   | 2   | 2     | 2   |  |
| CKE to CLK disable  |        | I <sub>ICLE</sub>           | 1    | 1    | 1   | 1   | 1   | 1     | 1   |  |
| Register set to active command                                  |        | I <sub>IRSA</sub>           | 1    | 1    | 1   | 1   | 1   | 1     | 1   |  |
| $\overline{\text{CS}}$ to command disable                       |        | I <sub>ICDD</sub>           | 0    | 0    | 0   | 0   | 0   | 0     | 0   |  |
| Power down exit to command input                                |        | I <sub>IPEC</sub>           | 1    | 1    | 1   | 1   | 1   | 1     | 1   |  |

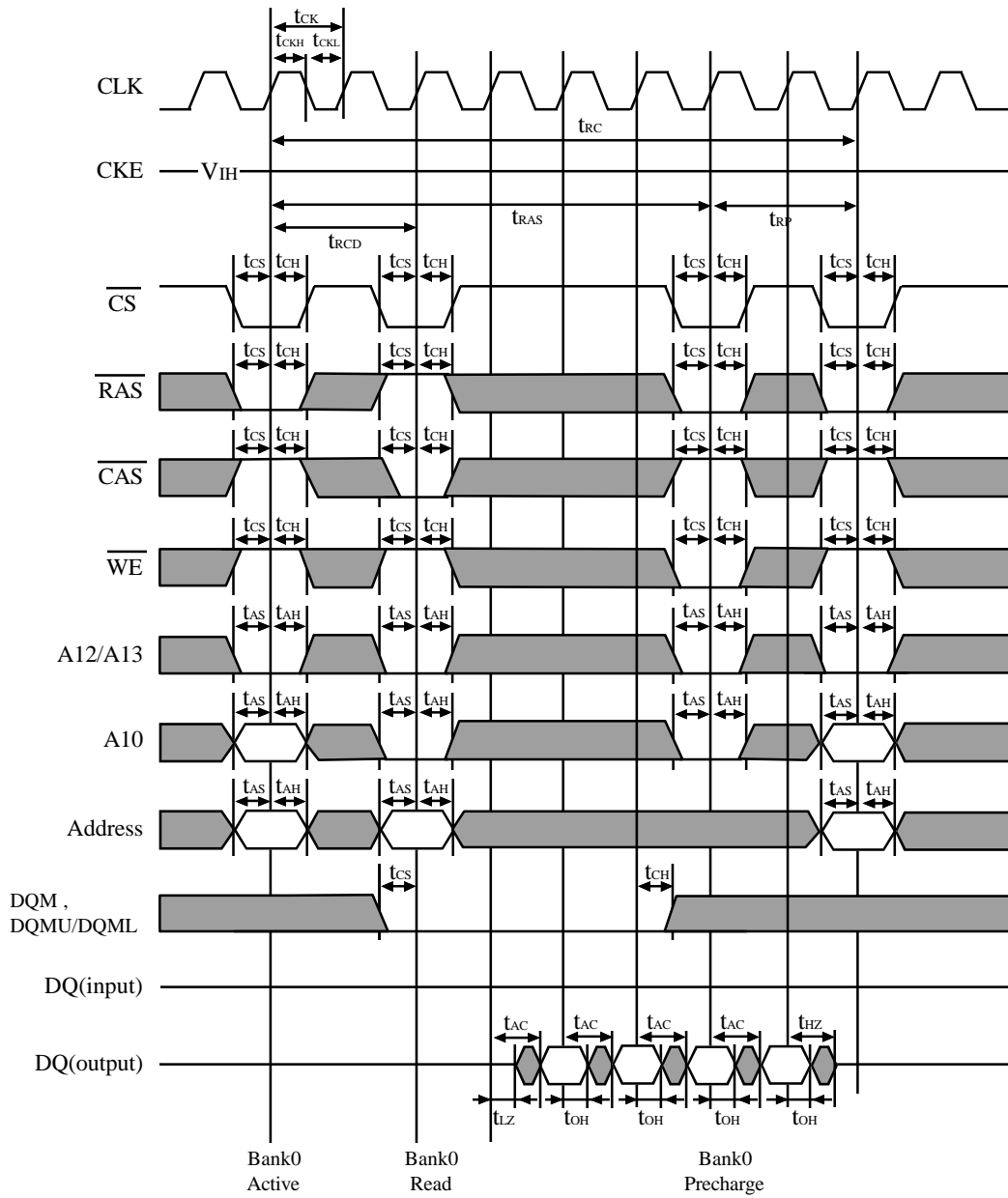
**Relationship Between Frequency and Minimum Latency**

| Parameter                            |        | Symbol           | - 7K | - 7J |    | - 8 |    | - 10K |    | Notes |
|--------------------------------------|--------|------------------|------|------|----|-----|----|-------|----|-------|
| frequency(MHz)                       |        |                  | 100  | 100  | 66 | 125 | 83 | 100   | 66 |       |
| t <sub>CK</sub> (ns)                 |        |                  | 10   | 10   | 15 | 8   | 12 | 10    | 15 |       |
| Burst stop to output valid data hold | (CL=2) | I <sub>BSR</sub> | 1    | -    | 1  | -   | 1  | -     | 1  |       |
|                                      | (CL=3) | I <sub>BSR</sub> | 2    | 2    | 2  | 2   | 2  | 2     | 2  |       |
| Burst stop to output high impedance  | (CL=2) | I <sub>BSH</sub> | 2    | -    | 2  | -   | 2  | -     | 2  |       |
|                                      | (CL=3) | I <sub>BSH</sub> | 3    | 3    | 3  | 3   | 3  | 3     | 3  |       |
| Burst stop to write data ignore      |        | I <sub>BSW</sub> | 0    | 0    | 0  | 0   | 0  | 0     | 0  |       |

Notes : 1. I<sub>RCD</sub> to I<sub>RRD</sub> are recommended value.

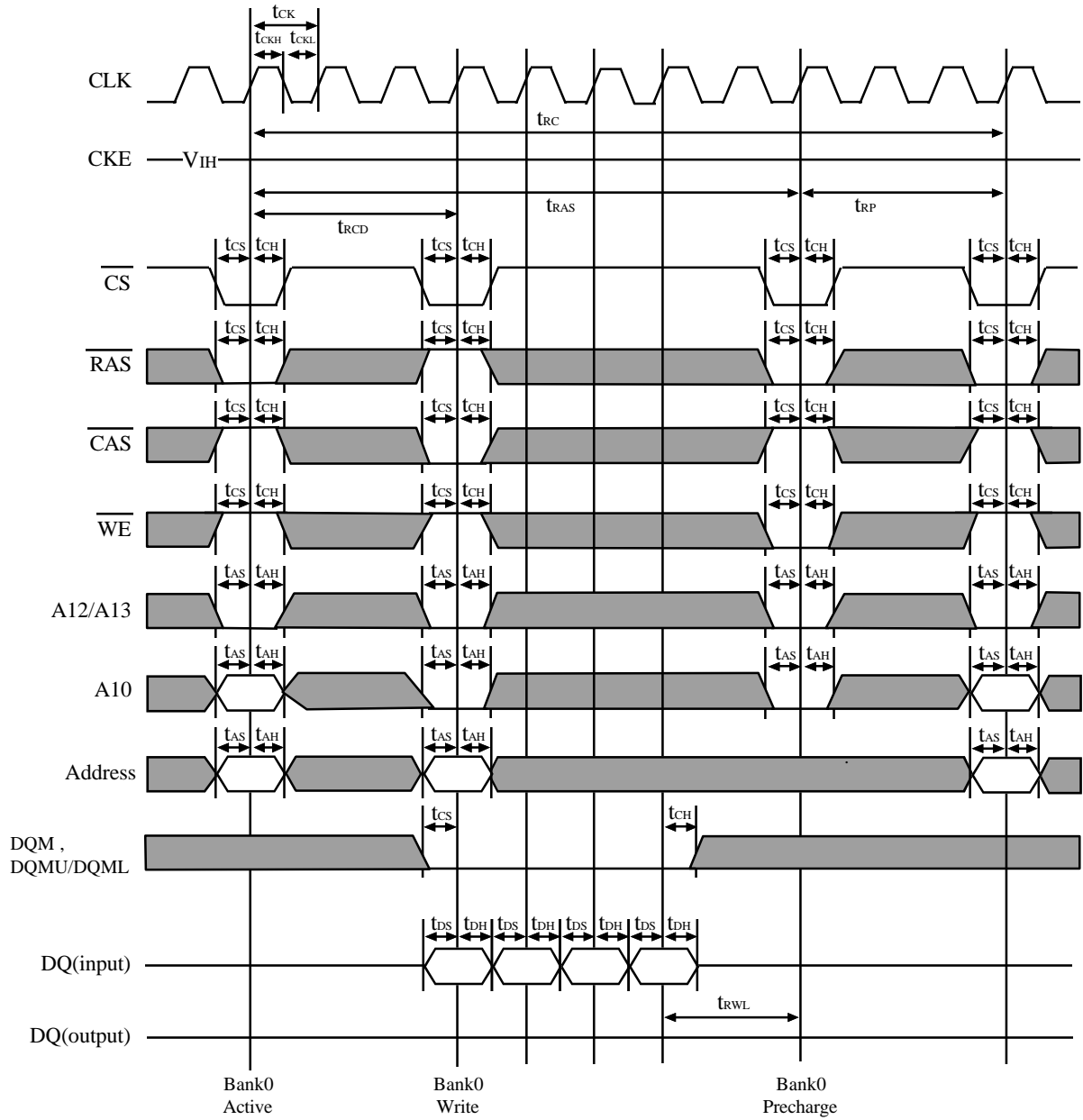
Timing Waveforms

Read Cycle



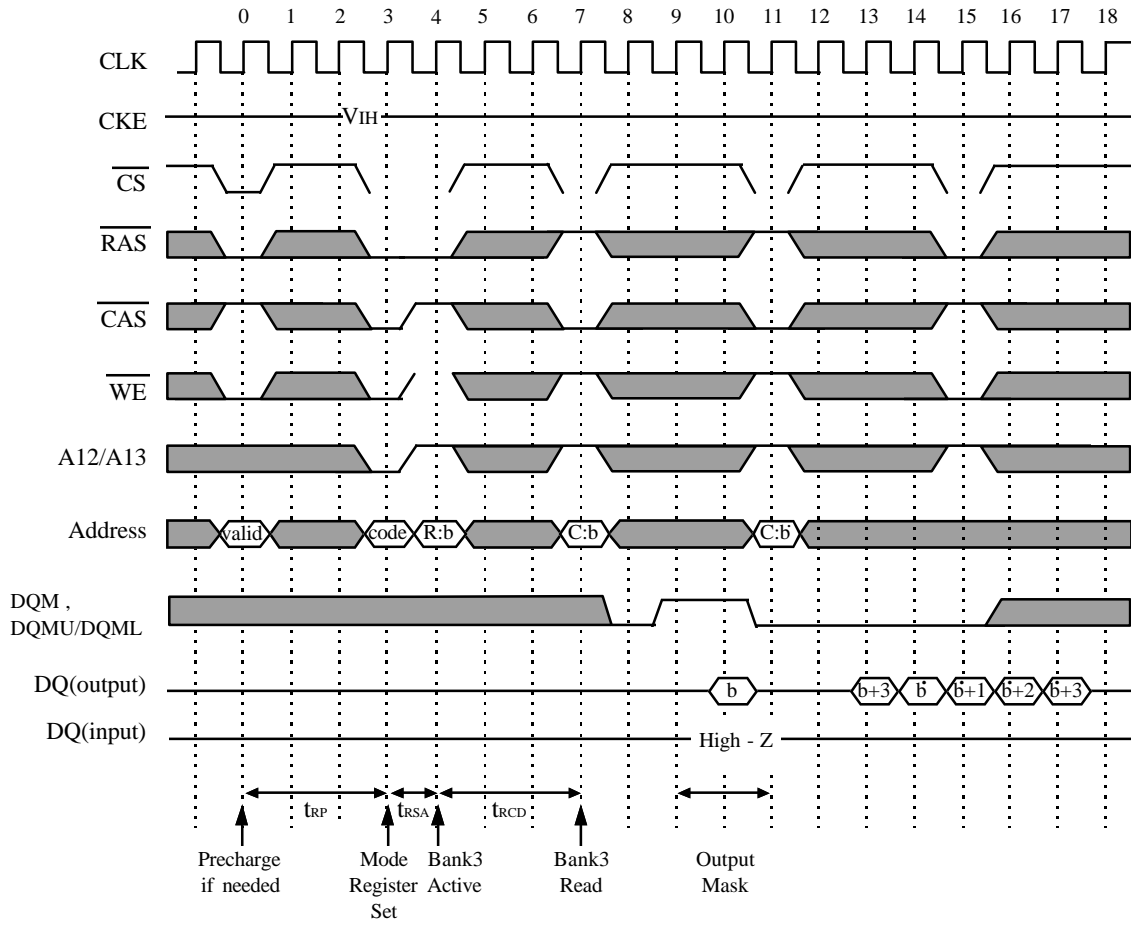
CAS Latency = 2  
 Burst Length = 4  
 Bank0 Access  
 $\square$  =  $V_{IH}$  or  $V_{IL}$

Write Cycle



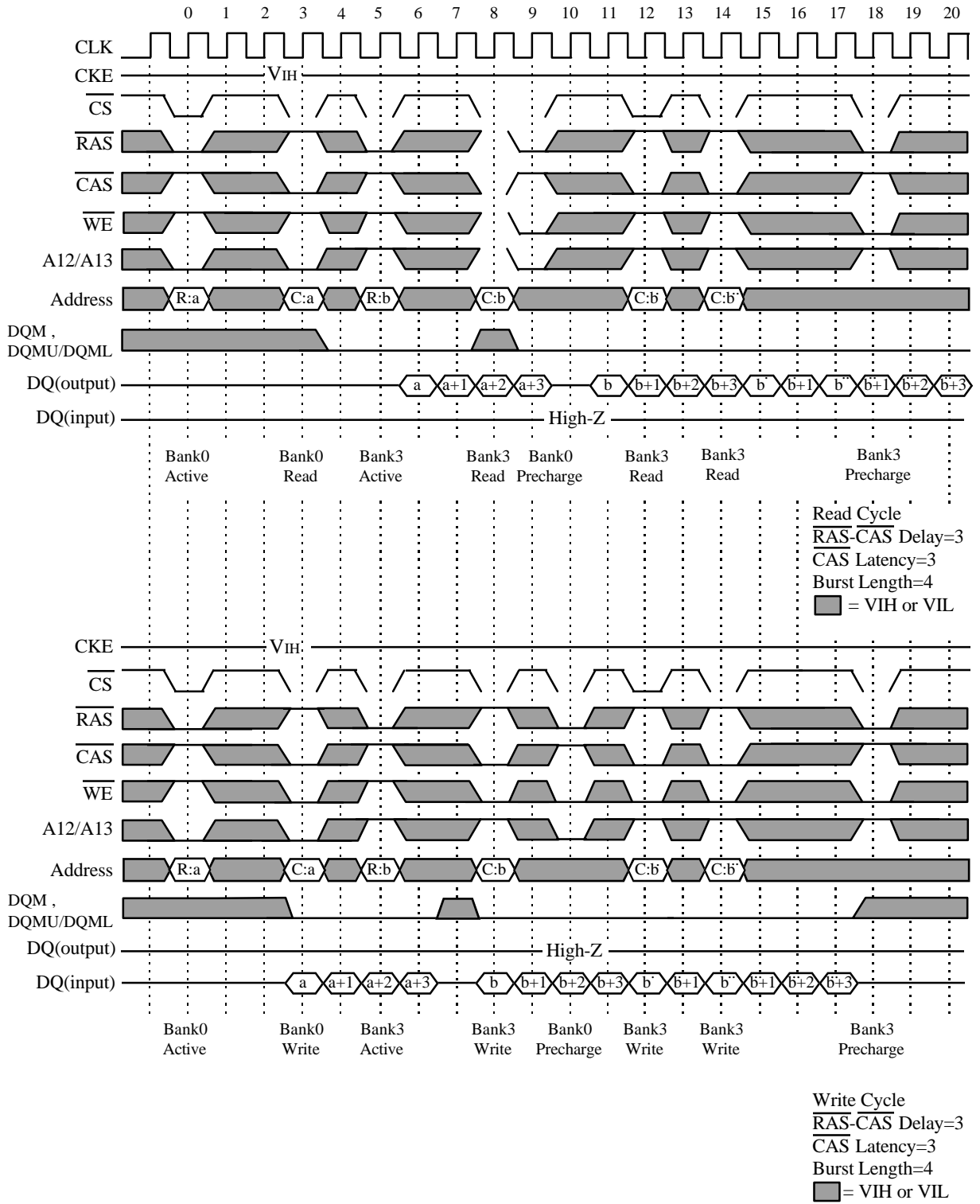
CAS Latency = 2  
 Burst Length = 4  
 Bank0 Access  
 █ =  $V_{IH}$  or  $V_{IL}$

Mode Register Set Cycle

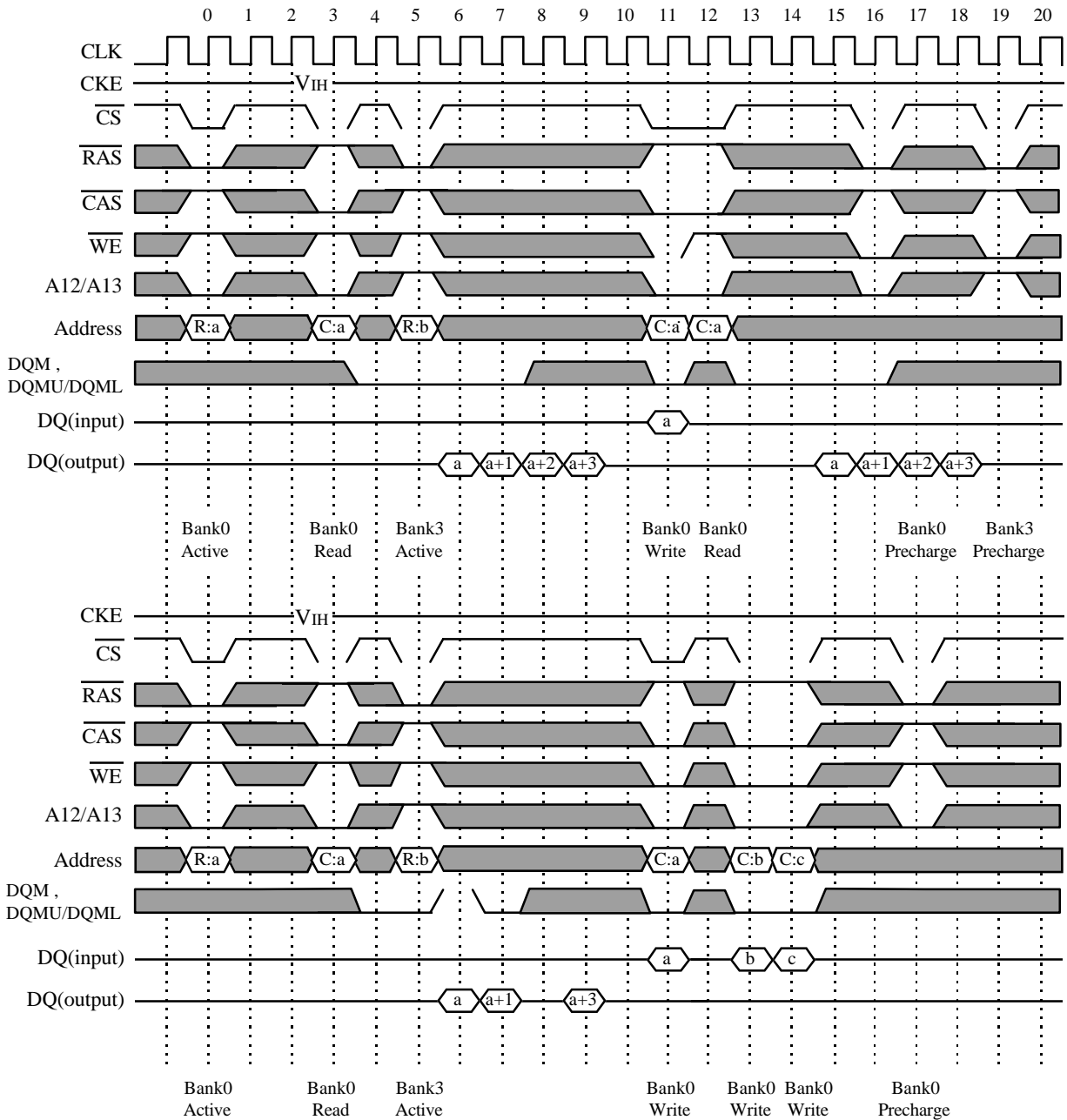


$t_{RCD}=3$   
 CAS Latency=3  
 Burst Length=4  
 ■ =  $V_{IH}$  or  $V_{IL}$

Read Cycle/ Write Cycle



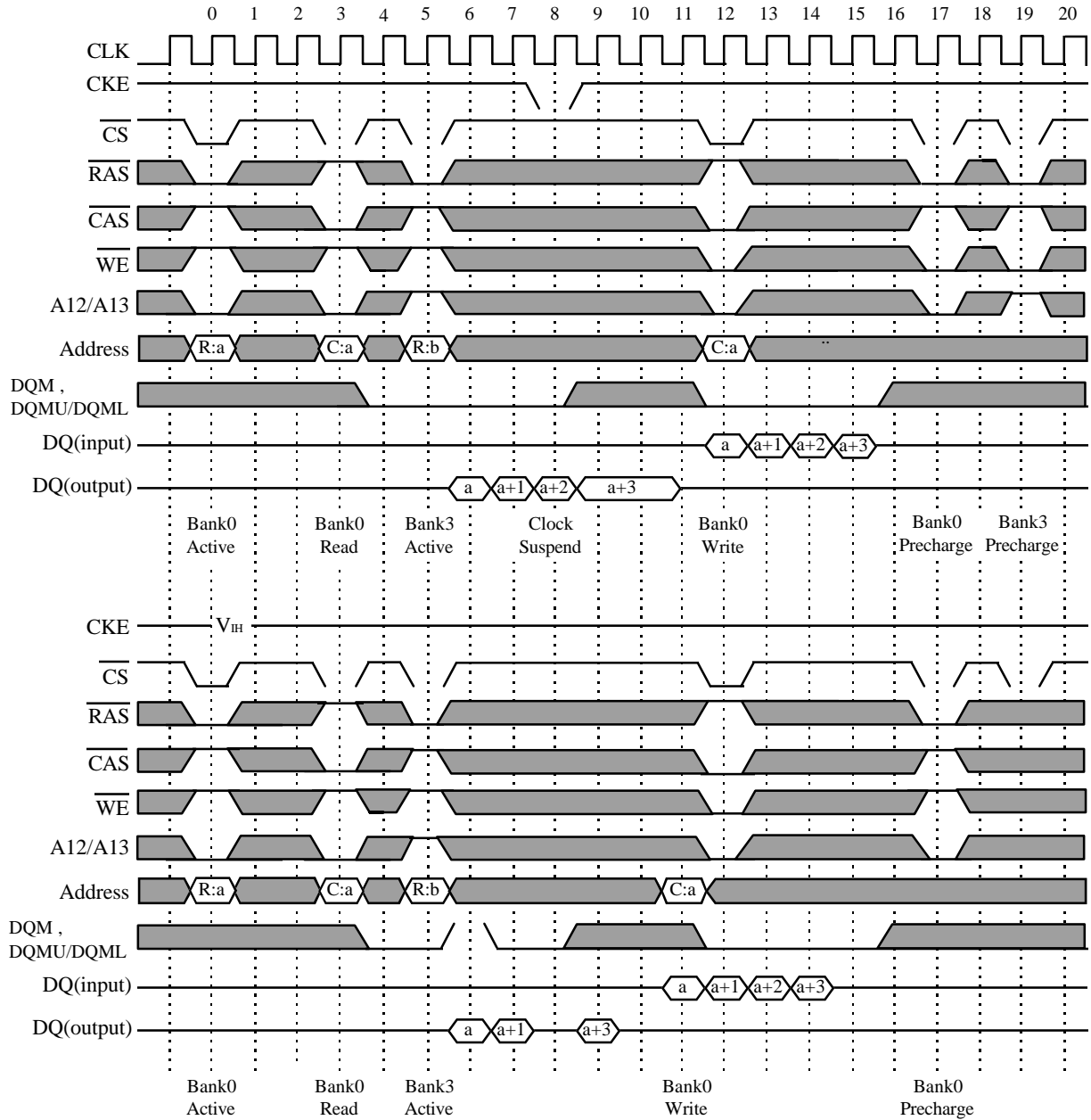
Read / Single Write Cycle



Read/Single Write Cycle  
 RAS-CAS Delay=3  
 CAS Latency=3  
 Burst Length=4  
 █ = VIH or VIL

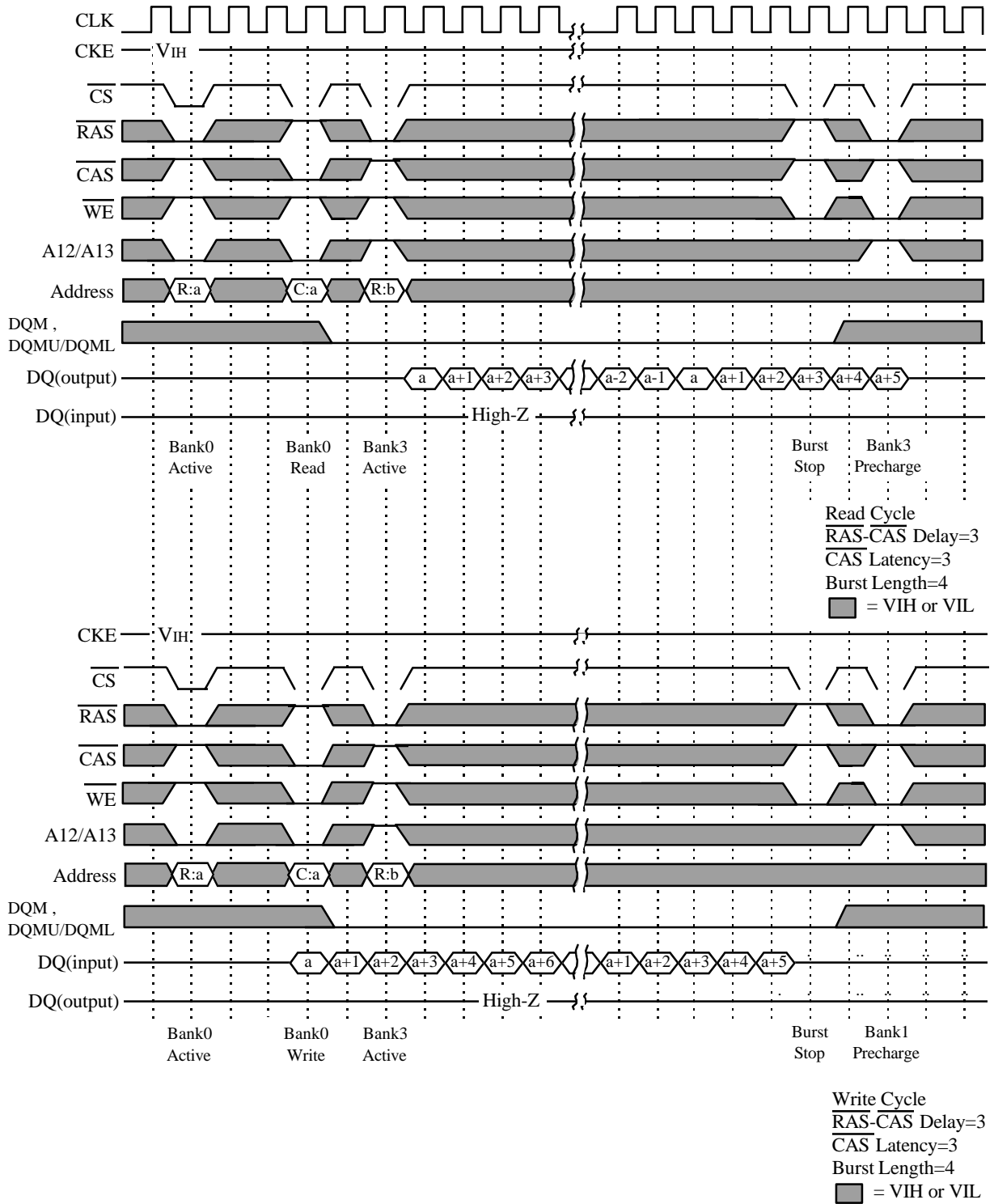


Read / Burst Write Cycle

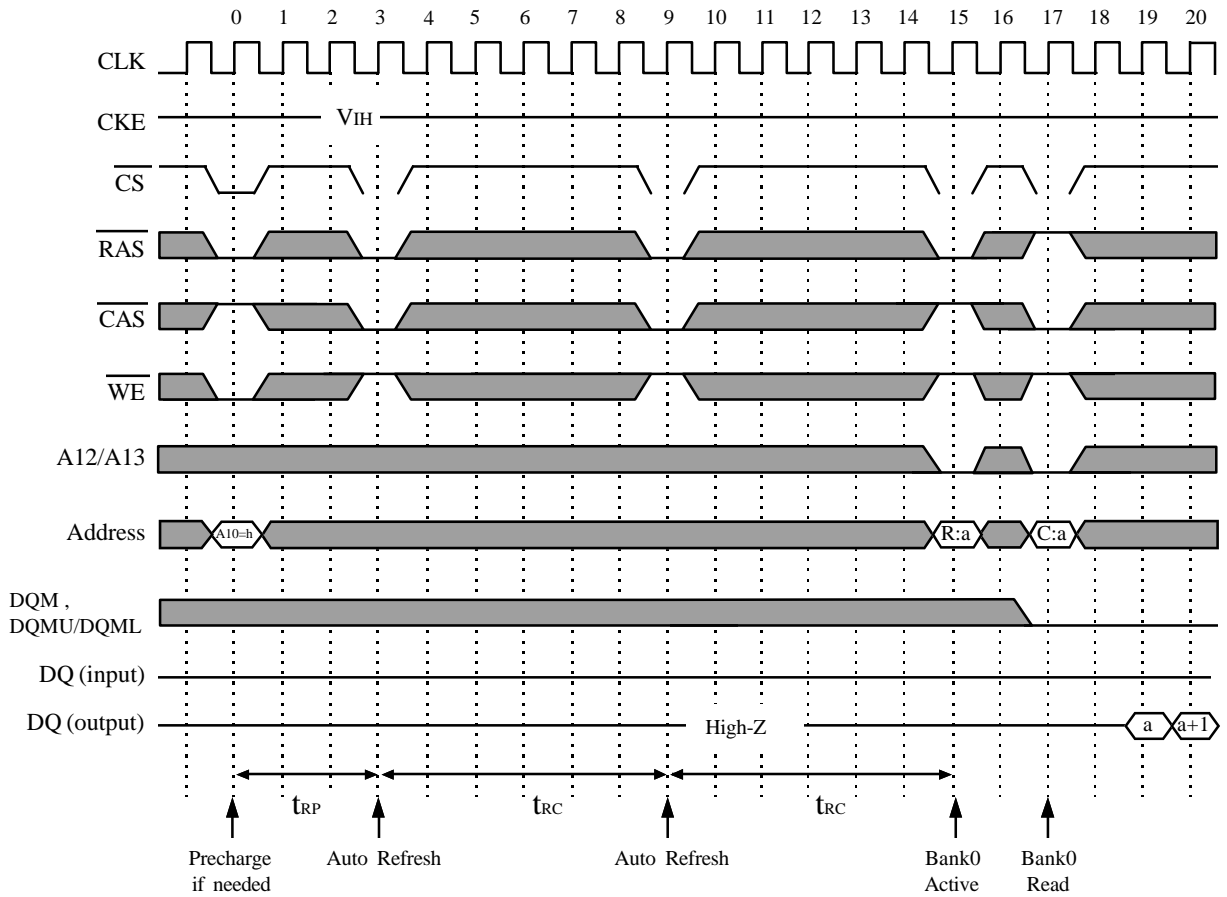


Read/Burst Write  
 RAS-CAS Delay=3  
 CAS Latency=3  
 Burst Length=4  
 ■ = VIH or VIL

Full Page Read / Write Cycle

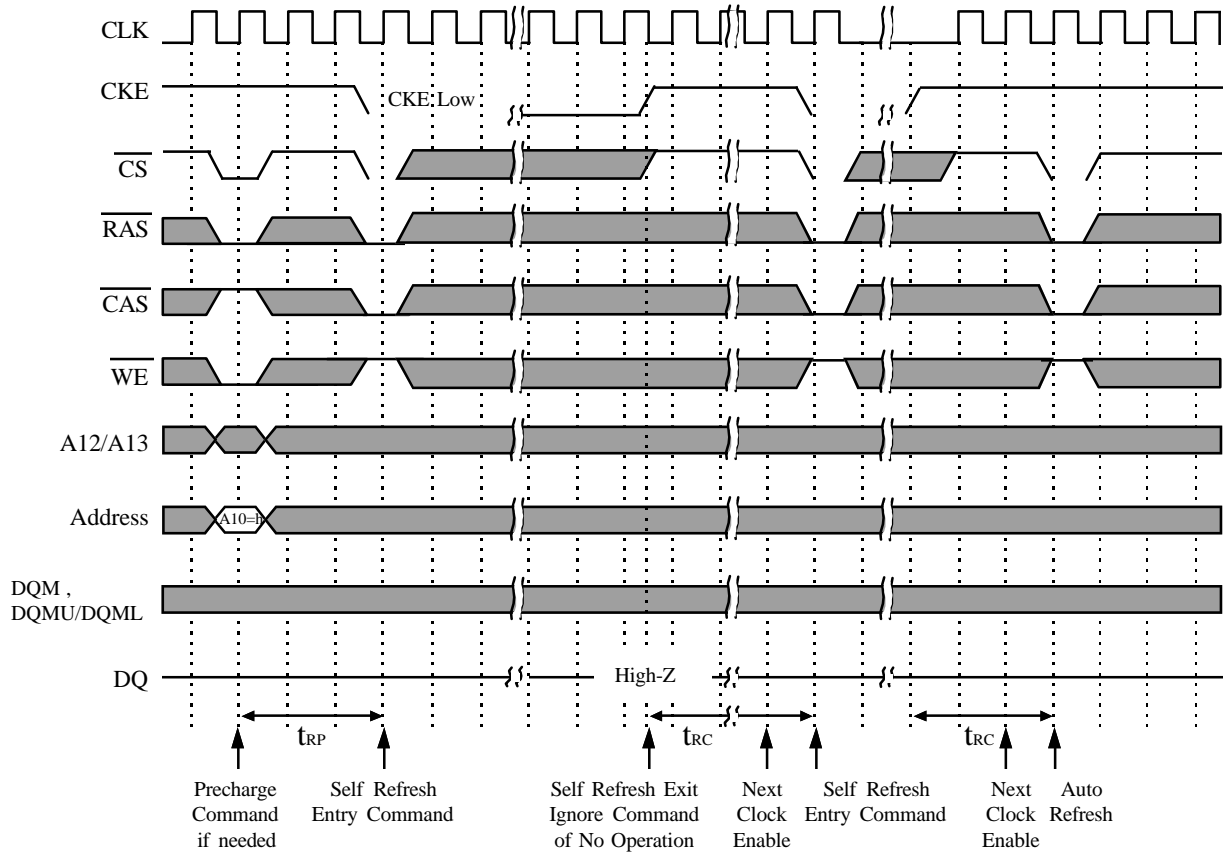


Auto Refresh Cycle



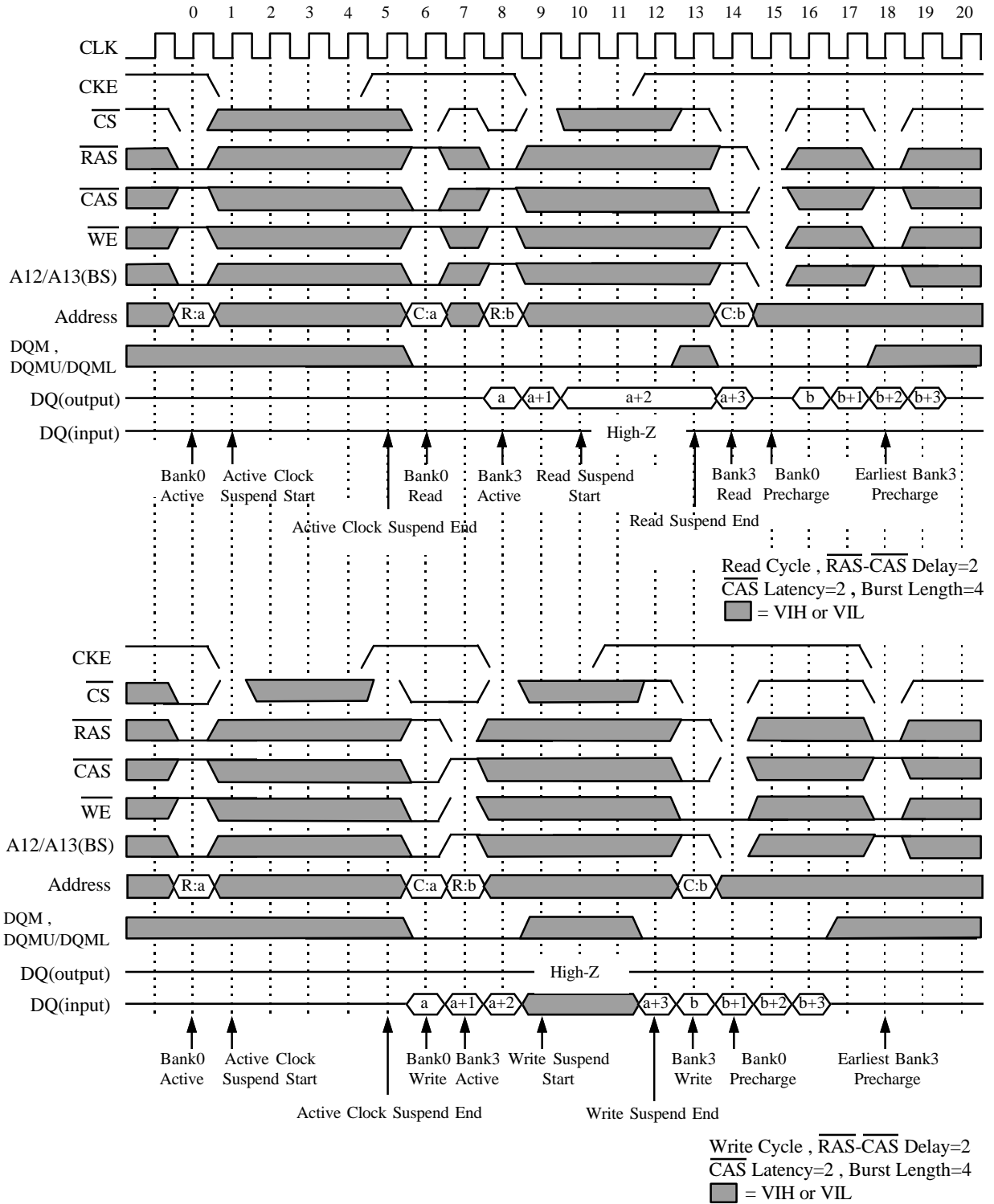
Refresh Cycle and Read Cycle  
 $\overline{RAS}$ - $\overline{CAS}$  Delay=2  
 $\overline{CAS}$  Latency=2  
 Burst Length=4  
 ■ =  $V_{IH}$  or  $V_{IL}$

Self Refresh Cycle

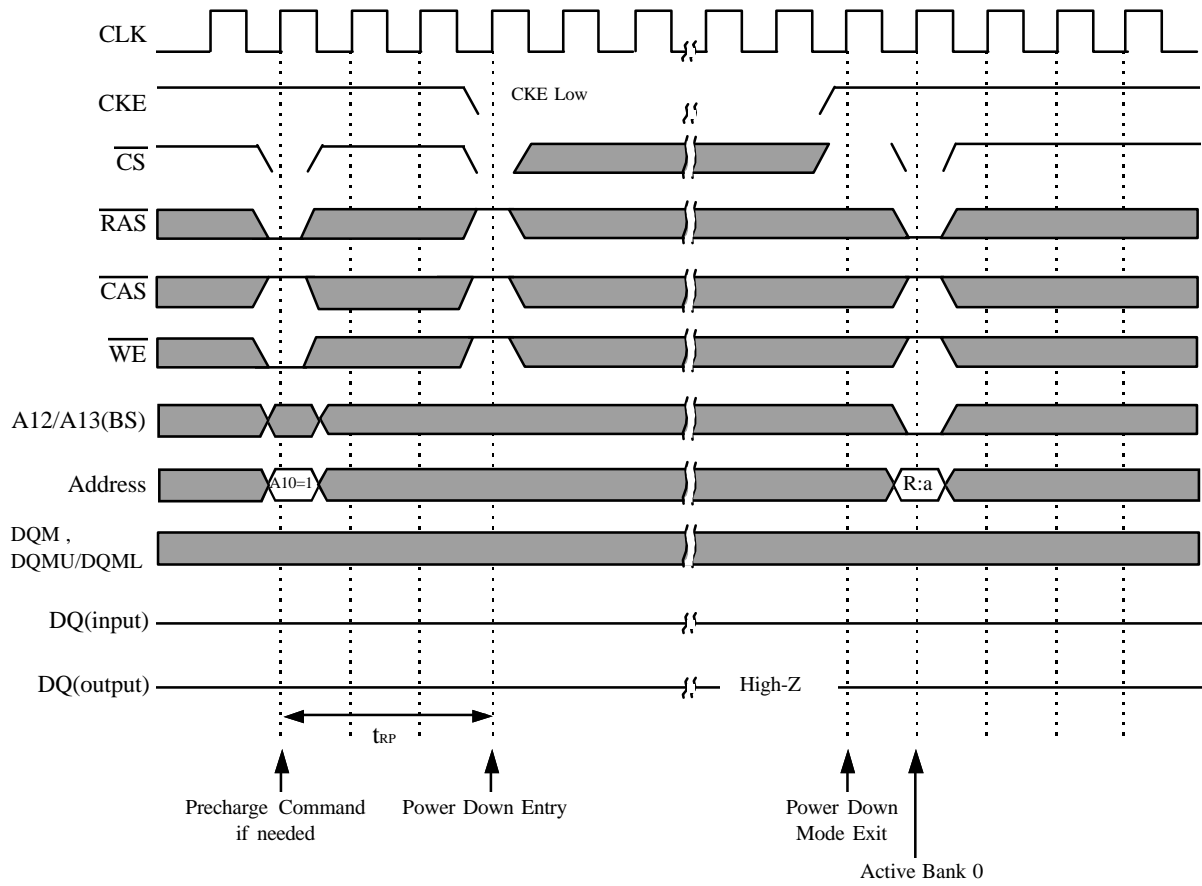


Self Refresh Cycle  
 RAS-CAS Delay = 3  
 CAS Latency=3  
 Burst Length=4  
 ■ = VIH or VIL

Clock Suspend (Active Power Down) Mode

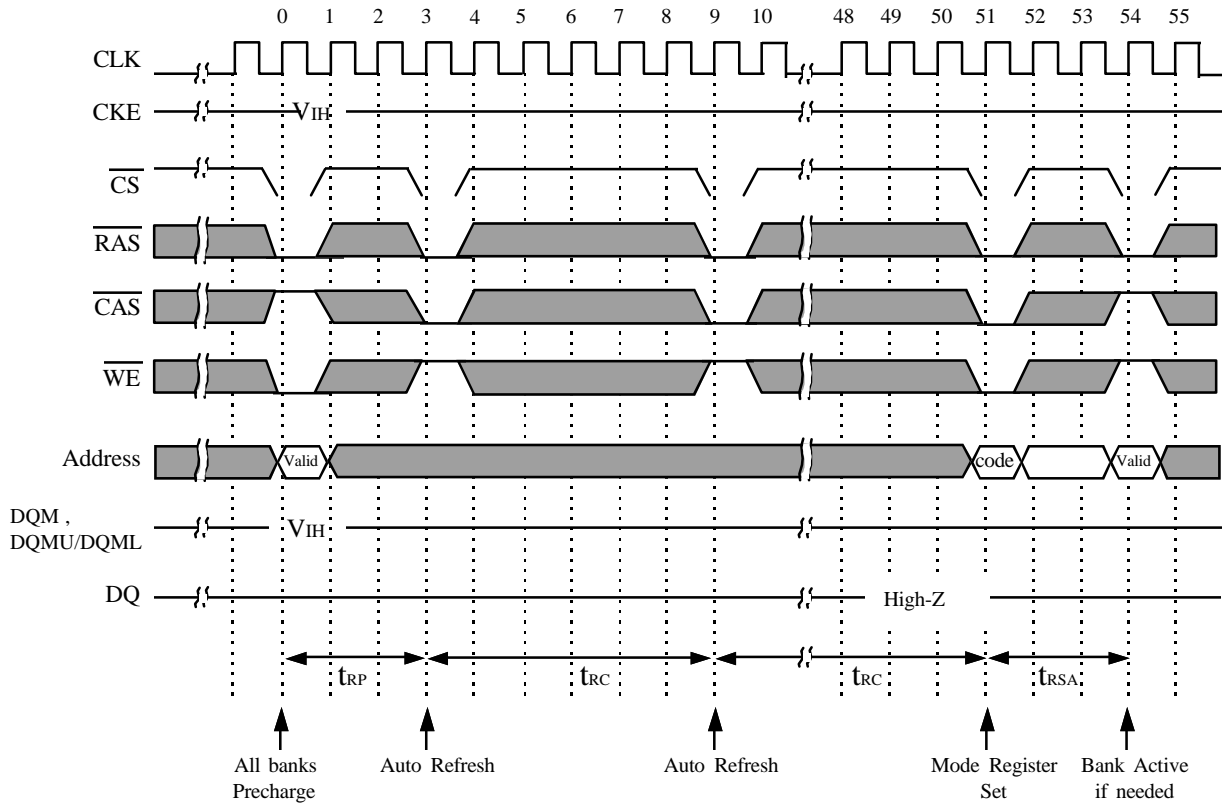


Power Down Mode



Power Down  
 Cycle  
 RAS-CAS Delay=3  
 CAS Latency=3  
 Burst Length=4  
 = VIH or VIL

Power Up Sequence



### Package Dimensions

#### GM72V66841CT/CLT Series (TTP-54D)

