



**GM72V66841ET/ELT**

2,097,152 WORD x 8 BIT x 4 BANK  
 SYNCHRONOUS DYNAMIC RAM

**Description**

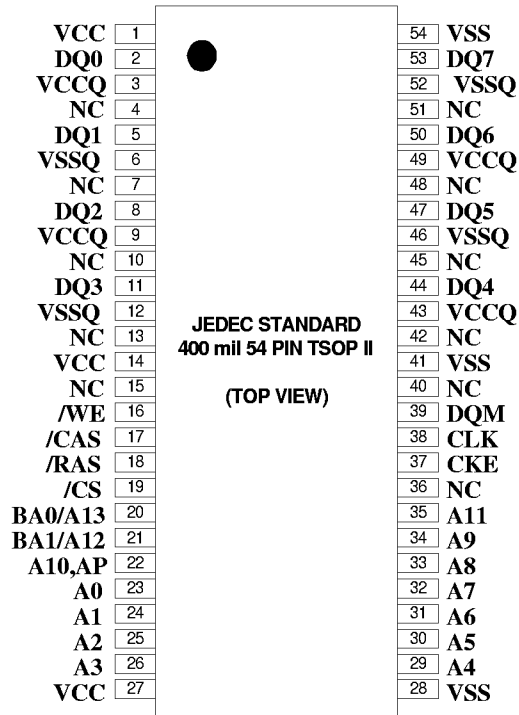
The GM72V66841ET/ELT is a synchronous dynamic random access memory comprised of 67,108,864 memory cells and logic including input and output circuits operating synchronously by referring to the positive edge of the externally provided Clock.

The GM72V66841ET/ELT provides four banks of 2,097,152 word by 8 bit to realize high bandwidth with the Clock frequency up to 143 Mhz.

**Features**

- \* PC133/PC100/PC66 Compatible
  - 7(143MHz)/-75(133MHz)/-8(125MHz)
  - 7K(PC100,2-2-2)/-7J(PC100,3-2-2)
- \* 3.3V single Power supply
- \* LVTTTL interface
- \* Max Clock frequency  
143/133/125/100MHz
- \* 4,096 refresh cycle per 64 ms
- \* Two kinds of refresh operation  
Auto refresh / Self refresh
- \* Programmable burst access capability ;
  - Sequence:Sequential / Interleave
  - Length :1/2/4/8/FP
- \* Programmable  $\overline{\text{CAS}}$  latency : 2/3
- \* 4 Banks can operate independently or simultaneously
- \* Burst read/burst write or burst read/single write operation capability
- \* Input and output masking by DQM input
- \* One Clock of back to back read or write command interval
- \* Synchronous Power down and Clock suspend capability with one Clock latency for both entry and exit
- \* JEDEC Standard 54Pin 400mil TSOP II Package

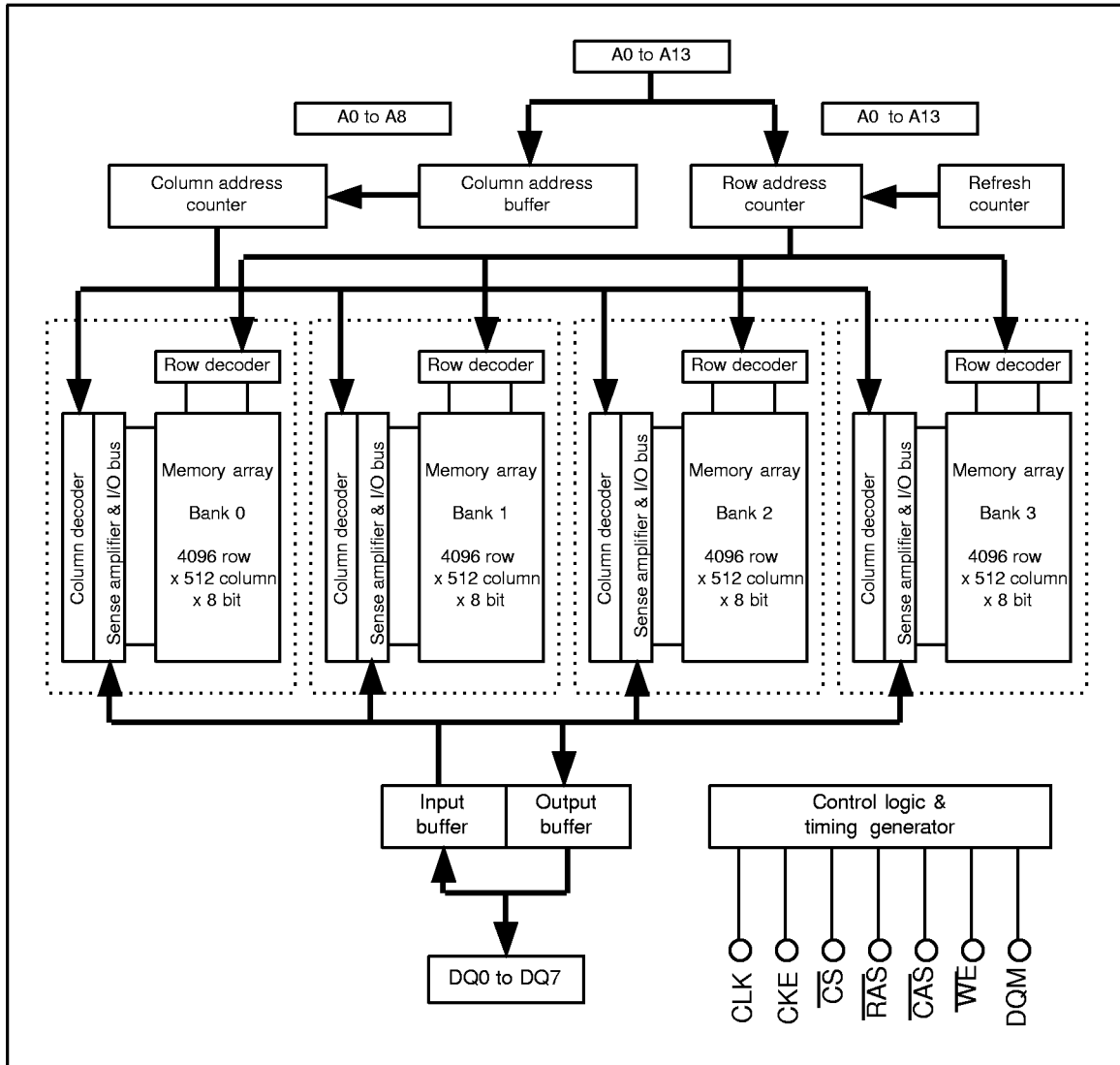
**Pin Configuration**



**Pin Name**

CLK	Clock
CKE	Clock Enable
$\overline{\text{CS}}$	Chip Select
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
A0~A9,A11	Address input
A10 / AP	Address input or Auto Precharge
BA0/A13 ~BA1/A12	Bank select
DQ0~DQ7	Data input / Data output
DQM	Data input / output Mask
VCCQ	Vcc for DQ
VSSQ	Vss for DQ
VCC	Power for internal circuit
VSS	Ground for internal circuit
NC	No Connection

Block Diagram



**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V <sub>T</sub>	-0.5 to V <sub>CC</sub> +0.5 ( $\leq 4.6$ (max))	V	1
Supply voltage relative to Vss	V <sub>CC</sub>	-0.5 to +4.6	V	1
Short circuit output current	I <sub>OUT</sub>	50	mA	
Power dissipation	P <sub>T</sub>	1.0	W	
Operating temperature	T <sub>opr</sub>	0 to +70	C	
Storage temperature	T <sub>stg</sub>	-55 to +125	C	

Notes : 1. Respect to Vss

**Recommended DC Operating Conditions (T<sub>a</sub> = 0 to + 70C)**

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V <sub>CC</sub> , V <sub>CCQ</sub>	3.0	3.6	V	1
	V <sub>SS</sub> , V <sub>SSQ</sub>	0	0	V	
Input high voltage	V <sub>IH</sub>	2.0	V <sub>CC</sub> +0.3	V	1, 2
Input low voltage	V <sub>IL</sub>	-0.3	0.8	V	1,3

Notes : 1. All voltage referred to Vss.

2. V<sub>IH</sub> (max) = 5.6V for pulse width  $\leq 3$ ns

3. V<sub>IL</sub> (min) = -2.0V for pulse width  $\leq 3$ ns

**DC Characteristics** (Ta = 0 to 70C, Vcc, VccQ = 3.3 V +/- 0.3 V, Vss, VssQ = 0 V)

Parameter	Symbol	- 7	- 75	- 8	-7K	-7J	Unit	Test conditions	Notes	
		Max	Max	Max	Max	Max				
Operating current	ICC1	85	85	80	80	80	mA	Burst length= 1 trc = min	1, 2, 3	
Standby current in power down	ICC2P	2					mA	CKE = VIL, tck = 12 ns	5	
Standby current in power down (input signal stable)	ICC2PS	2					mA	CKE=VIL, tck= infinity	6	
		0.4							6,8	
Standby current in non power down (CAS Latency=2)	ICC2N	15					mA	CKE,CS = VIH, tck = 12ns	4	
Standby current in non power down (input signal stable)	ICC2NS	12					mA	CKE = VIH, tck = infinity	4	
Active standby current in power down	ICC3P	6					mA	CKE = VIL, tck = 12 ns, DQ = High-Z	1,2,5	
Active standby current in power down (input signal stable)	ICC3PS	5					mA	CKE = VIL, tck = infinity	2,6	
Active standby current in non power down	ICC3N	30					mA	CKE,CS = VIH, tck = 12 ns, DQ = High-Z	1,2,4	
Active standby current in non power down (input signal stable)	ICC3NS	20					mA	CKE = VIH, tck = infinity	2,9	
Burst operating current	( CL= 2 )	ICC4	120					mA	tck = min BL = 4	1,2,3
	( CL= 3 )	ICC4	150	150	150	120	120	mA		
Refresh current	ICC5	140					mA	trc = min	3	
Self refresh current	ICC6	1					mA	VIH >=VCC - 0.2 VIL <=0.2V	7	
		0.4							7,8	

**DC Characteristics** (Ta = 0 to 70C, Vcc, Vccq = 3.3 V +/- 0.3 V, Vss, Vssq= 0 V)

(Continued)

Parameter	Symbol	- 7, - 75, - 8, - 7K, - 7J		Unit	Test conditions	Notes
		Min	Max			
Input leakage current	ILI	-1	1	uA	0 <= Vin <= Vcc	
Output leakage current	ILO	-1.5	1.5	uA	0 <= Vout <= Vcc DQ = disable	
Output high voltage	VOH	2.4	-	V	IOH = -2 mA	
Output low voltage	VOL	-	0.4	V	IOL = 2 mA	

Notes : 1. Icc depends on output load condition when the device is selected. Icc (max) is specified at the output open condition.

2. One bank operation.
3. Addresses are changed once per one cycle.
4. Addresses are changed once per two cycles.
5. After Power down mode, CLK operating current.
6. After Power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.
8. L-Version.
9. Input signals are VIH or VIL fixed.

**Capacitance** (Ta = 25C , Vcc, Vccq = 3.3 V + /- 0.3 V)

Parameter	Symbol	Min.	Max.	Unit	Notes
Input capacitance (CLK)	C11	2.5	4	pF	1, 3, 4
Input capacitance (Signals)	C12	2.5	5	pF	1, 3, 4
Output capacitance (DQ)	Co	4.0	6.5	pF	1, 2, 3, 4

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. DQM = VIH to disable Dout.
3. This parameter is sampled and not 100% tested.
4. Measured with 1.4 V bias and 200mV swing at the pin under measurement.



**AC Characteristics** ( $T_a = 0$  to  $70^\circ\text{C}$ ,  $V_{CC}, V_{CCQ} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS}, V_{SSQ} = 0\text{ V}$ )  
(Continued)

Parameter	Symbol	- 7		- 75		- 8		- 7K		- 7J		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write recovery or data-in to precharge lead time	$t_{RWL}$	7	-	7.5	-	8	-	10	-	10	-	ns	1
Active (a) to Active (b) command period	$t_{RRD}$	14	-	15	-	16	-	20	-	20	-	ns	1
Refresh period	$t_{REF}$	-	64	-	64	-	64	-	64	-	64	ms	

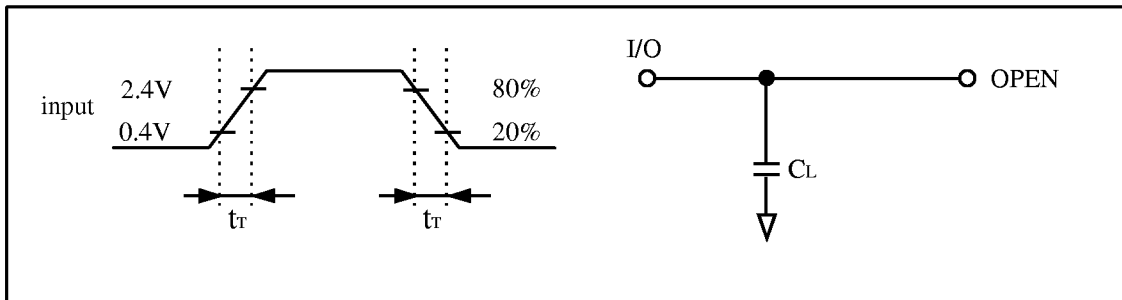
Notes : 1. AC measurement assumes  $t_r = 1\text{ns}$ . Reference level for timing of input signals is 1.40V.

If  $t_r$  is longer than 1ns, transition time compensation should be considered.

2. Access time is measured at 1.40V. Load condition is  $C_L = 50\text{pF}$  without termination.
3.  $t_{LZ}(\text{min})$  defines the time at which the outputs achieves the low impedance state.
4.  $t_{HZ}(\text{max})$  defines the time at which the outputs achieves the high impedance state.
5.  $t_{CES}$  define CKE setup time to CKE rising edge except Power down exit command.

**Test Condition**

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures







**Relationship Between Frequency and Minimum Latency**

Parameter		Symbol	-7		-75		-8		-7K		-7J		Notes
frequency(MHz)			143	100	133	100	125	100	100	100	100	66	
t <sub>CK</sub> (ns)			7	10	7.5	10	8	10	10	10	10	15	
Burst stop to output valid data hold	(CL=2)	I <sub>BSR</sub>	-	1	-	1	-	1	1	1	-	1	
	(CL=3)	I <sub>BSR</sub>	2	2	2	2	2	2	2	2	2	2	
Burst stop to output high impedance	(CL=2)	I <sub>BSH</sub>	-	2	-	2	-	2	2	2	-	2	
	(CL=3)	I <sub>BSH</sub>	3	3	3	3	3	3	3	3	3	3	
Burst stop to write data ignore		I <sub>BSW</sub>	0	0	0	0	0	0	0	0	0	0	

Notes : 1. I<sub>RCD</sub> to I<sub>RRD</sub> are recommended value.

### Package Dimensions

#### GM72V66841ET/ELT Series (TTP-54D)

