GM8182

PCB LAYOUT GUIDE

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REVISION HISTORY

GM8182 PCB Layout Guide

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Chapter 1

484 pin BGA

This chapter contains the following sections:

1.1 Decoupling

GM8182 BGA layout is strict attention must be given to decoupling capacitors between power and ground plane. GM8182 VCC_CORE/ VCC_DDR/ VCC_IO decoupling caps should be placed directly underneath the SoC on the opposite PCB side. And it's better to use one capacitor at each power pins.

VCC_CORE: use 10uf 0805/0.1uF 0402/0.01uF 0402 MLCC ceramic caps directly under the GM8182 BGA. And 100uF low ESR cap as bulk capacitance as close to the chip as possible.

VCC_DDR : use 10uf 0805/0.1uF 0402/0.01uF 0402 MLCC ceramic caps directly under the GM8182 BGA. And 100uF low ESR cap as bulk capacitance as close to the chip as possible.

VCC_IO : use 10uf 0805/0.1uF 0402/0.01uF 0402 MLCC ceramic caps directly under the GM8182 BGA. And 47uF low ESR cap as bulk capacitance as close to the chip as possible.

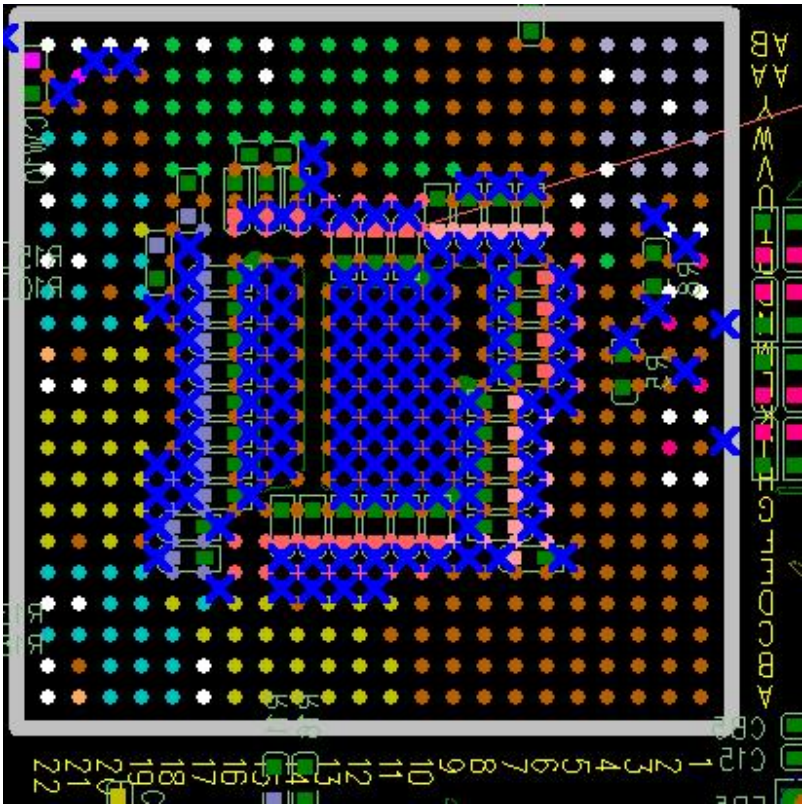


Figure 1 provides an example of how the BGA decoupling capacitors Layout on the GM8182 Evaluation Platform Board.

1.2 Power and Ground Plane

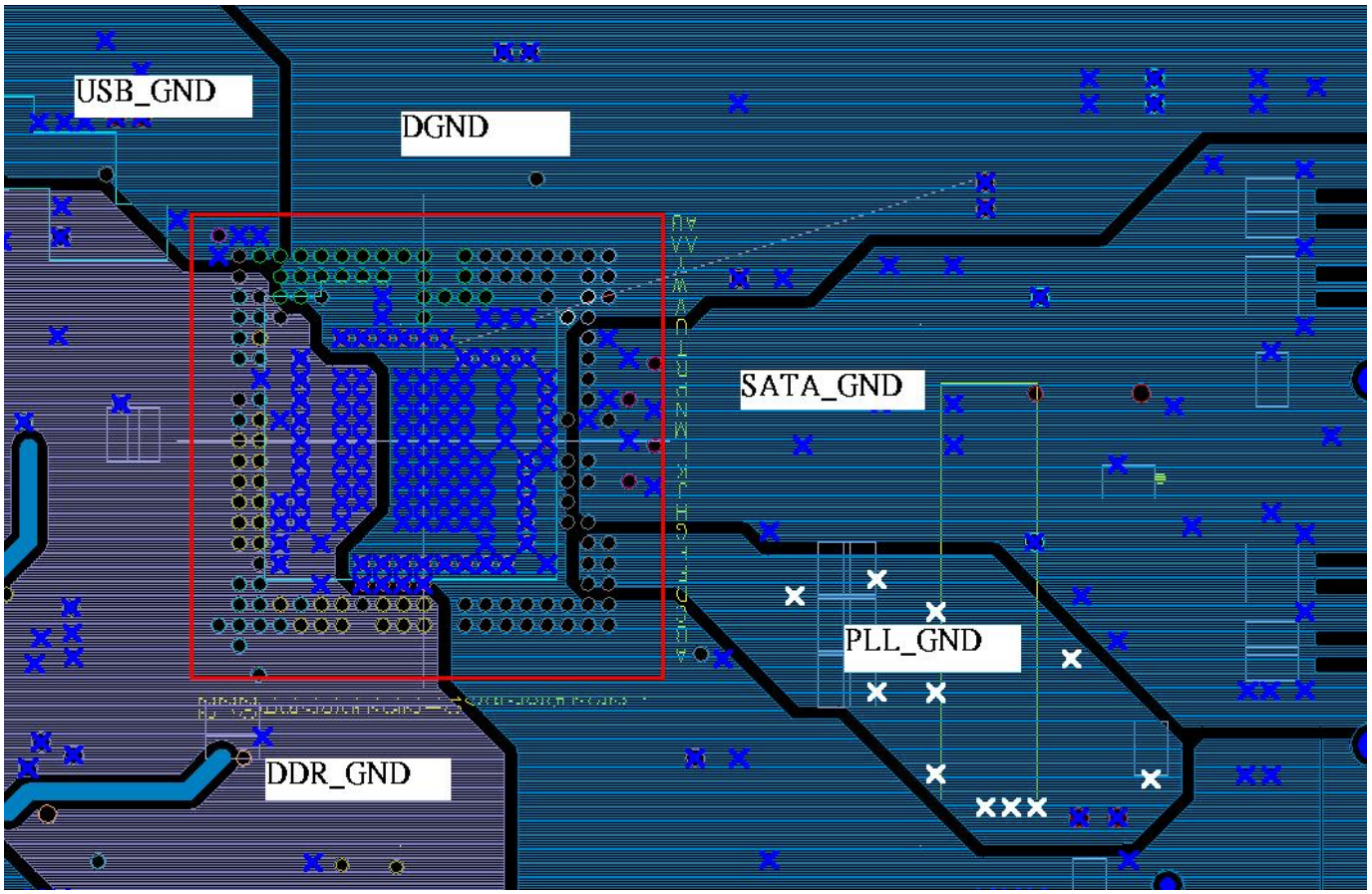


Figure 2 provides an example of how the ground plane Layout on the GM8182 four layer 8CH EVB Board.

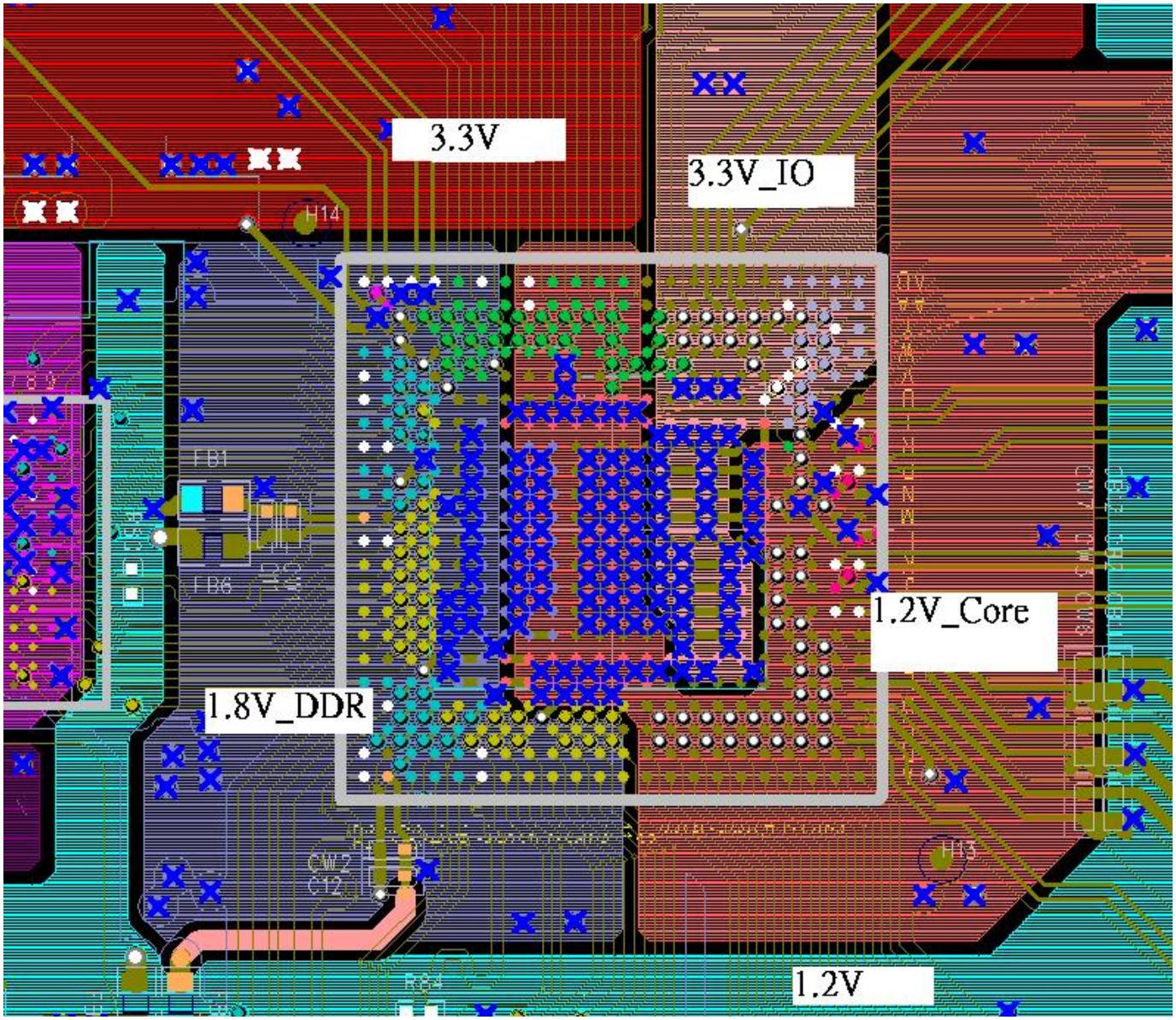


Figure 3 provides an example of how the power plane Layout on the GM8182 four layer 8CH EVB Board.

Chapter 2

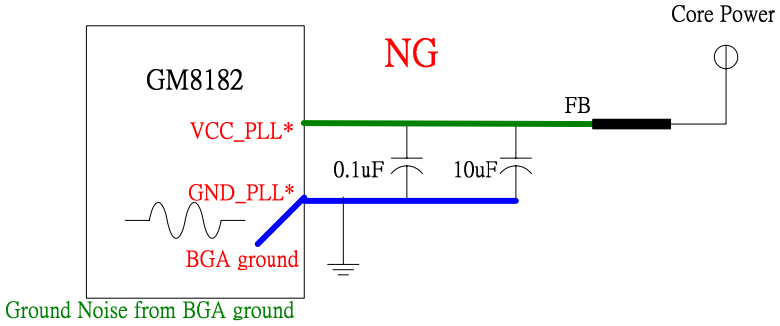
PLL

This chapter contains the following sections:

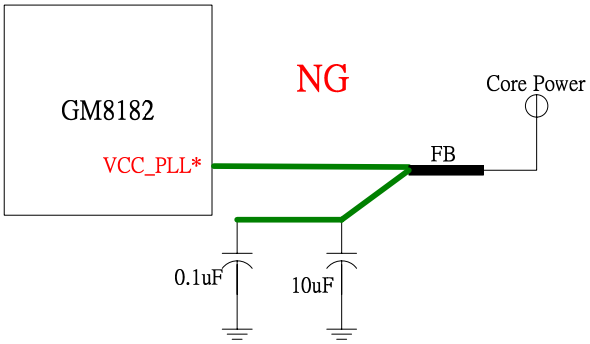
2.1 Trace Layout and Passive Materials Selection

The GM8182 PLL1,PLL2 and PLL3 are very high speed PLL. The layout of the PLL need to take cares the power and ground noise.

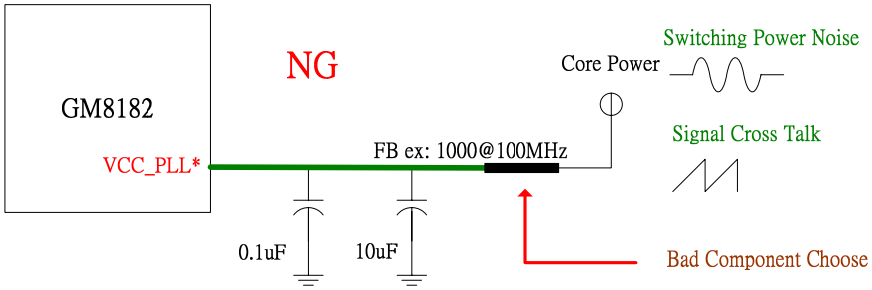
1. The PLL1 (CPU) power and ground noise don't exceed over 100mV pk-pk.
   The PLL2 (Mac, SATA) power and ground noise don't exceed over 200mVpk-pk.
   The PLL3 (Codec, Peripheral) power and ground noise don't exceed over 200mVpk-pk.
2. The power noise of PLL1 lower bond (1.2 - 0.5 x △V) don't under 1.08V.
   The power noise of PLL2 lower bond (1.2 - 0.5 x △V) don't under 1.08V.
   The power noise of PLL3 lower bond (1.2 - 0.5 x △V) don't under 1.08V.
3. PLL power, ground is analog signal. Don't connect the BGA power, ground to PLL power, ground directly.

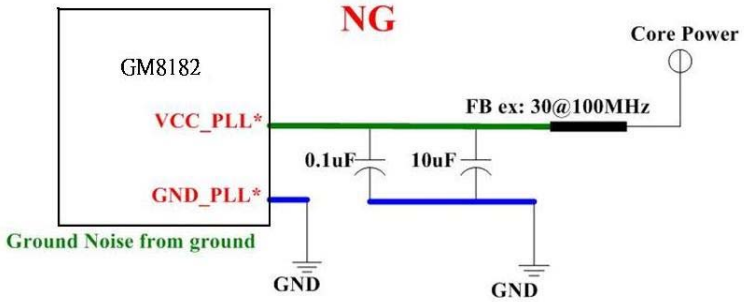


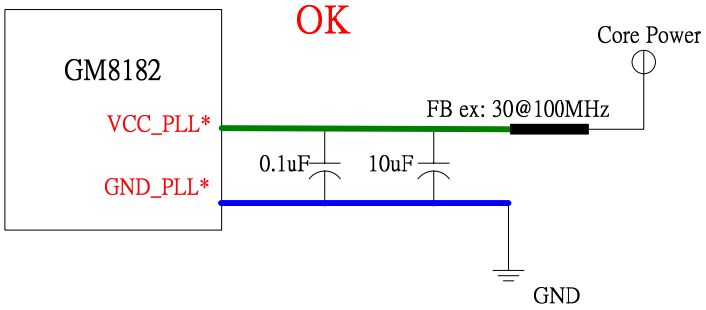
4. The PLL power trace needs to pass through the by-pass capacitors. It's better to use the 0.01~0.1uF capacitor and >10uF low ESR capacitor.



5. Doesn't use the ferrite bead which impedance over 100Ω@100MHz.







Chapter 3

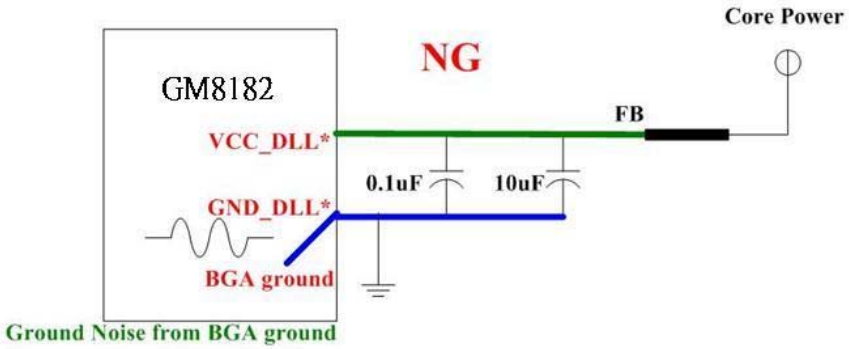
DLL

This chapter contains the following sections:

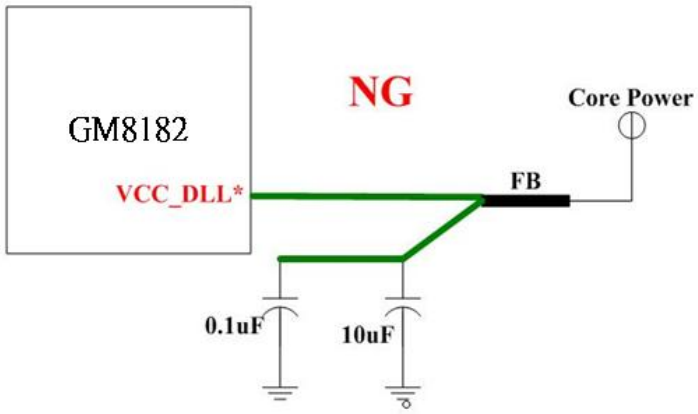
3.1 Trace Layout and Passive Materials Selection

The GM8182 DDLL0~DDLL1 are high speed DLL. The layout of the DLL need to take cares the power and ground noise.

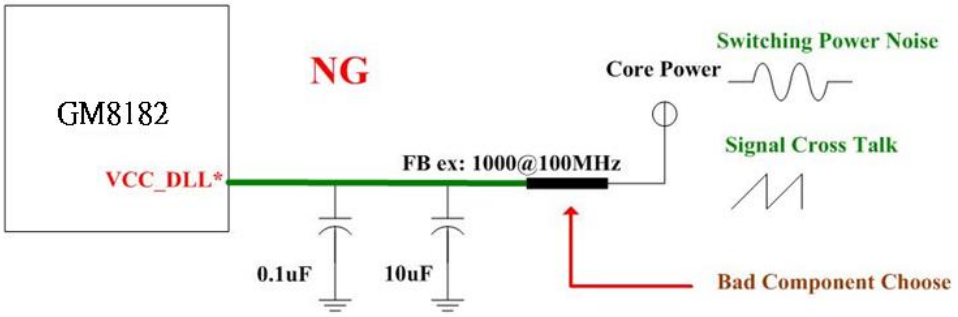
1. The DDLL0~DDLL1 (DDR2) power and ground noise don't exceed over 200mVpk-pk.
2. The power noise of DDLL0~DDLL2 lower bond (1.2 - 0.5 x △V) don't under 1.08V.
3. DDLL0~DDLL1 power, ground is analog signal. Don't connect the BGA power, ground to DLL power, ground directly.

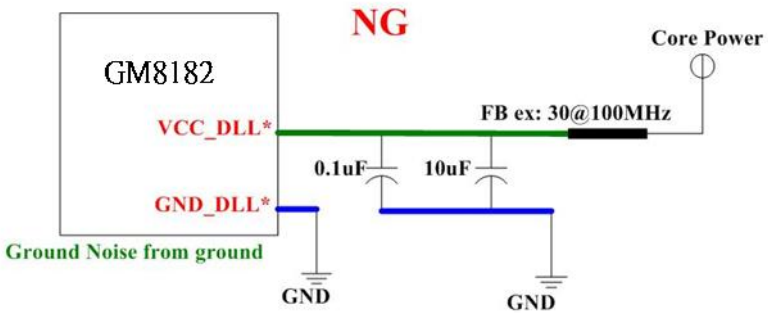


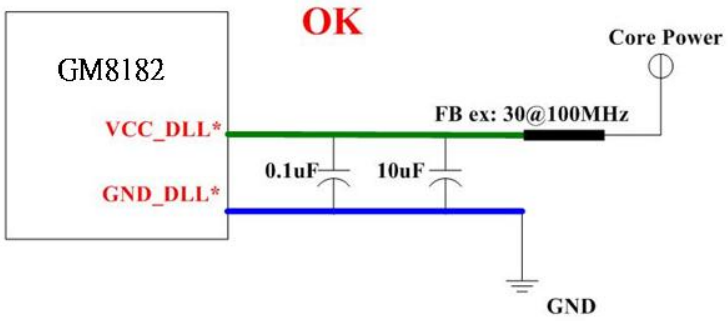
4. The DLL power trace needs to pass through the by-pass capacitors. It's better to use the 0.01~0.1uF capacitor and >10uF low ESR capacitor.



5. Doesn't use the ferrite bead which impedance over 100Ω@100MHz.







Chapter 4

DDR2-SDRAM

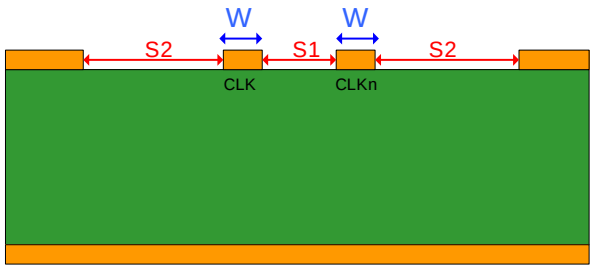
This chapter contains the following sections:

4.1 CLK/CLKn Impendence and Routing

The ultimate purpose of CLK/CLKn layout is to define the trace width/space, maximum length and impendence.

Trace Impedance:

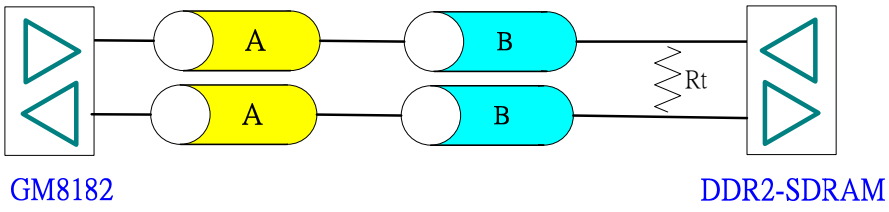
CLK/CLKn Differential trace impedance: 100 ohms +/- 15%



Signal	Typical	Unit
CLK and CLKn Trace Width (W)	5	mils
CLK and CLKn Trace Spacing (S1)	13	mils
CLK and CLKn to other Trace Spacing (S2)	>20	mils

Routing Specification:

Parallel termination **Rt = 100 ohms +/- 5%**



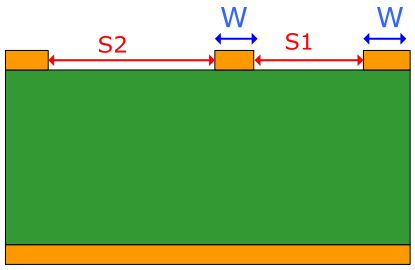
Description	Minimum Length	Maximum Length	Unit
Breakout from BGA (A)	0	0.5	inch
Lead in DDR2 (B)		8	inch
CLK and CLKn mismatch	0	20	mil

4.2 Address and Control Impendence and Routing

The ultimate purpose of address and control pins layout is to define the trace and bus group width/space, maximum length and impendence.

Trace Impedance:

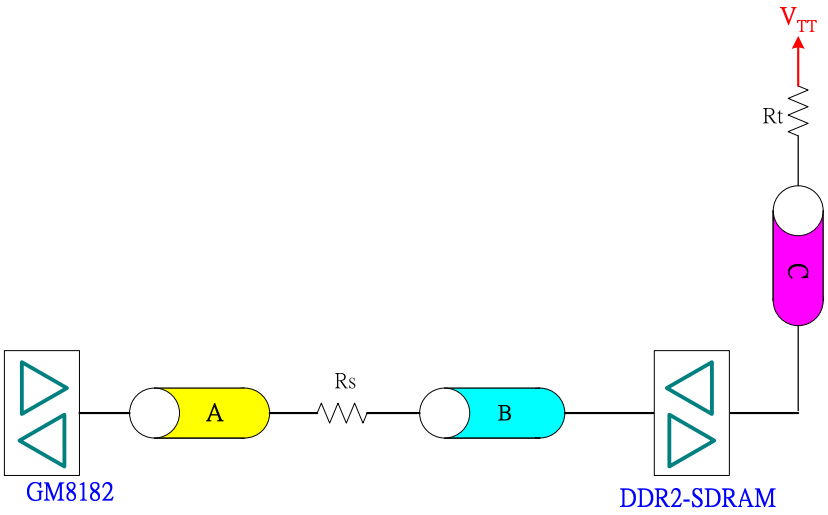
Address/Control Single-end trace impedance: 50 ohms +/- 15%



Signal	Typical	Unit
Trace width	5	mils
Address/Control to other Address/Control trace spacing (S1)	>12	mils
Address/Control to other DDR2-SDRAM trace spacing (S2)	>20	mils

Routing Specification:

Parallel Termination **Rt = 51 ohms +/- 10% (with Termination)**
Series Termination **Rs = 22 ohms +/- 5% (with Termination)**
Series Termination **Rs = 56 ohms +/- 5% (without Termination)**



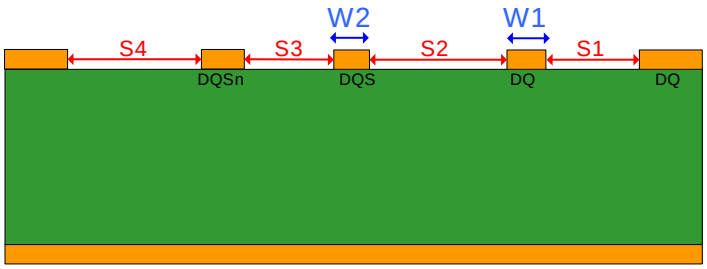
Description	Minimum Length	Maximum Length	Unit
Breakout from BGA (A)	0	0.5	inch
Lead in DDR2 (B)		8	inch
V_{TT} (C)	0.1	0.5	inch
Address/Control bus group mismatch		100	mil
Address/Control to CLK/CLKn signals mismatch		100	mil

4.3 DQS and DQ Impendence and Routing

The ultimate purpose of DQS and data pins layout is to define the trace and bus group width/space, maximum length and impendence.

Trace Impedance:

DQ Single-end trace impedance: 50 ohms +/- 15%
DQS/DQSn Differential trace impedance: 100 ohms +/- 15%

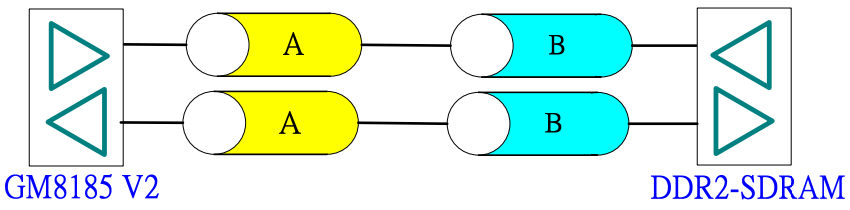


Signal	Typical	Unit
DQ and DQS/DQSn Trace width (W1) (W2)	5	mils
DQS and DQSn Trace Spacing (S3)	13	mils
DQ to other DQ trace spacing (S1)	>12	mils
DQ to other DDR2-SDRAM trace spacing (S2)	>20	mils
DQS/DQSn to other DDR2-SDRAM trace spacing (S4)	>20	mils

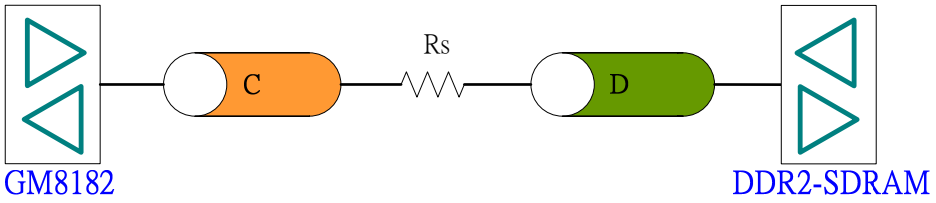
Routing Specification:

Parallel Termination **Rt = 51 ohms +/- 10% (with Termination)**
Series Termination **Rs = 22 ohms +/- 5% (with Termination)**
Series Termination **Rs = 56 ohms +/- 5% (without Termination)**

DQS/DQSn Routing



DQ Routing



Description	Minimum Length	Maximum Length	Unit
DQS/DQSn Breakout from BGA (A)	0	0.5	inch
DQS/DQSn Lead in DDR2 (B)		8	inch
DQ Breakout from BGA (C)	0	0.5	inch
DQ Lead in DDR2 (D)		8	inch
DQS and DQSn mismatch	0	40	mil
DQ bus group signals mismatch		100	mil
DQ and DQS lines respect to the CLK/CLKn signals mismatch		600	mil

Chapter 5

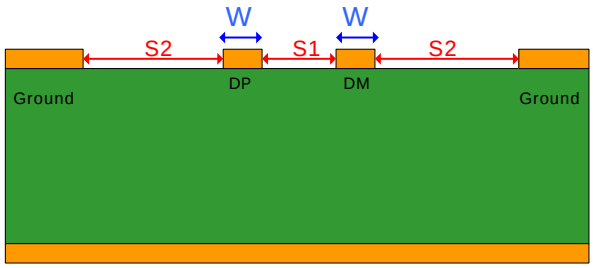
USB

This chapter contains the following sections:

5.1 USB2.0 Impendence Control

The ultimate purpose of USB2.0 layout is to define the trace width/space and impendence.

DP/DM Single-end trace impedance: 45 ohms +/- 15%
DP/DM Differential trace impedance: 90 ohms +/- 15%

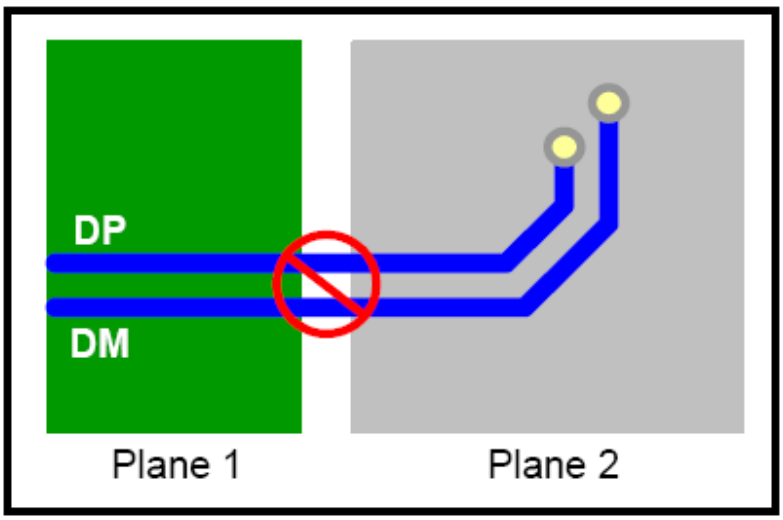


Signal	Minimum	Typical	Maximum	Unit
USB DP and DM trace width (W)		8		mils
DP and DM Trace Spacing (S1)		18		mils
DP/DM to other Trace Spacing (S2)				mils
DP and DM Trace Skew	0		25	mils

5.2 USB2.0 PCB Layer Stack up and Differential Pair Routing

In USB 2.0 applications, a PCB with a minimum of 4 layers is required. This is done to control the USB 2.0 differential signal pair impedance and supply a clear power and ground.

Route the USB 2.0 differential signal pair traces over continuous ground and power planes. Avoid crossing anti-etch areas or any break in the underlying planes. Don't route the USB 2.0 differential signal pair under crystal, oscillator. And clock synthesizers, magnetic devices or ICs. Doing so will cause interference.



Chapter 6

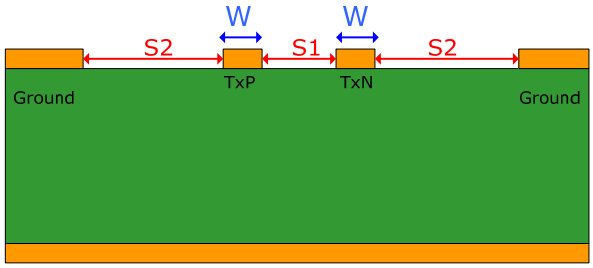
SATA

This chapter contains the following sections:

6.1 SATA Impendence Control

The ultimate purpose of SATA layout is to define the trace width/space and impendence.

TxP/TxN Single-end trace impedance: 47.5 ohms +/- 15%
TxP/TxN Differential trace impedance: 95 ohms +/- 15%

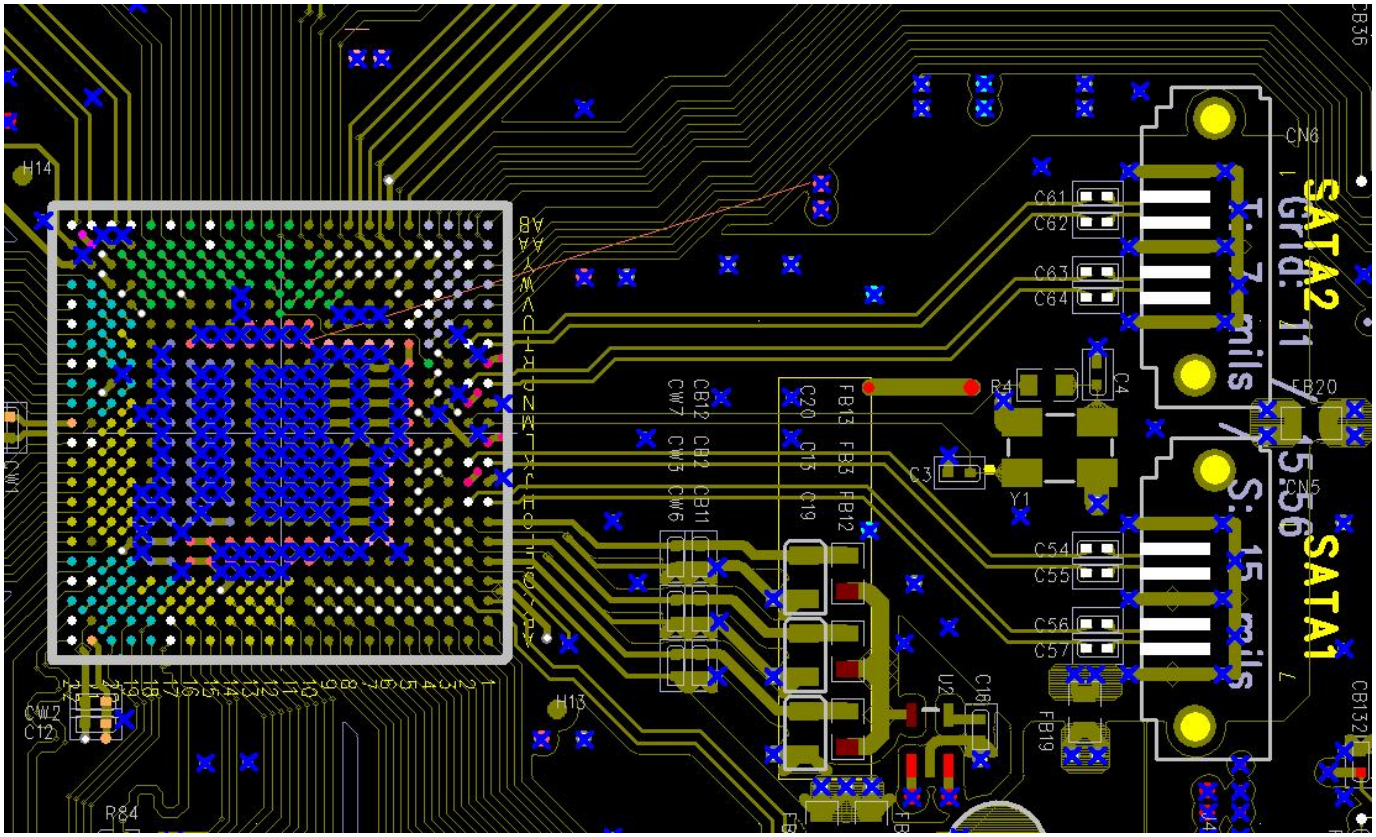


Signal	Minimum	Typical	Maximum	Unit
SATA TxP and TxN trace width (W)		7		mils
TxP and TxN Trace Spacing (S1)		15		mils

6.2 SATA PCB Layer Stack up and Differential Pair Routing

In SATA applications, a PCB with a minimum of 4 layers is required. This is done to control the SATA differential signal pair impedance and supply a clear power and ground.

Route the SATA differential signal pair traces over continuous ground and power planes. Avoid crossing anti-etch areas or any break in the underlying planes. Don't route the SATA differential signal pair under crystal, oscillator. And clock synthesizers, magnetic devices or ICs. Doing so will cause interference.



Chapter 7

Miscellaneous

This chapter contains the following sections:

7.1 I2S Bus Routing

To prevent crosstalk and skew effect on I2S signal, some recommendations are listed as below:

- Add GND shielding for I2S_MCLK is better.
- I2S_MCLK make spacing/width≧2 at least, expect the export trace out of IC pins.