CHAPTER 1. OVERVIEW

This section describes abstracted information of the GM82C700.

1.1 GENERAL DESCRIPTION

The GM82C700 is a single chip SCSI host adapter that is applied to peripheral devices controlled by PC/AT or equivalent microprocessors. This chip is one 80-pin QFP or 68-pin PLCC package and include function blocks to satisfy SCSI protocol. This chip can be implemented to personal computers such as laptops, portables, and so on. Prominence of SCSI is famous for its maximum data transfer rate of upto 10MBytes/sec. and maximum device connectivity of upto eight devices per one SCSI bus. If any computer system is designed with SCSI host adapter, it is free to add new device because of the fact that SCSI protocol supports various devices such as hard drives, high-capacity floppy drives, tape drives, CD-ROM, DAT, removable drives, and so on, the each device controllers may control upto eight physical devices.

The GM82C700 offer the advantage of reliability and cost, and it can replace host adapter card used before. This advantage is prominent in laptop and notebook which is constrained with the number of system I/O slot. The GM82C700 supports both slave DMA and programmed I/O. It has internal 128-byte data buffer to maximize performance of data transfer in host side. The GM82C700 supports both asynchronous and synchronous transfer in SCSI side. Built-in 'Power-Save' mode decrease power consumption by stopping clock supply to the internal logic.

Softwares that is made for the purpose of enough application of Disconnect/Reconnect characteristic of SCSI bus is supported under multi-tasking operation system. Under such environment, CPU can do other job during SCSI device is performing time consuming job such as 'SEEK'. The GM82C700 has high flexibility by supporting various options that can revise with software.

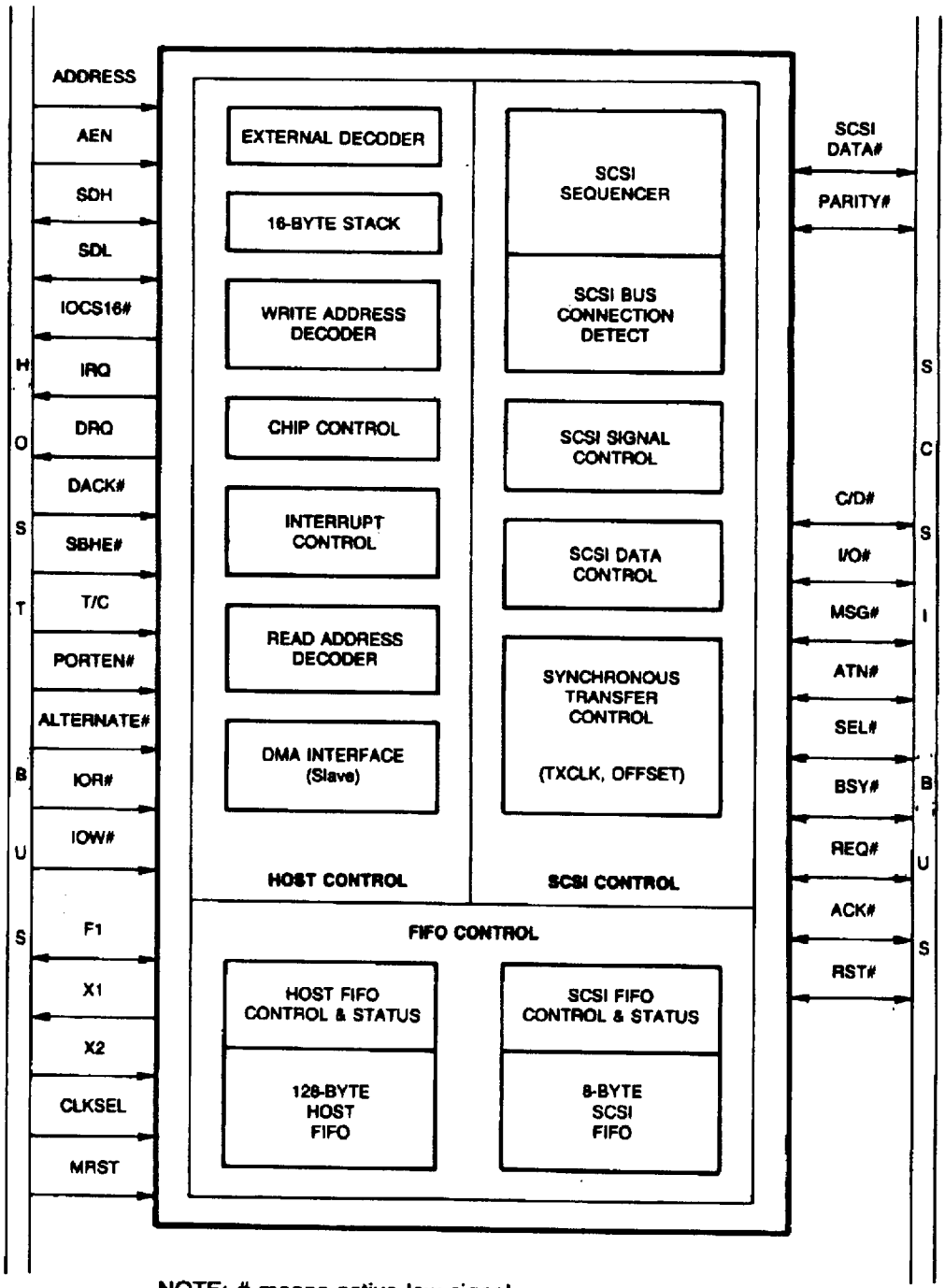
Originally the GM82C700 is designed as an initiator, but it supports target mode also. So the GM82C700 can be used in target system such as LBP or processor device. Internal hardware blocks such as transfer counter, ID register and I/O pins are designed for that the GM82C700 can operates as either an initiator or target.

1.2 FEATURES

- Single chip solution for SCSI bus controller
- 80-pin QFP/68-pin PLCC
- Support second party DMA transfer or programmed I/O
- Support synchronous or asynchronous SCSI transfer
- Support a full complement of SCSI driver software
- Contain an 128-byte host data buffer
- Contain an 8-byte SCSI data buffer
- 32-byte hardware stack
- Built-in "Power-Save" mode
- Data transfer rate upto 10 MByte/sec
- Operation frequency of upto 20 MHz
- Programmable configuration options
  - Enable or Disable Disconnect/Reconnect feature
  - At bus ON/OFF time
  - Selection Time Out period
  - Enable or Disable Parity Checking characteristic
  - SCSI ID
  - Transfer mode of DMA or PIO
  - Synchronous Negotiation

1.3 BLOCK DIAGRAM

Following Figure represent simplified block diagram of the GM82C700.



NOTE: # means active low signal.

CHAPTER 2. PIN INFORMATION

This section describes detailed PIN information of the GM82C700.

2.1 PIN CONFIGURATION

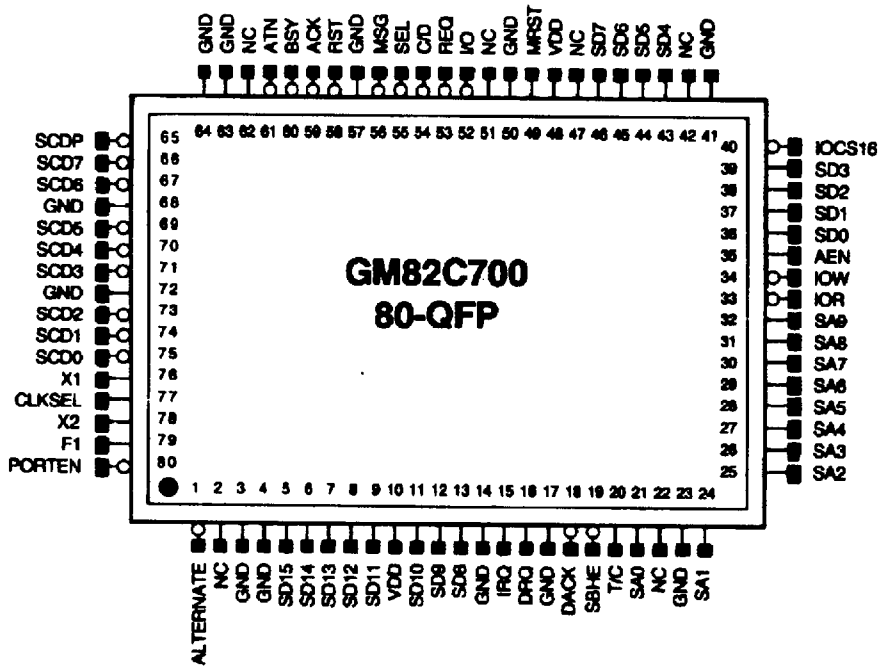


Figure 2.1 Pinout for 80-pin QFP

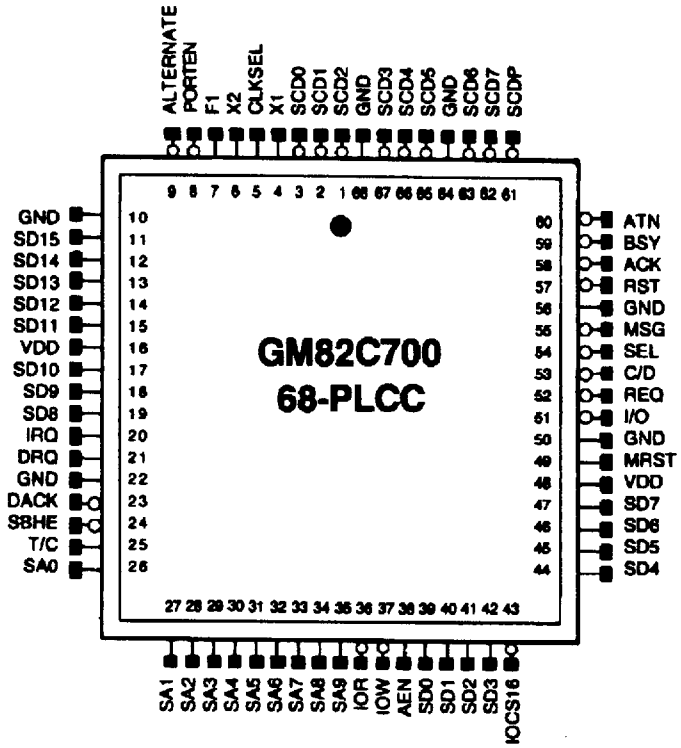


Figure 2.2 Pinout for 68-pin PLCC

2.2 PIN DESCRIPTION

1) Host Interface

SIGNAL NAME	PIN NUMBER		TYPE	DESCRIPTION
	80-PIN	68-PIN		
SD0-SD7	36-39 43-46	39-42 44-47	I/O	Low Order System Data Byte Lines. Utilize tri-state drivers (IOH = -8mA, IOL = 24mA).
SD8-SD15	5-9 11-13	17-19 11-15	I/O	High Order System Data Byte Lines. Utilize tri-state drivers (IOH = -8mA, IOL = 24mA).
ALTERNATE#	1	9	I	Alternate I/O Address Decode. When tied high, chip addresses are decoded from 340h. When tied low, chip addresses are decoded from 140h.
SA0-SA9	21 24-32	26-35	I	System Address Bus. Used to load addresses into the GM82C700 from the host.
AEN	35	38	I	Address Enable. Indicate the type of transfer taking place across the Host bus. Low for I/O access, High for DMA transfer.
IOW#	34	37	I	I/O Write. Indicate the direction of data transfer across the Host bus. When asserted (active low), it indicates data is being written into the GM82C700.
IOR#	33	36	I	I/O Read. Indicate the direction of data transfer across the Host bus. When asserted (active low), it indicates data is being read out of the GM82C700.
IRQ	15	20	O	Interrupt Request. Indicate the occurence of a condition requiring host intervention. This signal is used for all SCSI interrupts. IRQ utilize a two-state drivers (IOH = -8mA, IOL = 24mA).
DRQ	16	21	O	DMA Request. Indicate that the GM82C700 has data to send or is ready to received data. This is one of DMA handshake signals. Valid for DMA mode only. This pin utilize a two-state drivers (IOH = -8mA, IOL = 24mA)
DACK#	18	23	I	DMA Acknowledge. Indicate that the host is ready for a DMA transfer. This is another DMA handshake signal.
T/C	20	25	I	Terminal Count. Indicate the completion of a DMA transfer.This is driven by the host DMA controller, host DMA controller.
SBHE#	19	24	I	System Bus High Enable. Indicates that data on the SD8-SD15 lines is valid.
IOCS16#	40	43	O	I/O Chip Select 16. Driven low when the current I/O data transfer is 16 bits (one word) wide. Open collector driver, IOL = 24mA.

2.2 PIN DESCRIPTION (Continued)

SIGNAL NAME	PIN NUMBER		TYPE	DESCRIPTION
	80-PIN	68-PIN		
PORTEN	80	8	O	Port Enable. An address decode for an external port driver. Address bits 1-9 are included in this signal decode along with AEN. Address bit 0 must be decoded externally decoded with IOR and IOW. (Two state drive: IOL=2mA)
MRST	49	49	I	Master Reset. Used to restore the GM82C700 its start-up condition. This signal is active high at power up or hard reset. This signal has hysteresis for noise immunity. (1.5V < Vth+ < 2.0V; 0.6V < Vth- <1.1V; Vth+ - Vth- = 0.4V)

2) SCSI Bus Interface

SIGNAL NAME	PIN NUMBER		TYPE	DESCRIPTION	
	80-PIN	68-PIN			
SCD0#-SCD7#	66,67 69-71 73-75	1-3 62,63 65-67	I/O	SCSI Data Bus. Used to transfer data between the GM82C700 and devices on the SCSI Bus. Data transfer include SCSI commands, status, messages, and user data.	
SCDP#	65	61	I/O	SCSI Data Parity. Used to check for data transfer error on the SCSI Bus with odd parity.	
ATN#	61	60	I/O	SCSI Attention. Driven if initiator mode and detected if target mode.	
BSY#	60	60	I/O	SCSI Busy. Indicates that SCSI bus is being used.	
SEL#	55	54	I/O	SCSI Select. Used for SCSI device selection.	
ACK#	59	58	I/O	SCSI Acknowledge. This signal forms half of the SCSI data transfer handshake. Driven if initiator mode and detected if target mode.	
REQ#	53	52	I/O	SCSI Request. This signal forms half of the SCSI data transfer handshake. Driven if target mode and detected if initiator mode.	
RST#	58	57	I/O	SCSI Reset.	
MSG#	56	55	I/O	SCSI Message.	Indicate SCSI bus Phase. Driven if target mode and detected if initiator mode.
C/D#	54	53	I/O	SCSI Command/Data.	
I/O#	52	51	I/O	SCSI Input/Output.	

All SCSI lines utilize open collector drivers. (IOL=48mA, input hysteresis=0.2V)

2.2 PIN DESCRIPTION (Continued)

3) CLOCK and POWER

SIGNAL NAME	PIN NUMBER		TYPE	DESCRIPTION
	80-PIN	68-PIN		
X1	76	4	I	Crystal Input. 20Mhz crystal input for internal oscillator.
X2	78	6	O	Crystal Output. 20Mhz crystal output for internal oscillator.
CLKSEL	77	5	I	Clcok Select. This pin selects the clock source. If tied to VDD, the internal oscillator circuit is selected as the clock. If left to float, external clock source via F1 pin is selected as the clock.
F1	79	7	I/O	Clock Input/Output. This pin is either a clock input or clock output, depending on the condition of CLKSEL. If CLKSEL is tied high, it is clock output. If CLKSEL is left to float, it is the clock input for the GM82C700.
VDD	10,48	10,48	I	5-Volt Power Supply. Maximum variation is 5%.
GND	3,4,14 17,23 41,50 57,63 64,68 72	10,22 50,56 64,48	I	Ground.

Signals marked with # are active low.

CHAPTER 3. FUNCTIONAL INFORMATION

This section describes detailed functional information of the GM82C700.

3.1 GENERAL INFORMATION

The GM82C700 is a single chip SCSI solution for PC AT Host Adapter applications with which the features and advantages of SCSI can realized in PC AT systems. The GM82C700 provides all of the functionality necessary to implement a SCSI interface in one 80-pin QFP package. The GM82C700 can be used in small computer systems such as laptops, notebooks, and desktop computers.

The GM82C700 can be configured to operate as either a SCSI initiator or target with asynchronous or synchronous SCSI data tranfer modes through its register based host interface. To minimize host intervention, SCSI data transfers may be performed using "SCSI Full Automatic" transfer mode. The host may have complete control over SCSI data transfers by selecting "SCSI Manual" or "SCSI Half Automatic" tranfer mode alternatively.

Data transfers over the host bus may be accomplished using either "PIO" or "DMA" transfers. The GM82C700 can be configured to generate interrupts for all timing critical SCSI operations. To simplify the setup of two general purpose I/O ports (PORT A and PORT B), the GM82C700 also provides a decoded address output. To aid in programming, the chip provides a 16-byte stack which is controllable by the host processor.

3.2 FUNCTIONAL DESCRIPTION

This section described the major functional components of the GM82C700. There are eight major function components such as SCSI Controller, SCSI Interrupts, SCSI Selection/Reselection Autoconnect Sequencer, SCSI FIFO, Address Mapping and External Decode, Stack, Host Interface, Host FIFO.

The SCSI controller is the major component of GM82C700's hardware. It manages the interface to the SCSI bus including control of SCSI data transfers and sequencing of all SCSI control signals, with intelligence.

The SCSI controller can perform most of the lower level operations necessary to control the SCSI bus for itself. However, the host processor can directly manages and controls the SCSI bus data and signals if desired.

SCSI interrupts are available for all timing critical operations. The interrupt circuitry provides individual masking or clearing the status of any interrupt condition. Refer to the "INTERRUPTS" part later in this section or "REGISTER DESCRIPTIONS" of later section for more detailed information on interrupts in the GM82C700.

The SCSI Selection/Reselection Autoconnect Sequencer is a part of SCSI Controller. With the aid of this section, the GM82C700 can arbitrate automatically perform either a Selection or Reselection sequence. The SCSI SEQUENCE CONTROL REGISTER is set with appropriate value to accomplish these automatic sequence. Note that the SCSI ID REGISTER must be loaded with proper own and other device's ID value prior to starting an autoconnect sequence.

The SCSI FIFO is an 8-byte data buffer. It is used during "SCSI Full Automatic" data transfer mode only. Its main purpose is to buffer during synchronous data transfers, allowing synchronous offsets of up to 8. The SCSI FIFO is not used when "SCSI Manual" or "SCSI Half Automatic" data transfer mode is selected. Typically, above two transfer modes are used for Message In, Message Out, Status or Command phase and synchronous operation is prohibited for those phases. The status of the SCSI FIFO can be monitored by reading the SCSI STATUS 2 REGISTER, 34Dh.

The GM82C700 maps its internal registers onto the PC AT bus by decoding 10-bit of system address input to the chip (SA9-SA0) for one of two alternative I/O address ranges, 140h-15Fh or 340h-35Fh. This scheme allows the GM82C700 directly connect to the PC AT I/O bus with no more external devices required. The ALTERNATE input signal controls the selection of which range to decode for. Through these I/O address locations, the host processor monitors and/or controls all GM82C700 operations and data transfers by reading and writing GM82C700's internal registers.

As part of the address mapping function, the decode logic also generates an off chip signal, PORTEN, which is active low whenever either address 35Ah or 35Bh is selected (15Ah or 15Bh if the alternate address range is chosen).

With the PORTEN signal combined with some off chip logic as shown in "External Port Decode" later in this section, the user can take an easy means to implement two general purpose I/O ports (PORT A and PORT B).

To aid in programming, a 16-byte on-chip stack is available. The host processor can write stack pointer which is located in register 353h and write/read stack data which is located in register 35Dh.

The host interface consists of 32 read/write register locations internally mapped by the GM82C700 as described earlier. Through them, the host processor may monitor or control all aspects of GM82C700 operation.

The GM82C700 has an internal 128-byte data FIFO to buffer data between the host and the GM82C700 to facilitate data transfer performance. The Host FIFO is used during either "PIO" or "DMA" data transfers provided that "SCSI Full Automatic" data transfer mode is also selected. Otherwise if "SCSI Manual" or "SCSI Half Automatic" transfer modes are selected, host data is transferred directly to/from the SCSI data latch located in register 346h. The Host FIFO is 8-bits wide with conversions to 16-bit words performed as required by internal data path logic. Host FIFO operations may be monitored by reading the HOST STATUS REGISTER, 354h and HOST FIFO STATUS REGISTER, 355h.

3.3 SCSI DATA TRANSFERS

The GM82C700 operates as a SCSI initiator by loading the SCSI SEQUENCE CONTROL REGISTER with the proper values. To configure the chip for initiator modes, refer to the "Application Notes" of chapter 5. The GM82C700 can support both asynchronous and synchronous data transfers between two SCSI devices across the SCSI bus. To assist in data transfer control, a 24-bit transfer counter is available which will count up for each SCSI bus REQ/ACK handshake and generate an interrupt or status condition when maximum count value is reached.

Data transfers from the GM82C700 to the SCSI bus can be performed using one of three data transfer modes. Note that operational status in each mode can be monitored through interrupts or by polling for status.

- SCSI Manual: The host processor controls all aspects of the SCSI interface. SCSI bus control signals are controlled by the host processor via SCSI SIGNAL REGISTER located in 343h, and SCSI data is controlled via SCSI LATCHED DATA located in 346h. The GM82C700 acts as a SCSI bus buffer only.
- SCSI Half Automatic: The host processos provides most of the control. The SCSI data is controlled by the host processor via SCSI LATCHED DATA located in 346h. The GM82C700 provides automatic SCSI bus REQ/ACK handshaking.
- SCSI Full Automatic: Utilizing the intelligence of the GM82C700, this allows the host processor to off load the SCSI transfer operation of the GM82C700. The GM82C700 will run the SCSI interface and keep track of the transfer count after being initially set up by the host processor. This mode allows use of the GM82C700 internal FIFOs for maximum transfer performance.

In SCSI manual mode, the host processor reads or writes directly to the SCSI data bus via the latch at 346h and can monitor or control the SCSI bus control lines via the register at 343h. In this mode, the GM82C700 is essentially a bus buffer having no control functions. Note that SCSI Manual mode supports asynchronous SCSI transfers only and that the internal FIFOs are not used. This mode is typically used for SCSI Command, Message, or Status phase where decision making and control are of primary importance rather than data transfer speed. To select this mode, set SPIOEN = 0 & FFTXEN = 0 in the SCSI Transfer Control 0 Register, 341h.

In SCSI half automatic mode, the host processor writes or reads from the SCSI data bus via the latch at 346h, with the GM82C700 handling the REQ/ACK handshaking to transfer data across the SCSI bus. The P_RDYS bit in the SCSI Interrupt Status 0 Register at 34Bh signals transfer completion and can be polled or set to generate an interrupt. This mode supports asynchronous SCSI transfers only and bypasses the internal data FIFOs.

This mode is typically used for SCSI Command, Message, or Status phase where decision making and control are of primary importance rather than data transfer speed. To select this mode, set SPIOEN = 1 & FFTXEN = 0 in the SCSI Transfer Control 0 Register, 341h.

In SCSI full automatic mode, the GM82C700 will automatically handle the SCSI data transfer and provide the fastest transfer performance. In this mode, the internal FIFOs used and the data path through the chip is from the host bus, through the host FIFO, through the SCSI FIFO and finally out onto the SCSI bus. This mode will support both asynchronous and synchronous SCSI transfers. This mode usually used during the Command and Data phases on the SCSI bus. To select this mode, set SPIOEN = 0 & FFTXEN = 1 in the SCSI Transfer Control 0 Register, 341h. The control for synchronous SCSI transfers are located in the SCSI RATE & OFFSET CONTROL REGISTER, 344h.

3.4 HOST PROCESSOR DATA TRANSFERS

Data transfers between the host bus and the GM82C700 can take place using either of the following two modes:

- PIO : Through Programmed I/O the host processor handles the data transfer into/out of the GM82C700.
- DMA : Data transfers between the host and the GM82C700 are run by DMA controller in the host system.

Selection of host data transfer mode is controlled through the HOST TRANSFER CONTROL 0 REGISTER, 352h.

In PIO mode, the host processor writes to or reads from the 128-byte host FIFO via the 16-bit data register at 356h. By taking advantage of the Repeat Insuring instruction found in i80X86 processors, very high data transfer rates are possible.

In DMA mode, the host processor sets up the data transfer operation by loading a system DMA controller with a memory pointer and the transfer count. The host DMA controller then writes or reads data to or from the GM82C700 host FIFO via the data register at 356h. Once begun, host DMA transfers run to completion without further host processor intervention. In the GM82C700, only 8-bit DMA transfers are available.

3.5 INTERRUPTS

The GM82C700 can be configured to generate interrupts for all transfer critical conditions. Interrupts are controlled through a set of internal registers as shown in Table 3-1. Each interrupt condition has a readable status bit and controlling enable and clear bits.

The status bit reflects the current state of the interrupt source independent of interrupts being enabled. It may be read by the host processor at any time to obtain a real time indication of the condition. Removing the condition that caused the status bit to be latched does not always clear the status bit. Refer to the descriptions of the status bits and their corresponding clear bit to determine the exact conditions under which they are cleared.

TABLE 3-1. INTERRUPTS

Status Name	Status Register	Enable Register	Clear Register
SELODS	34B_6 read	350_6 write	34B_6 write
SELIDS	34B_5 read	350_5 write	34B_5 write
SELOBS	34B_4 read	350_4 write	34B_4 write
SWRAPS	34B_3 read	350_3 write	34B_3 write
P_RDYS	34B_1 read	350_1 write	34B_1 write
DMADOS	34B_0 read	350_0 write	34B_0 write
HWSTOS	34C_7 read	351_7 write	34C_7 write
RSTINS	34C_5 read	351_5 write	34C_5 write
PHSERS	34C_4 read	351_4 write	n/a
BFREES	34C_3 read	351_3 write	34C_3 write
PARERS	34C_2 read	351_2 write	34C_2 write
PHSCHS	34C_1 read	351_1 write	34C_1 write
REQINS	34C_0 read	351_0 write	34C_0 write
SWINTR	352_0 read	352_2 write	352_0 write

The enable bit gates the entry of the status bit into the interrupt processing chain and essentially serves as an interrupt mask. In order for a condition to cause an interrupt, its enable bit must be set, otherwise the interrupt associated with the condition is suppressed.

The clear bit resets the interrupt latch corresponding to the particular interrupt condition. The interrupt latch will be set if the corresponding enable bit was set allowing the status bit condition to propagate. By clearing the interrupt latch, the interrupt condition will be removed from generation of the interrupt signal output on the IRQ pin. In some cases, the clear bit will also clear the status bit, but not always. Refer to the descriptions of each status bit to determine the exact conditions under which they are cleared.

All of the interrupt sources shown in Table 3-1 are logically ORed to form the signal output on the IRQ pin. The OR of all these sources is available for monitoring on the INTRST status bit in the Host Status Register at 354h. A master enable is also available to gate the signal going out on the IRQ pin. If the INTREN bit of the 352h is reset, no interrupts will be output on the IRQ pin. INTRST is valid even if the INTREN bit is reset.

3.6 EXTERNAL PORT DECODE

Within the GM82C700's internal address range, the chip enables for two addresses, 35Ah, and 35Bh (15Ah & 15Bh if alternate address is selected) are output on the PORTEN pin instead of being used internally, in order to provide a convenient way to add general purpose I/O ports external to the GM82C700. These external ports may be used for control outputs or configuration input, in conjunction with general GM82C700 SCSI operation. By combining the active low PORTEN output with the I/O bus IOW, IOR and SA0 as shown in Figure 3-1, select signals for up to two read and two write bus tranceivers are easily generated.

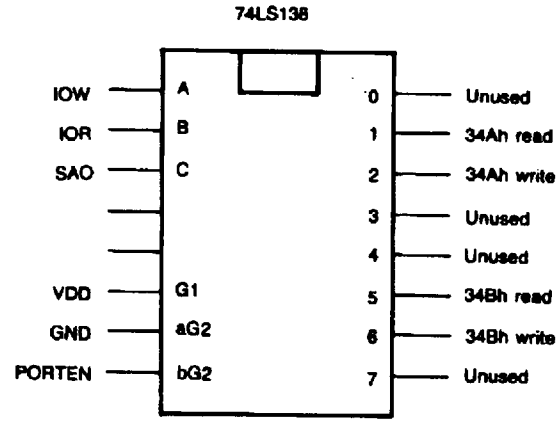


FIGURE 3-1. TYPICAL EXTERNAL DECODER

3.7 CLOCKING

A clocking source of up to 20 MHz is required in order to operate the GM82C700. It may be supplied externally or the internal crystal oscillator circuit may be used.The advantage of using an external source is that power saving of up to 30 percent of total GM82C700 power consumption may be realized by shutting down the internal oscillator circuits.

The CLKSEL pin controls which clocking source is used. To use the internal oscillator, the CLKSEL pin must be tied to +5Vdc in order to supply a power source to the internal oscillator circuits. In addition, a crystal of up to 20 MHz must be connected to the X1, X2 pins. The generated clock signal will also be output on the F1 pin for use elsewhere if desired. To input an external clocking signal, the internal oscillator circuits must be powered down by disconnecting the CLKSEL pin. Internally, CLKSEL will be grounded by a pull down resister, or more preferably should be externally grounded. By powering down the oscillator circuits, the direction of the F1 buffer is changed, allowing the input of the external clocking source. The external clocking source should ideally have a 50% duty cycle with a minimum of 40/60 acceptable. Voltage input requirements are TTL levels.

The GM82C700 may operate with a clock frequency of less than 20 MHz although all timing parameters must be derated for the slower operation.

3.8 POWER MANAGEMENT

One of the most important feature of the GM82C700 is the ability to allow to the user to manage chip power consumption. Power consumption in the GM82C700 can be functionally organized as three major components as shown in Figure 3-2. Power component A is drawn by the bulk of the GM82C700 circuits and may be turned off during periods of inactivity by activating the 'Power-Save' mode of operation. Power component B is used to operate the on board crystal oscillator circuit. It can be avoided entirely by using an external clock source input on the F1 pin. Power component C is made up of current used to maintain the Host Processor interface in order to allow constant access to the GM82C700 control registers by the Host Processor. It is the minimum amount the chip can draw while still maintaining Host Processor control and access.

Power Components	Block Name	Power Ratio
A	Core Control Logic	50%
B	Crystal Oscillator	30%
C	Host(CPU) Interface	20%

FIGURE 3-2. POWER COMPONENTS

During periods of inactivity, the GM82C700 may be shut down by the Host Processor to achieve power saving. 'Power-Save' Mode works by shutting off the clock to the bulk of the GM82C700 circuits. Removing the clock reduces power to a static level, saving power component B. Power-Save is entered by setting bit 7 (PWRDWN) of the 353h register and exited by either resetting the bit or performing a chip master reset. Note that during powersave, the GM82C700's Host Processor interface circuits are still active, allowing manipulation of the GM82C700 register set by the Host Processor. If no GM82C700 operations at all are expected, the chip may shut down entirely by turning off all clock sources to the chip. As long as the power supply vaoltage is maintained, the GM82C700 will statically maintain all register values. Note that during powersave, no SCSI operations can be performed or responded to. To minimize power consumption, the GM82C700 software device driver and BIOS available from GoldStar implement 'Power-Save' as described.

CHAPTER 4. REGISTER DESCRIPTION

This section describes detailed information for internal registers of the GM82C700 which are located in 32 address range, from 340h to 35Fh or from 140h to 15Fh. Each register has its own functions and can be written and read by the host processor via the host data bus.

4.1 SCSI SEQUENCE CONTROL

This register can be written and read by the host processor via the host data bus and its address is 340H or 140H. This register controls the non-information transfer phase i.e. from bus free phase to selection or reselection phase. Higher 4-bits in this register controls the operation mode of Selection/Reselection process for the GM82C700. When SCSI reset signal is asserted, all bits except SCRSTO are cleared. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	TARGET	SELOEN	SELTEN	SELIEN	ATNOEN	ATNIEN	ATNPEN	SCRSTO
DEFAULT	0	0	0	0	0	0	0	0

Enable Target Device Mode(TARGET) bit controls the role of the GM82C700. The GM82C700 operates as a target device by setting this bit to "1". For the case of host adaptor, this bit should be set to "0" because the GM82C700 operates as an initiator role.

Enable Selection Out Attempt (SELOEN) bit determines whether attempt to arbitrate or not. When set and if 'enable target device mode' bit is defined as "0", the GM82C700's SCSI logic performs a Selection sequence as Initiator and select a Target. When this bit is set and if 'enable target device mode' bit is set to "1", the GM82C700's SCSI logic performs a Reselection sequence as a Target device and reselect an Initiator. There are two status bits, 'selection initiated out status' and 'status of selection out done' located in 34Bh, for reporting the status of selection/reselection sequence to the host processor.

Enable Selection In(SELTEN) bit controls response of the GM82C700 when selected. When set, it allows the GM82C700 to respond to valid Selection sequence. There is a status bit, 'status of selection in done' located in 34Bh, for reporting the status of selection/reselection sequence to the host processor.

Enable Reselection In(SELIEN) bit controls response of the GM82C700 when reselected. When set, it allows the GM82C700 to respond to valid Reselection sequence. There is a status bit, 'status of selection in done' located in 34Bh, for reporting the status of selection/reselection sequence to the host processor.

Assert ATN On Selection Out(ATNOEN) bit controls assertion of ATN signal by initiator to transfer message to the selected target. When set, ATN is assreted during Selection Out Sequence. The process can deassert ATN by setting 'clear ATN out signal' bit in the register of address 34Ch. If SCSI bus goes to Bus Free state, it forces to all SCSI devices to deasserts ATN. Clearing this bit does not deassert ATN.

Assert ATN On Selection In(ATNIEN) bit controls assertion of ATN signal by initiator to transfer message to the target which reselect this initiator. When set, ATN is asserted during Reselection In Sequence. Deassertion conditions are same as above description.

Assert ATN On Parity Error(ATNPEN) bit controls assertion of ATN signal by initiator to transfer message to the selected target when parity error is detected. When both this bit and 'parity check' bit located in 342h are set, ATN signal is asserted if a parity error is detected on SCO-SC7 during the Data In, Message in, or Status In phases. Deassertion conditions are same as above description.

SCRSTO: SCSI Reset Out(SCRSTO) bit determines assertion of RST signal on the SCSI bus. When set, RST is asserted on the SCSI bus. The process must deassert RST by clearing SCRSTO if abnormal condition is disappeared.

4.2 SCSI TRANSFER CONTROL O

This register can be written and read by the host processor via the host data bus and its address is 341H or 141H. This register controls transfer between the SCSI bus and host, via the SCSI and host FIFOs. This register also controls the selection of SCSI PIO mode as the transfer mode and enables the SCSI FIFO and SCSI transfer counter to clear. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	SCTXEN	FFTXEN	CHANEN	STCRST	SPIOEN	RSVD	CHANRS	RSVD
DEFAULT	0	0	0	0	0	0	0	0

SCSI Transfer Enable(SCTXEN) bit controls transfer between the SCSI bus and the GM82C700's internal SCSI logic. When set, data can be transferred between the SCSI bus and the SCSI FIFO. Transfers are terminated clearing this bit. This bit must be read back as a low before the transfer is considered halted.

Inter FIFO Transfer Enable(FFTXEN) bit controls transfer between two internal FIFOs. When set, transfers between the SCSI FIFO and host FIFO are enabled.

Channel Enable (CHANEN) bit enables data path of the GM82C700. This bit should be always set when the GM82C700 operates as a SCSI device.

Reset Transfer Counter(STCRST) bit controls internal 24-bit transfer counter. When set, the SCSI transfer count is set to zero value. This is self clearing bit.

SCSI PIO Mode Enable (SPIOEN) bit controls SCSI transfer mode. When set, SCSI PIO mode is used as the tranfer mode. Once a SCSI PIO transfer is started, SPIOEN must remain set throughout the entire transfer. If SPIOEN is cleared at any time during the transfer, the transfer will be halted without corrupting valid data in the SCSI data latch.

Reset Channel (CHANRS) bit controls initialization procedure of data path. When set, the SCSI FIFO, and the SCSI transfer counter are cleared.

4.3 SCSI TRANSFER CONTROL 1

This register can be written and read by the host processor via the host data bus and its address is 342H or 142H. This register controls various transfer controls associated with SCSI transfers. This register controls the Selection/Reselection timer, odd byte alignment, and parity checking. Following figure shows the function table for this register.

BIT	7	6	5	4 3	2	1	0
NAME	DUMMYB	WRAPEN	CHKPAR	STOSEL	HWSTEN	ALIGNB	RSVD
DEFAULT	0	0	0	00	0	0	0

SCSI Dummy Transfer (DUMMYB) bit controls dummy transfer of 1-byte unused data to/from the SCSI bus. When set, the GM82C700 reads data from the SCSI bus but does not store or use that data, or write null data of 00h to the SCSI bus. In dummy transfer mode, data is not saved and FIFO full or FIFO empty conditions do not cause transfer halts. This bit cannot be set in test mode.

Transfer Counter Wrap Enable (WRAPEN) bit enables the 24-bit transfer counter to count larger than 2^{24}. When set, the 24-bit transfer counter can wrap past 0. If the amount of data to be transferred is larger than 24-bit maximum value, this bit should be set to "1" until final wrap is reached. Initiator should always set this bit because initiator counts up the amount of data being transferred.

Parity Check(CHKPAR) bit controls parity checking scheme. When set, parity checking is enabled on the SCSI bus. When cleared, "SCSI parity error" status bit located in 34Ch always reads 0.

Timeout Period Selection(STOSEL) field determines the selection timeout values when selected device is not respond. This field contains the selection timeout code. The selection timeout codes are defined as following:

STOSEL	Value	Timeout Period
0	0	256 ms
0	1	128 ms
1	0	64 ms
1	1	32 ms

Hardware Timeout Counter Enable(HWSTEN) bit enables internal selection timeout counter. When set, the hardware selection timer is enabled. When the internal selection timer exceeds the timeout limit during a Selection Out sequence, SEL signal is deasserted and 'Selection timeout expired' status bit located in 34Ch is set. If 'enable HWSTO interrupt' bit located in 351h is cleared, SEL signal will continue to be asserted until deasserted by the processor.

Byte Align(ALIGNB) bit controls dummy handshaking. When set, it forces a handshake between the host FIFO and the SCSI FIFO. Any data passed for this handshake is discarded. This procedure is used to align data when an odd byte boundary disconnect occurs during a write operation.

4.4 SCSI SIGNAL IN

This register can be read by the host processor via the host data bus and its address is 343H or 143H. This register reflects the current state of the SCSI control lines on the SCSI bus except RST signal. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	C_D_IN	I_O_IN	MSG_IN	ATN_IN	SEL_IN	BSY_IN	REQ_IN	ACK_IN
DEFAULT	Undefined							

4.5 SCSI SIGNAL OUT

This register can be read by the host processor via the host data bus and its address is 343H or 143H. If the GM82C700 is an initiator, this register controls the excepted state of the SCSI control lines. If the GM82C700 is a target, this register controls the actual signal values of the SCSI control lines. All bits in this register are cleared by Bus Free, SCSI Reset, or Hard Reset conditions. Following figure shows the function table for this register.

In INITIATOR Mode

BIT	7	6	5	4	3	2	1	0
NAME	C_DEXP	I_OEXP	MSGEXP	ATNOUT	SELOUT	BSYOUT	REQOUT	ACKOUT
DEFAULT	0	0	0	0	0	0	0	0

In TARGET Mode

BIT	7	6	5	4	3	2	1	0
NAME	C_DOUT	I_OOUT	MSGOUT	ATNOUT	SELOUT	BSYOUT	REQOUT	ACKOUT
DEFAULT	0	0	0	0	0	0	0	0

Expected Phase Values(C_DEXP, I_OEXP, MSGEXP) field represent the states of C/D, I/O, MSG excepted for the next REQ pulse in Initiator mode. The C/D, I/O, MSG signals on the SCSI bus are not affected by these bit values.

Phase Signal Out(C_DOUT, I_OOUT, MSGOUT) field controls physical phase of the SCSI bus in target mode. Phase control signals(C/D, I/O, MSG) on the SCSI bus is driven by this field in Target mode.

Other SCSI Signal Out(ATNOUT, SELOUT, BSYOUT, REQOUT, ACKOUT) field controls physical states of each SCSI signals on the SCSI bus. Driving high forces assertion SCSI signal on the SCSI bus. Driving low let internal hardware logic which has some intelligence to drive SCSI signal on the SCSI bus.

4.6 SCSI RATE & OFFSET CONTROL

This register can be written by the host processor via the host data bus and its address is 344H or 144H. This register is used to control the timing and offset parameters for synchronous SCSI transfer. If OFFSET is set to 0, SCSI transfers are asynchronous. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	RSVD	TXRATE			OFFSET			
DEFAULT	0	0	0	0	0	0	0	0

Synchronous Transfer Rate(TXRATE) field represent the synchronous transfer rate code. Following figure shows definition of the transfer rates and associated timing parameters for all valid transfer rate codes. Timing parameters are given for a 20MHz clock. For clock rates other than 20MHz, Timing parameters are given in clock period(T) Transfer rates at less than 2.22MBps must be made in asynchronous mode.

			Handshake Signal		
TXRATE			Active Time	PERIOD	RATE (MBps)
0	0	0	50ns	100ns, 2*T	10.00
0	0	1	50ns	150ns, 3*T	6.67
0	1	0	100ns	200ns, 4*T	5.00
0	1	1	100ns	250ns, 5*T	4.00
1	0	0	100ns	300ns, 6*T	3.33
1	0	1	100ns	350ns, 7*T	2.86
1	1	0	100ns	400ns, 8*T	2.50
1	1	1	100ns	450ns, 9*T	2.22

SCSI Offset Value(OFFSET) field represent the offset value for synchronous transfer except 0h. When this field is set to zero, the SCSI transfer mode is considered as asynchronous. OFFSET must be loaded with the values derived from the SCSI synchronous transfer request negotiations. Valid synchronous offset ranges are 1h through 8h.

4.7 SELECTION/RESELECTION ID

This register can be read by the host processor via the host data bus and its address is 345H or 145H. When the GM82C700 has been reselected, the SCSI ID bits of the target and the initiator are set in this register. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	SEL_ID							

4.8 SCSI ID CONTROL

This register can be written by the host processor via the host data bus and its address is 345H or 145h. This register containes the SCSI IDs of the GM82C700 and the other unit involved in the SCSI operation. If GM82C700 operates as an initiator, OWN_ID field (bits 6-4) contains the initiator ID and OTH_ID field (bits 2-0) contains the target ID. If GM82C700 operates as an target, OWN_ID field (bits 6-4) contains the target ID and OTH_ID field (bits 2-0) contains the initiator ID. Vaild ID value ranges are 0 through 7. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	RSVD	OWN_ID			RSVD	OTH_ID		
DEFAULT	0	X	X	X	0	X	X	X

4.9 SCSI PIO MODE LATCHED DATA

This register can be written or read by the host processor via the host data bus and its address is 346H or 146H. This register is data latch used for manual or SCSI PIO data transfers. In Initiator mode, write_mode_data is written to this register, read_mode_data is read from this register. In Target mode, write_mode_data is read from this register and read_mode_data is written to this register. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	PIOSCD							
DEFAULT	X	X	X	X	X	X	X	X

4.10 SCSI DATA BUS

This register can be read by the host processor via the host data bus and its address is 347H or 147H. This register reflects the current state of the SCSI bus data lines. It is used during manual selection or reselection. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	SCDBUS							

4.11 SCSI TRANSFER COUNTER

This register can be written or read by the host processor via the host data bus and its address is 348h to 34AH or 148H to 14AH. The transfer count register actually comprises three 8-bit registers, SCSI Transfer Count 0, 1, & 2. This register contains the data transfer count for the current SCSI operation. Bit 0 of 348h is the LSB. Bit 7 of 34Ah is MSB. In initiator mode, this register must be cleared by the host processor whenever inter-FIFO transfer is enabled and then counts the number of bytes sent or received, counting up for each ACK pulse received. For transactions involving disconnection and reconnection, this register can be loaded with the current (remaining) transfer count of the transaction. In Target mode, this register is loaded with the number of REQ to send out on the SCSI bus, and then counts the number of bytes sent or received, counting down for each REQ pulse transmitted. When the count value reaches 0, two status bits 'SCSI transfer done status' and 'transfer counter wrap status' bits are set. If there are larger than 2^{24} data to transfer, clear 'transfer counter wrap status' bit via setting 'clear transfer counter wrap' located in 34BH. Following figure shows the function table for these registers.

34AH

BIT	7	6	5	4	3	2	1	0
NAME	STC_HB							
DEFAULT	X	X	X	X	X	X	X	X

349H

7	6	5	4	3	2	1	0
STC_MB							
X	X	X	X	X	X	X	X

348H

7	6	5	4	3	2	1	0
STC_LB							
X	X	X	X	X	X	X	X

4.12 SCSI INTERRUPT STATUS 0

This register can be read by the host processor via the host data bus and its address is 34BH or 14BH. This register reflects the state of eight SCSI status bits. If the interrupts corresponding to these status bits are enabled, interrupts are generated when the status bits are set. Interrupts are enabled using the SCSI INTERRUPT MODE 0 register and cleared using the CLEAR SCSI INTERRUPT 0 register. The status bits in this register are available regardless of the condition of the enable bits. Clearing an interrupt does not necessarily clear the status bit; the means by which a status bit may be cleared is specified for each bit. The clear bits also state specifically when they clear the associated status bit. Refer to the discussion of interrupts in Section 4 of this manual for more information on the interrelation of status, interrupt, enable, and clear bits. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	TMODES	SELODS	SELIDS	SELOBS	SWRAPS	SCTDOS	P_RDYS	DMADOS

Target Mode Selected (TMODES) bit indicates the mode of the GM82C700. This bit is set to "1" when the GM82C700 should be operate as a target and only valid after a reselection or selection has completed and until Bus Free occur.

Status of Selection Out Done(SELODS) bit is set when the GM82C700 has successfully completed Selection Out. This bit will remain a one for the duration of the command in process; it is cleared by Bus Free. This condition generates an interrupt if corresponding interrupt enable bit located in 350h is set.

Status of Reselection in Done(SELIDS) bit is set when the GM82C700 has been reselected. To enable clearing this bit, 'clear reselection in done status' bit located in 34Bh must first be set. Bus Free condition will then clear this bit. This feature allows the initiator to recognize that a Reselection In sequence occured, even if Bus Free occurred before it reads this bit. This condition generates an interrupt if corresponding interrupt enable bit in 350h is set.

Selection Initiated Out Status(SELOBS) bit is set when the GM82C700 begins a Selection Out sequence. This bit is set upon successful arbitration of the bus, and remains set throughout the Selection Out sequences. When the Selection Out sequence has completed, this bit is cleared. This condition generates an interrupt if corresponding interrupt enable bit located in 350h is set.

Transfer Counter Wrap Status(SWRAPS) bit is set when the 24-bit transfer counter (348h-34Ah) wrap past 0, i.e. the transfer counter increments from FFFFFFh to 000000h. This bit is cleared by setting corresponding cler bit located in 34Bh. This condition generates an interrupt if corresponding interrupt enable bit located in 350h is set.

SCSI Transfer Done Status(SCTDOS) bit is valid for Target mode only. SCTDOS is set when 'transfer counter wrap enable' bit located in 342h is "1" and the transfer counter wrap past 0 and cleared by setting corresponding clear bit located in 34Bh. This bit can be set by setting 'set SCSI transfer done' bit located in 34Bh. This condition generates an interrupt if corresponding interrupt enable bit located in 350h is set.

SCSI PIO Ready(P_RDYS) bit is set when data is ready to be transferred on the SCSI bus. This bit is set when REQ is asserted. On outbound transfers, this bit is cleared on a write to the SCSI data latch. On inbound transfers, this bit is cleared on a read from the SCSI data latch. This condition generates an interrupt if corresponding interrupt enable bit located in 350h is set.

DMA Done(DMADOS) bit is only valid in DMA mode. For transfers to the SCSI bus, This bit is set when both the SCSI FIFO and the host FIFO are empty, and terminal count(T/C) has been asserted by the host DMA controller. For transfers from the SCSI bus, DMADOS is set when terminal count(T/C) has been asserted by the host DMA controller. This condition generates an interrupt if corresponding interrupt enable bit located in 350h is set.

4.13 SCSI INTERRUPT STATUS 1

This register can be read by the host processor via the host data bus and its address is 34Ch or 14Ch. This register reflects the state of eight SCSI status bits. If the interrupts corresponding to these status bits are enabled, interrupts are generated when the status bits are set. Interrupts are enabled using the SCSI INTERRUPT MODE 1 register and cleared using the CLEAR SCSI INTERRUPT 1 register. The status bits in this register are available regardless of the condition of the enable bits. Clearing an interrupt does not necessarily clear the status bit; the means by which a status bit may be cleared is specified for each bit. The clear bits also state specifically when they clear the associated status bit. Refer to the discussion of interrupts in Section 3 of this manual for more information on the interrelation of status, interrupt, enable, and clear bit. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	HWSTOS	ATNINS	RSTINS	PHSERS	BFREES	PARERS	PHSCHS	REQINS

Selection Time Out Expired(HWSTOS) bit indicates that selection timer has reached to predefined timeout time. This bit is set when 'hardware timeout counter enable' bit located in 342h is set and a Selection Out time out has occured by hardware selection timer. This bit is cleared by setting corresponding clear bit located in 34Ch. This condition generates an interrupt if corresponding interrupt enable bit located in 351h is set.

Attention In to Target(ATNINS) bit indicates the status of ATN signal on the SCSI bus. This bit is valid in Target mode only. This bit is set when the initiator assert ATN signal to the SCSI bus and cleared when ATN signal deasserted. This condition generates an interrupt if corresponding interrupt enable bit located in 351h is set.

SCSI Reset In(RSTINS) bit indicates the status of RST signal on the SCSI bus. This bit is set when a bus reset occurs on the SCSI bus. This bit remains set until cleared by setting corresponding clear bit located in 34Ch. This condition generates an interrupt if corresponding interrupt enable bit in 351h is set.

Phase Error(PHSERS) bit represent the status of phase error. This bit is set when the expected phase loaded in the SCSI SIGNAL IN register does not match the phase active on the SCSI bus. This bit is qualified by 'request initiated' status bit located in this register. This bit is cleared when the phase active on the SCSI bus matches the expected phase loaded in the SCSI SIGNAL IN register. This condition generates an interrupt if corresponding interrupt enable bit located in 351h is set.

Bus Free(BFREES) bit is set when both BSY and SEL have been negated for bus free delay time defined in SCSI protocol and cleared by setting corresponding clear bit located in 34Ch. This condition generates an interrupt if corresponding interrupt enable bit located in 351h is set.

SCSI Parity Error(PARERS) bit is set when a pairty error detected during an inbound Information Transfer Phase and 'parity check' bit located in 342h is set. If 'parity check' bit is cleared, this bit is always 0. Parity is sampled on the leading edge of REQ. This bit is cleared by setting corresponding clear bit located in 34Ch. After driving PARERC high, SCSIPERR reflects the parity of the last byte transferred on the bus. This condition generates an interrupt if corresponding interrupt enable bit located in 351h is set.

Phase Changed(PHSCHS) bit is set when the expected phase loaded in the SCSI Signal In register does not match the phase active on the SCSI bus. This bit is cleared by setting corresponding clear bit located in 34Ch. This condition generates an interrupt if corresponding interrupt enable bit in 351h is set.

Request Initiated(REQINS) bit is set when the GM82C700 detects the leading edge of REQ. This bit is cleared when ACK is asserted on the bus, or when corresponding clear bit located in 34Ch is set. This condition generates an interrupt if corresponding interrupt enable bit located in 351h is set.

4.14 CLEAR SCSI INTERRUPT 0

This register can be written by the host processor via the host data bus and its address is 34Bh or 14Bh. This register cleares the interrupts associated with the status bits in SCSI STATUS 0 register. Setting any of these bits clears the corresponding interrupt and deassert IRQ. IRQ may not be deasserted if there are other interrupts active. A clear bit does not need to be cleared before it can be set again. Writing a zero to any bit in this register has no effect. Clearing an interrupt does not necessarily clear the status bit associated with the condition which cause the interrupt. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	SSCTDO	SELODC	SELIDC	SELOBC	SWRAPC	SCTDOC	P__RDYC	DMADOC
DEFAULT	1	1	1	1	1	1	1	1

Set SCSI Transfer Done(SSCTDO) bit controls the 'SCSI transfer done status' bit located in 34Bh. When set, the above status bit is set.

4.15 CLEAR SCSI INTERRUPT 1

This register can be written by the host processor via the host data bus and its address is 34Ch or 14Ch. This register cleares the interrupts associated with the status bits in SCSI STATUS 1 register except 'clear ATN out signal'. 'Other description for this register is same as above register clear SCSI Interrupt 0'. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	HWSTOC	CLRATN	RSTINC	RSVD	BEREEC	PARERC	PHSCHC	REQINC
DEFAULT	1	1	1	0	1	1	1	1

Clear ATN Out Signal(CLRATN) bit controls ATN signal on the SCSI bus. When this bit is set, ATN signal on the SCSI bus is cleared. When cleared, has no effect on the status of ATN signal.

4.16 SCSI STATUS REGISTER 2

This register can be read by the host processor via the host data bus and its address is 34Dh or 14Dh. This register reflects the state of the SCSI FIFO. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	RSVD	RSVD	OFFNZR	SFFEMP	SFFULL	SFFCNT		

SCSI Offset Non-Zero(OFFNZR) bit represent zero condition of offset counter value. If set, it indicates that the REQ/ACK offset for a synchronous SCSI transfer is non-zero. When cleared, it indicates that the REQ/ACK offset is zero.

SCSI FIFO Empty(SFFEMP) bit represent the emptyness of SCSI FIFO.

SCSI FIFO Full(SFFULL) bit represent the fullness of SCSI FIFO.

SCSI FIFO Count(SFFCNT) field contains the count of the number of bytes in the SCSI FIFO. If its value is 0h. it indicates SCSI FIFO is either full or empty depends on above two bits.

4.17 SCSI STATUS REGISTER 3

This register can be read by the host processor via the host data bus and its address is 34Eh or 14Eh. This register contains information on the state of the current synchronous SCSI transfer. *NOTE THAT Do Not Read This Register Unless All Transfers Are Stopped.* Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	DIFCNT				OFFCNT			

Count Difference(DIFCNT) field contains the difference in the value of SCSI FIFO counter and offset counter. In the case of Data Out Phase, difference counter of initiator remains 0 until transfer has completed and difference counter of target contains the same value of offset counter.

Offset Count(OFFCNT) field contains the current value of the offset counter. This is the count of the number of REQs received for which no ACKs have been issued.

4.18 SCSI STATUS REGISTER 4

This register can be read by the host processor via the host data bus and its address is 34Fh or 14Fh. This register contains information on error conditions for the current SCSI transfer. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	RSVD	RSVD	RSVD	RSVD	RSVD	SYNERS	FFWERS	FFRERS
DEFAULT	0	0	0	0	0	0	0	0

Synchronous Transfer Error(SYNERS) bit represent the occurrence of synchronous error while synchronous transfer is going. Synchronous transfer error occurred when one of the following two conditions is detected. (1) At the beginning of an inbound synchronous transfer, when the SCSI FIFO is not empty prior to the transfer of the first byte of the SCSI bus. This condition may cause the SCSI FIFO to overflow, as 'Count Difference' located in 34Eh is not correct. 2) At the beginning of a synchronous transfer, 'SCSI offset non-zero' status bit located in 34Dh is set. This condition indicates that the previous transfer did not completed successfull.

SCSI FIFO Write Error(FEWERS) bit represent occurrence of some error condition on writing data to the SCSI FIFO. This bit is set when more than one source is enabled to write to the SCSI FIFO. This error can arise under the following condition that the transfer path is set up to send data from the host FIFO, through the SCSI FIFO, onto the SCSI bus, with the GM82C700 reselected as an Initiator and the target driving I/O such that data is enabled SCSI bus-to-SCSI FIFO (for DATA In Phase).

SCSI FIFO Read Error(FFRERS) bit represent occurrence of some error condition on reading data from the SCSI FIFO. This bit is set when more than one source is enabled to read from the SCSI FIFO.

4.19 SCSI COUNTER TEST CONTROL

This register can be written by the host processor via the host data bus and its address is 34Fh or 14Fh. This register is used to initiate test modes in internal GM82C700 SCSI logic. *NOTE THAT Do Not Write To This Register During Normal Operation.* Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	RSVD	RSVD	RSVD	RSVD	TXCNTU	TXCNTD	RSVD	TXCNTT
DEFAULT	0	0	0	0	0	0	0	0

Transfer Count Up(TXCNTU) bit controls test condition of SCSI transfer counter. When set, the SCSI transfer counter counts up at the input clock rate.

Transfer Count Down(TXCNTD) bit controls test condition of SCSI transfer counter. When set, the SCSI transfer counter counts down at the input clock rate.

Transfer Count Test(TXCNTT) bit enables counter test. When set, a stage-to-stage carry true is forced in both the transfer and select abort counters, which cause both counters to run at the clock rate. During the transfer count test, the counter contents can be monitored by reading the desired stage. If this bit and 'hardware timeout counter enable' bit located in 342h are both high, then the SCSI Transfer Count read register (bit 5-0, 348h) is reassigned to the Select Abort Counter in the following manner:

Bit	Assignment
5	Stage 6 (/2, output)
4	Stage 5 (/2, output)
3	Stage 4 (/2, output)
2	Stage 3 (/10, carry out)
1	Stage 2 (/256, carry out)
0	Stage 1 (/256, carry out)

4.20 CLEAR SCSI ERRORS

This register can be written by the host processor via the host data bus and its address is 34Fh or 14Fh. This register clears the error condition status bits in the SCSI STATUS 4 register(34Fh). Setting any of these bits clear the corresponding status bit. A clear bit does not need to be cleared before it can be set again. Writing a zero to any bit in this register has no effect. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	RSVD	RSVD	RSVD	RSVD	RSVD	SYNERC	FFWERC	FFRERC

Clear Synchronous Transfer Error(SYNERC) bit cleares 'synchronous transfer error' status bit located in 34Fh if set.

Clear SCSI FIFO Write Error (FFWERC) bit cleares 'SCSI FIFO write error' status bit located in 34Fh if set.

Clear SCSI FIFO Read Error(FFRERC) bit cleares 'SCSI FIFO read error' status bit located in 34Fh if set.

4.21 SCSI INTERRUPT MODE 0

This register can be written and read by the host processor via the host data bus and its address is 350h or 150h. This register enables the interrupts associated with the status bits in SCSI STATUS 0 register. Setting any of these bits enables the corresponding interrupt. If an event occurs that cause a status bit to be set, and the enable bit for that condition is set, IRQ is asserted. Clearing an enable bit causes the interrupts associated with the condition to be masked. However the status bit associated with the condition is still set, regardless of the state of the enable bits. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	RSVD	SELODE	SELIDE	SELOBE	SWRAPE	SCTDOE	P__RDYE	DMADOE
DEFAULT	0	0	0	0	0	0	0	0

4.22 SCSI INTERRPUT MODE 1

This register can be written and read by the host processor via the host data bus and its address is 351h or 151h. This register enables the interrupts associated with the status bits in SCSI STATUS 1 register. Setting any of these bits enables the corresponding interrupt. If an event occurs that cause a status bit to be set, and the enable bit for that condition is set, IRQ is asserted. Clearing an enable bit causes the interrupts associated with the condition to be masked. However the status bit associated with the condition is still set, regardless of the states of the enable bits. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	HOSTOE	ATNINE	RSTINE	PHSERE	BFREEE	PARERE	PHSCHE	REQINE
DEFAULT	0	0	0	0	0	0	0	0

4.23 HOST TRANSFER CONTROL 0

This register can be written and read by the host processor via the host data bus and its address is 352h or 152h. This register contains the basic control for PIO and DMA transfer modes. The bits which enable a mode may be set at the same time as the bits configuring the mode. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	HOTXEN	DWIDTH	HOMODE	EMDBWD	WRMODE	INTREN	FFCRST	SWINTR
DEFAULT	0	0	0	0	0	0	0	0

Host Transfer Enable(HOTXEN) bit controls transfer between host main memory and the host FIFO. When set, data transfer between host main memory and the host FIFO in either PIO or DMA mode is enabled. Clearing this bit also clears 'host data transfer done' status bit in 354h.

Data Width(DWIDTH) bit determines the data width of host side. When this bit is set, transfers between host main memory and the host FIFO are 8 bits wide and utilize SD0-SD7. When this bit is cleared, transfers between host main memory and the host FIFO are 16 bits wide and utilize SD0-SD15. Transfers utilizing host DMA mode are 8 bits wide.

Host Transfer Mode(HOMODE) bit determines the host transfer mode. When this bit is set, transfers between host main memory and the host FIFO are in DMA mode. When this bit is cleared, transfers between host main memory and the host FIFO are in PIO mode. *NOTE: When changing from PIO to DMA with HOTXEN = 1, any direction change must be done first (bit 3 below).*

Double World Transfer Emulation(EMDBWD) bit determines the use of emulated 32-bit transfer supported above 386DX processors. When this bit is set, 32Bit data transfer emulation is enabled. When this bit enabled, data port is mapped both addresss 356h and 358h. When this option is used, DWIDTH should always be set. When this bit is cleared, the normal 16Bit data port is used.

Transfer Direction(WRMODE) bit determines the direction of data transfer. When this bit is set, data is transfered from host main memory to the host FIFO in either PIO or DMA mode. When this bit is cleared, data is transfered from the host FIFO to the host main memory in either PIO or DMA mode.

Master Interrupt Enable(INTREN) bit enable interrupt generation of the GM82C700 SCSI controller. If this bit is set, interrupt function operate normally. If cleared, all interrupts are masked.

Reset FIFO Counter(FFCRST) bit controls initialization of FIFO counter. When this bit is set, the FIFO counter is cleared. This bit is a self-clearing bit.

Software Interrupt(SWINTR) bit represent user defined interrupt source. If above 'master interrupt enable' bit is set, setting this bit asserts IRQ. This bit is provides for software-generated interrupts.

4.24 HOST TRANSFER CONTROL 1

This rgister can be written and read by the host processor via the host data bus and its address is 353h or 153h. This register used to set the power-save feature and write the stack offset pointer. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	PWRDWN	EXTSTK	RSVD	STKPTR				
DEFAULT	0	0	0	0	0	0	0	0

Power Save Mode(PWRDWN) bit controls clock distribution. When this bit is set, the internal clock is stopped to conserve power. Once the clock is stopped, the GM82C700 is not operational.

Enable Extended Stack(EXTSTK) bit controls the depth of stack. When this bit is set, it allows access to the upper 16-byte of the 32-byte stack area. When cleared, only the lower 16-byte of the stack may be accessed.

Stack Pointer(STKPTR) field represents initial stack address and is write-only.

4.25 HOST STATUS

This register can be read by the host processor via the host data bus and its address is 354h or 154h. This register reflects the real-time status of the current DMA or PIO transfer. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	HODONE	WREADY	INTRST	DFFULL	DFFEMP	DFF_HF	RSVD	RSVD

Host Data Transfer Done(HODONE) bit is used in DMA mode only. This bit is set when the host DMA controller has transfered the last byte or word and assert T/C. While this bit is set, the internal host DMA logic is disabled; the host DMA logic remains disabled until this bit is cleared. This bit is cleared when 'host transfer enable' bit located in 352h is cleared. This condition does not generate an interrupt.

Word Ready(WREADY) bit indicates that two bytes of data can be accessed. This bit is used in PIO mode only. When set, a 16-bit word is ready for transfer to or from the host FIFO. If the transfer count for a particular transfer does not equal or end on a 128-byte boundary, the host must transfer data into or out of the host FIFO one word at a time; this bit is used to control that process.

Interrupt Status(INTRST) bit indicates interrupt status of GM82C700. This bit is OR of all enabled interrupts. This bit may be read at any time, whether or not interrupts have been enabled via 'master interrupt enable' bit. This provides means to poll for interrupts.

Host FIFO Full(DFFULL) bit indicates full state of host data FIFO. This bit is set when the host FIFO is full. This bit is used during SCSI-to-host PIO transfers.

Host FIFO Empty(DFFEMP) bit indicates empty state of host data FIFO. This bit is set when the host FIFO is empty. This bit is used during SCSI-to-host PIO transfers.

Host FIFO Half Full(DFF_HF) bit indicates half full state of host data FIFO. This bit indicates that the host FIFO is at least half full.

4.26 HOST FIFO STATUS

This register can be read by the host processor via the host data bus and its address is 355h or 155h. This register provides a count of the current number of bytes in the host FIFO. *NOTE: The host FIFO is 128 bytes deep. Under some circumstances, the host FIFO may hold up to 4 additional bytes (132 bytes). FCNT contains the correct count in these circumstances.* Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	HFFCNT							

4.27 HOST DATA PORT

This register can be written and read by the host processor via the host data bus and its address is 356h or 156h'. Data transfers between the GM82C700 and the host take place via this register in both DMA and PIO mode. DMA transfers are 8-bit only. Host PIO transfers are 8 or 16-bit, as defined by the state of SBHE. If SBHE is not active, 8 bits will be transfered via the low order data byte; if SBHE is active, 16 bits will be transfered. Following figure shows the function table for this register.

BIT	15	14	13	12	11	10	9	8
NAME	HDD_DH							
DEFAULT	0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	0
HDD_DL							
0	0	0	0	0	0	0	0

4.28 BURST CONTROL

This register can be written and read by the host processor via the host data bus and its address is 358h or 158h. This register controls the burst on and burst off times for DMA transfers. The GM82C700 will run as many Burst On/Burst Off cycles as necessary to transfer all data. To disable the BON and BOFF timers, load both BON and BOFF with 0h. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	BONVAL				BOFVAL			
DEFAULT	1	1	1	1	0	0	0	1

Burst On Time Value(BONVAL) field contains the maximum value, in microseconds, of the transmission (burst) period. The GM82C700 bursts data for the duration of BONVAL, or until all data has been sent, whichever less. BON may range from 0(none) to 15 microseconds.

Burst Off Time Value(BOFVAL) field contains the minimum value, in microseconds, of the off-line(down) period. The GM82C700 will not request DMA service for at least the duration of BOFVAL. BOFVAL may range from 0(none) to 15 microseconds.

4.29 EXTERNAL PORT A

This register can be written and read by the host processor via the host data bus and its address is 35Ah or 15Ah. This register provides an external 8 or 16-bit port which may be accessed at any time. Port A is user defined. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	EXTPOA							
DEFAULT	User Defined Initial Value of external port A							

4.30 EXTERNAL PORT B

This register can be written and read by the host processor via the host data bus and its address is 35Bh or 15Bh . This register provides an external 8 or 16-bit port which may be accessed at any time. Port B is user defined. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	EXTPOB							
DEFAULT	User Defined Initial Value of external port B							

4.31 VERSION REGISTER

This register can be read by the host processor via the host data bus and its address is 35Ch or 15Ch. This register gives the version number of the chip. Version number for the GM82C700 is 00h. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	VERNUM							

4.32 STACK DATA

This register can be written and read by the host processor via the host data bus and its address is 35Dh or 15Dh. This port is an 8-bit wide by 32-byte stack for general purpose memory use. The stack port may be addressed by writing to the lower 5 bits of HOST TRANSFER CONTROL 1 register. The offset points to the first location in the stack to be read from or written to. This allows the software directly access any byte in the stack. Successive reads or writes access the next higher location inthe stack. When the EXTSTK bit in HOST TRANSFER CONTROL 1 register is set, 32-bytes (lower 16-byte and upper 16-byte) of the stack area are available. When this bit is not set, only lower 16-bytes of the stack area are available. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	STACKD							
DEFAULT	0	0	0	0	0	0	0	0

4.33 IDENTIFICATION REGISTER

This register can be read by the host processor via the host data bus and its address is 35Fh or 15Fh. This register is used for identification purpose. Successive reads of this register return a 32-byte ASCII string of '(C)1993 GoldStar GM82C700 '. In ASCII this produces the following hexadecimal string: 28, 43, 29, 31, 39, 39, 33, 20, 47 6F, 6C, 64, 53, 74, 61, 72, 47 4D, 38, 32, 43, 37, 30, 30, 20, 20, 20, 20, 20, 20, 20, 20. Following figure shows the function table for this register.

BIT	7	6	5	4	3	2	1	0
NAME	ID_VAL							

CHAPTER 5. APPLICATION NOTES

This chapter provides basic information on using the GM82C700. It includes instructions for running data transfers and concludes with a simple application drawing.

This section consists as following:

- Selection/Reselection sequence.
- SCSI PIO mode transfer (Initiator/Target)
- SCSI Automatic transfer (Initiator/Target)
  (Host-PIO/DMA)
- Diagnostics
- Odd byte disconnection
- Initiator message handling

5.1 SELECTION/RESELECTION SEQUENCE

The GM82C700 can perform Selection In, Selection Out, Reselection Out or Reselection In sequences automatically. The following sections describe the tasks you must perform to run automatic Selection In, Selection Out, Reselection Out or Reselection In sequence.

1) SELECTION IN SEQUENCE

1. Adjust the ID value of SCSI devices (345h).
2. Enable selection in sequence (Set bit 5 of 340h).

NOTE: You may also set ATNINE in the SCSI STATUS O register (bit 6 of 351h) to generate an interrupt if the initiator assert ATN.

3. Wait for Selection In Done and TMODES bit to be set (bits 7 & 5 of 34Bh).
4. Check the SELECTION/RESELECTION ID register (345h) for the SCSI ID of the initiator.
5. Adjust synchronous data transfer rate and offset value (344h).
6. When Selection In Done and TMODES bit is set (bits 7 & 5 of 34Bh), you have been selected and may continue with an information transfer phase.

2) RESELECTION IN SEQUENCE

1. Adjust the ID value of SCSI devices (345h).
2. Enable selection out sequence (Set bit 6 of 340h).

NOTE: You may also set ATNIEN in the SCSI SEQUENCE CONTROL register (bit 2 of 340h) to assert ATN on reselection.

3. Wait for Selection In Done bit to be set (bit 5 of 34Bh).
4. Load the expected phase (bits 7-5 of 343h).
5. Adjust synchronous data transfer rate and offset value (344h).
6. When Selection In Done bit is set (bit 5 of 34Bh), you have been reselected and may continue with an information transfer phase.

3) SELECTION OUT SEQUENCE

1. Adjust the ID value of SCSI devices (345h).
2. Adjust synchronous data transfer rate and offset value (344h).
3. Set the expected phase (bits 7-5 of 343h). All other controls must be cleared.
4. Adjust the SCSI TRANSFER CONTROL 1 register (342h).
5. Clear Channel (Set bit 1 of 341h); this clears the transfer counter and channel. CHANEN (bit 5 of 341h) should always be set.
6. Reset CHANRS (bit 1 of 341h).

NOTE: If the transfer mode is SCSIPIO, it is not necessary to clear channel. However, you should do it anyway, as the target might respond with an unexpected phase, such as Data In when you are expecting Message Out.

7. Enable selection out sequence (Set bit 6 of 340h).

NOTE: If you are using either the Automatic Attention Out or the Automatic attention Parity options, you should set enable bits for them (bits 3 & 1 of 340h). If you are using the Automatic Attention Out option, the expected phase set in the SCSI SIGNAL OUT register (343h) in Step 2 should be Message Out; the target determines whether this phase is supported.

8. Enable interrupt generation (Set bit 2 of 350h).
9. Enable interrupt for Selection Out Done, Selection Initiated Out (Set bits 6 & 4 of 350h).
10. Enable interrupt for Hardware Selection Time Out Abort (Set bit 7 of 351h).
11. Disable selection out sequence (Reset bit 6 of 340h).
12. Wait for IRQ assertion or wait for one of following bits to be set:
    - Selection Out Done : Bit 6, 34Bh
    - Selection Initiated Out : Bit 4, 34Bh
    - Selection Time Out Abort : Bit 7, 351h
13. When Selection Out Done bit is set (bit 6 of 34Bh), the target has been selected and you may initiate an information transfer phase.
14. In order to detect a passing Bus Free condition during selection, follow this sequence:
    a) Clear the Bus Free Interrupt (Set bit 3 of 34Ch).
    b) Clear SELOEN in the SCSI SEQUENCE CONTROL register.
    c) Disable the Selection Time Out Interrupt (Reset bit 7 of 351h).
    d) Disable the Selection Out Done Interrupt (Reset Bit 6 of 350h).
    e) Look at the status of Selection Out Done (bit 6 of 34Bh). If it is still active, a Bus Free condition has not occurred since selection.

4) RESELECTION OUT SEQUENCE

1. Adjust the ID value of SCSI devices (345h).
2. Adjust synchronous data transfer rate and offset value (344h).
3. Set the phase after reselection (bits 7-5 of 343h). All other controls must be cleared.
4. Wait for IRQ assertion or wait for one of following bits to be set:
    - Selection Out Done : Bit 6, 34Bh
    - Selection Initiated Out : Bit 4, 34Bh
    - Selection Time Out Abort : Bit 7, 351h

NOTE: TMODE (bit 7 of 34Bh) should be set or you have initiated a Selection sequence.

5. Adjust the SCSI TRANSFER CONTROL 1 register (342h).
6. Adjust the SCSI TRANSFER COUNTER with appropriate value.
7. Clear Channel (Set bit 1 of 341h); this clears the transfer counter and channel. CHANEN (bit 5 of 341h) should always be set.
8. Reset CHARNS (bit 1 of 341h).

NOTE: If the transfer mode is SCSIPIO, it is not necessary to clear channel. However, you should do it anyway, as the target might respond with an unexpected phase, such as Data In when you are expecting Message Out.

9. When Selection Out Done bit is set (bit 6 of 34Bh), the target has been selected and you may initiate an information transfer phase.

5.2 SCSI PIO TRANSFERS

Use the SCSI PIO data transfer modes whenever you need host processor intervention during the transfer, such as during message exchanges. SCSI PIO is asynchronous only, so you should not use it for data-in or data-out phases. There are two types of SCSI PIO: Manual and Automatic.

Manual: The host processor writes directly to the SCSI data bus via the latch at 346h and reads or drives the SCSI bus control lines via the register at 343h. In Manual mode, the GM82C700 is essentially a bus buffer having no control functions.

Automatic: The host processor writes directly to the SCSI data bus via the latch at 346h, while the GM82C700 performs automatic SCSI bus control. Automatic SCSI PIO transfers can be monitored by interrupt or polling status. Interrupt configuration for the GM82C700 is controlled by the interrupt mode registers at 350h and 351h. Polling mode is driven off the P_RDYS status bit.

The following sections describe the tasks you must perform to accomplish automatic SCSI PIO transfers as either an initiator or target.

1) HOST TO SCSI DATA TRANSFER AS AN INITIATOR

1. Enable SCSI PIO Transfer (Set bit 3 of 341h). CHANEN (bit 5 of 341h) should always be set.
2. Adjust transfer mode to 16-bit PIO Write mode and reset FIFO (352h).
3. Wait for P_RDYS status to be set (bit 1 of 34Bh).
4. Write data to the SCSI PIO MODE LATCHED DATA register (346h).
5. If you have more data to transfer, repeat step 3-5. Otherwise, go to step 6.
6. Disable SCSI PIO Transfer (Reset bit 3 of 341h).

2) SCSI TO HOST DATA TRANSFER AS AN INITIATOR

1. Enable SCSI PIO Transfer (Set bit 3 of 341h). CHANEN (bit 5 of 341h) should always be set.
2. Wait for P_RDYS status to be set (bit 1 of 34Bh).
3. Read data from the SCSI PIO MODE LATCHED DATA register (346h).
4. Test PHSERS bit (bit 4 of 34Ch). If PHSERS is cleared, repeat Step 2-4. If PHSERS is set, go to Step 5.
5. Disable SCSI PIO Transfer (Reset bit 3 of 341h).

3) HOST TO SCSI DATA TRANSFER AS AN TARGET

1. Set proper phase (bits 7-5 of 343h).
2. Enable SCSI PIO Transfer (Set bit 3 of 341h). CHANEN (bit 5 of 341h) should always be set.
3. Wait for P_RDYS status to be set (bit 1 of 34Bh).
4. Write data to the SCSI PIO MODE LATCHED DATA register (346h). By this action, Target asserts REQ signal.
5. If you have more data to transfer, repeat step 3-5. Otherwise, go to step 6.
6. Disable SCSI PIO Transfer.

4) SCSI TO HOST DATA TRANSFER AS AN TARGET

1. Set proper phase (bits 7-5 of 343h).
2. Enable SCSI PIO Transfer (Set bit 3 of 341h). CHANEN (bit 5 of 341h) should always be set.
3. Wait for P_RDYS status to be set (bit 1 of 34Bh).
4. Read data from the SCSI PIO MODE LATCHED DATA register (346h). By this action, the target deasserts REQ when the initiator deasserts ACK, and automatically asserts another REQ signal.
5. If you have more data to transfer, repeat Steps 3-5. If not, go to Step 6.
6. Disable SCSI PIO Transfer (Reset bit 3 of 341h).

5.3 AUTOMATIC DATA TRANSFER MODE

Use the Automatic data transfer mode for automatic SCSI data transfers. SCSI Automatic mode uses two types of host transfer modes: host PIO and host DMA.

Host PIO: The host processor writes to or reads from the 128-byte host FIFO via the data register at 356h. Host PIO transfers are driven off the status bits in the status register at 352h.

Host DMA: The host processor sets up the data transfer operation by loading its DMA controller with a memory pointer and the transfer count. The host DMA controller writes/reads transfer data to/from the 128-byte host FIFO via the data register at 356h. Once begun, host DMA transfers run to completion without futher host processor intervention.

The following sections describe how to accomplish normal mode SCSI transfers as an initiator.

1) HOST TO SCSI DATA TRANSFER: INITIATOR, PIO

1. Wait for the phase change (bit 1 of 34Ch, R).
2. Load the expected phase (bits 7-5 of 343h).
3. Turn off the data path, then turn it on again.
4. Clear the transfer count and the SCSI and host FIFOs.
5. Enable SCSI transfer and FIFO transfer (Set bits 7 & 6 of 341h); this enables the GM82C700 SCSI logic. CHANEN (bit 5 OF 341h) should always be set.
6. Enable Host transfer and adjust transfer mode to 16-bit PIO Write mode (Set bits 7 & 3, reset bits 6 & 5 of 352h).
7. Wait for HFFEMP or INTRST to be set (bits 3-5 of 354h).
8. Wait for INTRST to clear.
9. If HFFEMP is set and INTRST is cleared (bits 3-5 354h), use REP OUTSW to write 128 bytes (64 words).
10. Adjust host processor transfer count.
11. Test for the end of the transfer in the host processor by checking HODONE (bit 7 of 354h); if not set, repeat step 7-11.
12. If HODONE is set, disable Host transfer (Reset bit 7 of 352h).

2) SCSI TO HOST DATA TRANSFER: INITIATOR, PIO

1. Wait for the phase change (bit 1 of 34Ch, R).
2. Load the expected phase (bits 7-5 of 343h).
3. Test for phase mismatch and match the phase.
4. Clear the transfer counter and the SCSI and host FIFOs.
5. Enable SCSI transfer and FIFO transfer (Set bits 7 & 6 of 341h); this enables the GM82C700 SCSI logic. CHANEN (bit 5 of 341h) should always be set.
6. Enable Host transfer and adjust transfer mode to 16-bit PIO Read mode (Set bit 7, reset bits 6.5 & 3 of 352h).
7. Wait for HFFFUL or INTRST to be set (bits 4 and 5 of 354h).
8. Wait for INTRST to be cleared. You may also need to wait for Word Ready (bit 6 of 354h).
9. If HFFFUL is set and INTRST is cleared (bits 4 and 5 of 354h), use REP INS to read 128 bytes (64 words).
10. Adjust host processor transfer count.
11. Test for the end of the transfer in the host processor; repeat Steps 7-10 until all data has been read.
12. When all data has been read, disable Host transfer (Reset bit 7 of 352h).

3) HOST TO SCSI DATA TRANSFER: INITIATOR, DMA

1. Load the expected phase (bits 7-5 of 343h).
2. Clear the transfer counter and the SCSI and host FIFOs.
3. Set up the host DMA controller for address, byte count, and transfer mode.
4. Wait for REQINC to be set and PHSERS to be cleared (bits 0 & 4 of 34Ch).
5. Enable SCSI transfer and FIFO transfer (Set bits 7 & 6 of 341h); this enables the GM82C700 SCSI logic. CHANEN (bit 5 of 341h) should always be set.
6. Enable Host transfer and adjust transfer mode to 8-bit DMA Write mode (Set bits 7, 6, 5 & 3 of 352h).
7. Wait for the DMADOS, PHSERS, or other interrupts. Interrupts must be enabled in order to assert IRQ.

4) SCSI TO HOST DATA TRANSFER: INITIATOR, DMA

1. Load the expected phase (bits 7-5 of 343h).
2. Clear the transfer count and the SCSI and host FIFOs.
3. Set up the host DMA controller for address, byte count, and transfer mode.
4. Wait for REQINS to be set and PHSERS to be cleared (bits 0 & 4 of 34Ch).
5. Enable SCSI transfer and FIFO transfer (Set bits 7 & 6 of 341h); this enables the GM82C700 SCSI logic. CHANEN (bit 5 of 341h) should always be set.
6. Enable Host transfer and adjust transfer mode to 8-bit DMA Read mode (Set bits 7, 6 & 5, reset bit 3 of 352h).
7. Wait for the DMADOS, PHSERS, or other interrupts. Interrupts must be enabled in order to assert IRQ.

5) HOST TO SCSI DATA TRANSFER: TARGET, PIO

1. Set the SCSI phase with proper value (bits 7-5 of 343h).
2. Adjust the SCSI TRANSFER COUNTER with appropriate value.
3. Adjust the SCSI TRANSFER CONTROL registers (341h & 342h).
4. Clear the transfer count and the SCSI and host FIFOs.
5. Enable SCSI transfer and FIFO transfer (Set bits 7 & 6 of 341h); this enables the GM82C700 SCSI logic. CHANEN (bit 5 of 341h) should always be set.
6. Enable Host transfer and adjust transfer mode to 16-bit PIO Write mode (Set bits 7 & 3, reset bits 6 & 5 of 352h).
7. Wait for HFFEMP or INTRST to be set (bits 3 and 5 of 354h).
8. Wait for INTRST to clear.
9. If HFFEMP is set and INTRST is cleared (bits 3 and 5 of 354h), use REP OUTSW to write 128 bytes (64 words).
10. Adjust host processor transfer count.
11. Test for the end of the transfer in the host processor by checking HODONE (bit 7 of 354h); if not set, repeat step 7-11.
12. If HODONE is set, disable Host transfer (Reset bit 7 of 352h).
13. After all procedure has completed, deassert all SCSI signal (Reset 343h) to force Bus Free state.

6) SCSI TO HOST DATA TRANSFER: TARGET, PIO

1. Set the SCSI phase with proper value (bits 7-5 of 343h).
2. Adjust the SCSI TRANSFER COUNTER with appropriate value.
3. Adjust the SCSI TRANSFER CONTROL registers (341h & 342h).
4. Clear the transfer count and the SCSI and host FIFOs.
5. Enable SCSI transfer and FIFO transfer (Set bits 7 & 6 of 341h); this enables the GM82C700 SCSI logic. CHANEN (bit 5 of 341h) should always be set.
6. Enable Host transfer and adjust transfer mode to 16-bit PIO Write mode (Set bits 7, reset bits 6.5&3 of 352h).
7. Wait for HFFFUL or INTRST to be set (bits 4 and 5 of 354h).
8. Wait for INTRST to be cleared. You may also need to wait for Word Ready (bit 6 of 354h).
9. If HFFFUL is set and INTRST is cleared (bits 4 and 5 of 354h), use REP INS to read 128 bytes (64 words).
10. Adjust host processor transfer count.
11. Test for the end of the transfer in the host processor; repeat Steps 7-10 until all data has been read.
12. When all data has been read, disable Host transfer (Reset bit 7 of 352h).
13. After all procedure has completed, deassert all SCSI signal (Reset 343h) to force Bus Free state.

7) HOST TO SCSI DATA TRANSFER: TARGET, DMA

1. Set the SCSI phase with proper value (bits 7-5 of 343h).
2. Adjust the SCSI TRANSFER COUNTER with appropriate value.
3. Adjust the SCSI TRANSFER CONTROL registers (341h & 342h).
4. Clear the transfer count and the SCSI and host FIFOs.
5. Set up the host DMA controller for address, byte count, and transfer mode.
6. Wait for REQINS to be set (bits 0 of 34Ch).
7. Enable SCSI transfer and FIFO transfer (Set bits 7 & 6 of 341h); this enables the GM82C700 SCSI logic. CHANEN(bit 5 of 341h) should always be set.
8. Enable Host transfer and adjust transfer mode to 8-bit DMA Write mode (Set bits 7, 6, 5 & 3 of 352h).
9. Wait for the DMA Done or any other interrupt (IQR assertion). Interrupt must be enabled in order to assert IRQ.
10. After all procedure has completed, deassert all SCSI signal (Reset 343h) to force Bus Free state.

8) SCSI TO HOST DATA TRANSFER: TARGET, DMA

1. Set the SCSI phase with proper value (bits 7-5 of 343h).
2. Adjust the SCSI TRANSFER COUNTER with appropriate value.
3. Adjust the SCSI TRANSFER CONTROL registers (341h & 342h).
4. Clear the transfer count and the SCSI and host FIFOs.
5. Set up the host DMA controller for address, byte count, and transfer mode.
6. Wait for REQINS to be set (bits 0 to 34Ch).
7. Enable SCSI transfer and FIFO transfer (Set bits 7 & 6 of 341h); this enables the GM82C700 SCSI logic. CHANEN (bit 5 of 341h) should always be set.
8. Enable Host transfer and adjust transfer mode to 8-bit DMA Read mode (Set bits 7, 6 & 5, reset bit 3 of 352h).
9. Wait for the DMA Done or any other interrupt (IRQ assertion). Interrupt must be enabled in order to assert IRQ.
10. After all procedure has completed, deassert all SCSI signal (Reset 343h) to force Bus Free state.

5.4 DIAGNOSTICS

The 128-byte host FIFO and associated logic can be tested using the wrap around feature. Using host DMA or PIO mode, transfers are accomplished in the normal manner. To check the FIFO, make sure that HOTXEN and SCTXEN (bits 6 & 7 of 341h) are cleared. Set write mode (Set bit 3 of 352h) and begin the transfer. To read the data back, set read mode (Reset bit 3 of 352h).

5.5 ODD BYTE DISCONNECTION

It is possible for a SCSI device to disconnect after an odd number of bytes has been transferred across the SCSI bus while in 16-bit DMA mode. In that case, the chip has a mechanism to change modes of operation from DMA to PIO and back again without loss of data. The general procedure is as follows:

1) READ OPERATION

1. Check to determine that only one byte of data is left.
2. Switch to PIO mode, leaving HOTXEN set (bit 7 of 352h).
3. Read byte from port 356h and save.
4. To continue the transfer, set mode to PIO Write.
5. Write byte to port 356h.
6. Change direction to read (Reset bit 3 of 352h).
7. Change mode to DMA transfer (Set bit 6 of 352h).
8. Enable SCSI transfers (Set bit 7 of 341h).

2) WRITE OPERATION

1. Check to determine that an odd number of bytes has been transferred across the SCSI bus.
2. Save the DMA address pointer and word counter minus 2.
3. To continue the transfer, set the ALIGNB bit (bit 1 of 342h).
4. Enable DMA transfer; the first byte will be thrown away. Initiator Message Handling.

5.6 INITIATOR MESSAGE HANDLING

Messages are intended to be handled by SCSI PIO transfer. Certain special cases to consider are messages after selection, multiple messages, or parity errors. If messages after selection are to be handled by the initiator, ATN is asserted on the bus. The target responds with the Message Out phase at this time. The first message is the ID message, and after this, the initiator has the option of sending a multiple-byte message such as a synchronous data transfer request. ATN remains asserted during Message Out transfers, until cleared by setting CLRATN (bit 6 of 34Ch). In order to maintain SCSI protocol, ATN should be cleared before the last ACK of a message sequence or, in the case of automatic SCSI PIO, the last write to SCSIDAT. In the case of an error condition, ATN should be cleared after the first REQ of the Message Out phase and before the last ACK of the message sequence. If a parity error occurs on Message In, ATN is asserted before ACK, and the message should be retransmitted.

CHAPTER 6. ELECTRICAL INFORMATION

OPERATING CONDITIONS
0 °C < TEMP < 70°C
4.5V < VDD < 5.5V
Load Capacitance = 50 pF, unless otherwise noted.

6.1 ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	MIN	MAX	UNIT
POWER SUPPLY VOLTAGE	0.0	7	V
INPUT VOLTAGE	−0.5	VDD + 0.5	V
OUTPUT VOLTAGE	−0.5	VDD + 0.5	V
STORAGE TEMP.	−40	+125	°C
POWER DISSIPATION		1	W

6.2 CRYSTAL OSCILLATOR SPECIFICATION

PARAMETER (Note 2)	VALUE
Design Type	Price
Minimum Resistor Shunting XIN and XOUT	21,000
Maximum Capacitance between XIN and XOUT	12 pF (Note 1)
Maximum Motional Resistance of Crystal:	50 ohm
Oscillation Mode:	Fundamental
Minimum Crystal Q:	20,000
Oscillation Frequency:	20 MHz

Notes: 1) Including Co of crystal and board layout.
2) The required capacitors are contained on the chip
Do NOT ground any crystal terminals.

6.3 DC ELECTRICAL INFORMATION

SYMBOL	CHARACTERISTICS		MIN	MAX	UNIT	CONDITIONS	
I_{IL}	Input Leakage Current		-10	145	μA	Pull Down	CLKSEL
			-145	10	μA	Pull Up	DRQ, PORTEN
			-2	2	μA	CMOS	X1, F1
			-2	2	μA	Schmitt Trigger	MRST, SCD[7:0], SCDP, C/D, I/O, MSG, ATN, SEL, BSY, REQ, ACK, RST
			-2	2	μA	TTL	SA[9:0], SBHE, IOR, IOW, AEN, DACK, T/C, SD[15:0]
V_{IL}	Input Low Voltage			0.3VDD	V	CMOS	X1, F1
				0.8	V	Schmitt Trigger	MRST, SCD[7:0], SCDP, C/D, I/O, MSG, ATN, SEL, BSY, REQ, ACK, RST
				0.8	V	TTL	All Pins except CMOS and Schmitt Trigger Input
V_{IH}	Input High Voltage		0.7VDD		V	CMOS	X1, F1
			2.0		V	Schmitt Trigger	MRST, SCD[7:0], SCDP, C/D, I/O, MSG, ATN, SEL, BSY, REQ, ACK, RST
			2.0		V	TTL	All Pins except CMOS and Schmitt Trigger Input
Vh	Input Hysteresis		200		mV	Schmitt	All Schmitt Trigger Input
V_{OH} and V_{OL}	Open-Drain	V_{OL}		0.4	V	I_{OL}=24mA	IOCS16N
		V_{OL}		0.4	V	I_{OL}=48mA	SCD & [7:0], SCDP, C/D, I/O, MSG, ATN, SEL, BSY, REQ, ACK, RST
	Output Only	V_{OL}		0.4	V	I_{OL}=24mA	IRQ
		V_{OH}	2.4		V	I_{OH}=8mA	
	Bidirectional Outputs	V_{OL}		0.4	V	I_{OL}=4mA	PORTEN (with Pull Up)
		V_{OH}	2.4		V	I_{OH}=4mA	
		V_{OL}		0.4	V	I_{OL}=8mA	F1
		V_{OH}	2.4		V	I_{OH}=8mA	
		V_{OL}		0.4	V	I_{OL}=24mA	SD[15:0] DRQ (with Pull Up)
		V_{OL}	2.4		V	I_{OH}=8mA	
	Clock Output	V_{OL}		0.4	V	I_{OL}=8mA	X2
		V_{OH}	2.4		V	I_{OH}=4mA	

6.4 SYSTEM TIMING

All timing values are given for a 20 MHz clock.
Operating conditions are: Ta = T_A = 0°C to 70°C, V_{DD} = 5V + 5%

(Unit: ns)

Parameter	Description	Min	Max	Remarks
CPU Interface Timing				
t1	Chip clock period	50		
t2	Address setup time to IOR falling	25		
t3	Address hold time after IOR rising	25		
t4	IOCS16 valid after address and SBHE valid		60	
t5	IOCS16 disabled after address and SBHE invalid		30	
t6	Valid data delay time from IOR falling	6	60	
t7	Data hold time after IOR rising	4		
t8	Driver OFF time from IOR rising		25	
t9	Driver ON time from IOR falling		25	
t10	Read Cycle update	2t1		
t11	Read Cycle time	4t1		
t12	IOR pulse width	2t1		
t13	Address setup time to IOW falling	25		
t14	Address hold time after IOW rising	25		
t15	Data setup time to IOW rising	5		
t16	Data hold time after IOW rising	15		
t17	Write Cycle update	2t1		
t18	Write Cycle time	4t1		
t19	IOW Pulse width	2t1		
t20	Delay time from IOR to valid data		60	
t21	Data hold time after IOR rising	4		
t22	Drive ON tim from IOR falling		25	
t23	Drive OFF time from IOR rising		25	
t24	DMA Read Cycle update	2t1		
t25	DMA Read cycle time	4t1		
t26	DMA IOR Pulse width	2t1		
t27	DRQ OFF time from DMA IOR falling	10	60	
t28	Terminal Count pulse width	50		
t29	Data setup time to DMA IOW falling	5		
t30	Data hold time to DMA IOW rising	15		

(continued)

Parameter	Description	Min	Max	Remarks
t31	DRQ OFF time from DMA IOW falling	50		
t32	DMA Write Cycle update	2t1		
t33	DMA Write Cycle time	4t1		
t34	DMA Write pulse width	2t1		
SCSI Bus Timing				
t35	BSY active from IOW rising		16t1+60	
t36	SEL active from IOW rising		64t1+60	
t37	SELINGO Interrupt from ENSELO		92t1+60	
t38	SELDO interrupt from Target BSY		4t1+60	
t39	Own ID valid from BSY falling		20	
t40	Target ID valid from SEL falling	24t1+60		
t41	Interrupt from phase change		37	
t42	Interrupt from phase change/REQ		40	
t43	Phase change from IOW rising		46	
t44	BUS FREE from SEL/BSY/RST rising		9t1+40	
t45	SPIORDY Interrupt from REQ falling		3t1+35	
t46	SPIORDY cleared from IOR falling		60	
t47	ACK asserted from IOR rising		3t1+35	
t48	ACK deasserted from REQ rising		2t1+62	
t49	SCSI Data setup time to REQ or ACK		5	
t50	SCSI Data hold time after REQ or ACK		15	
t51	SCSI Data Setup time to IOR low		15	
t52	SCSI Data hold time after IOR low		5	

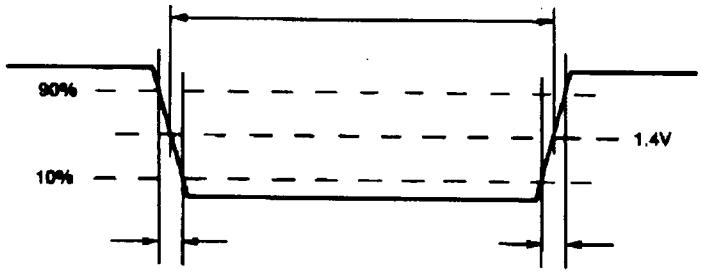


Fig 1. AC Input Conditions

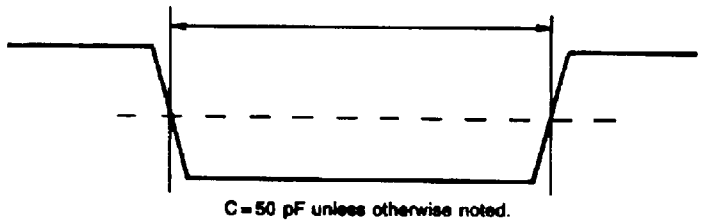


Fig 2. AC Output Conditions

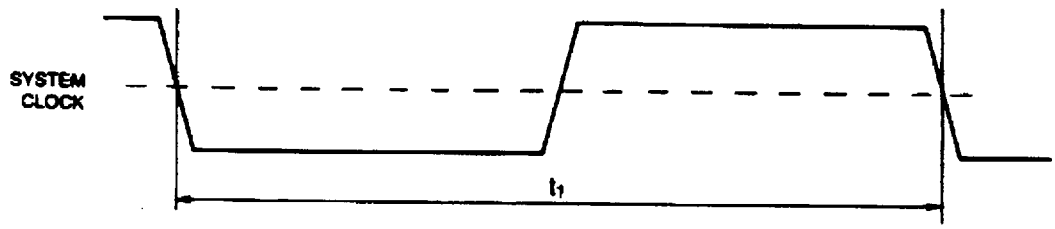


Fig 3. System Clock Timing

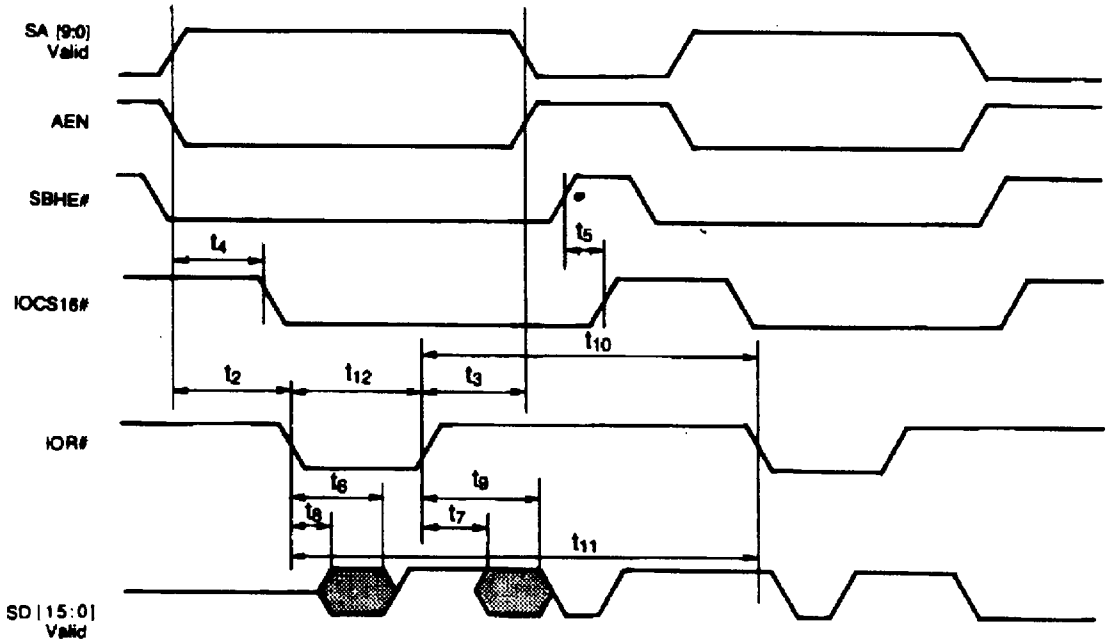


Fig 4. PIO Data Read Cycle

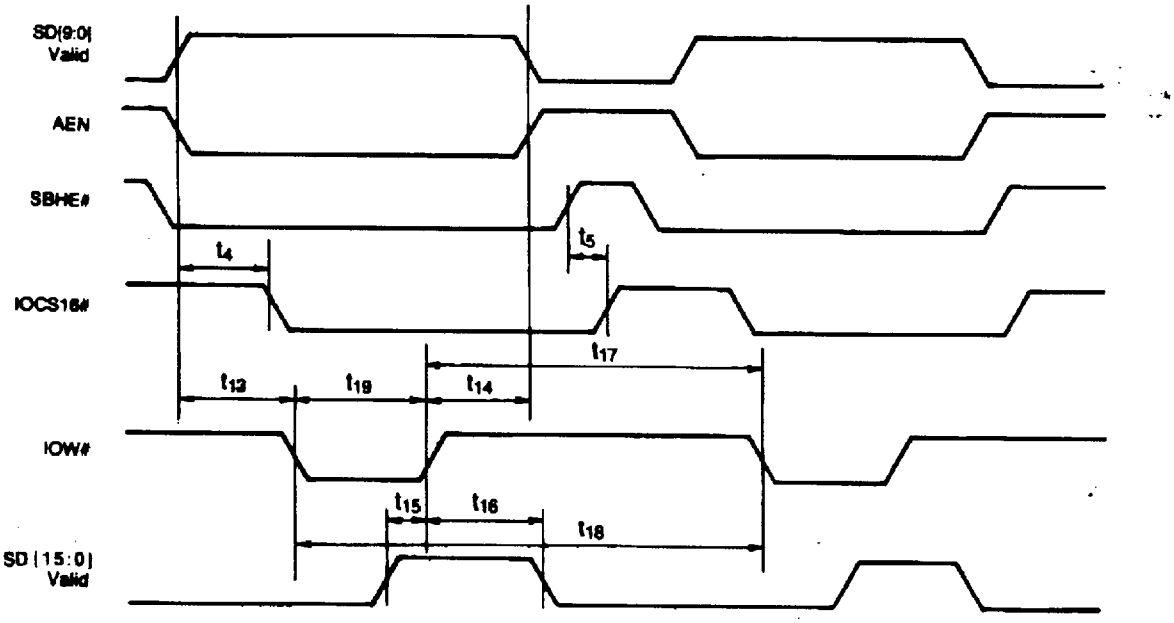


Fig 5. PIO Data Write Cycle

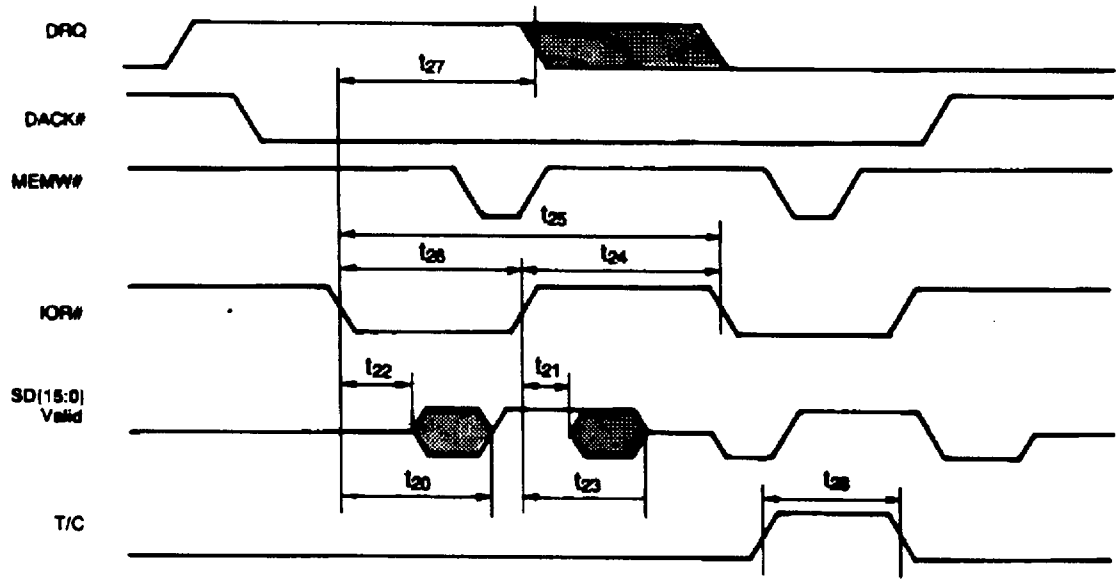


Fig 6. DMA Data Read Cycle

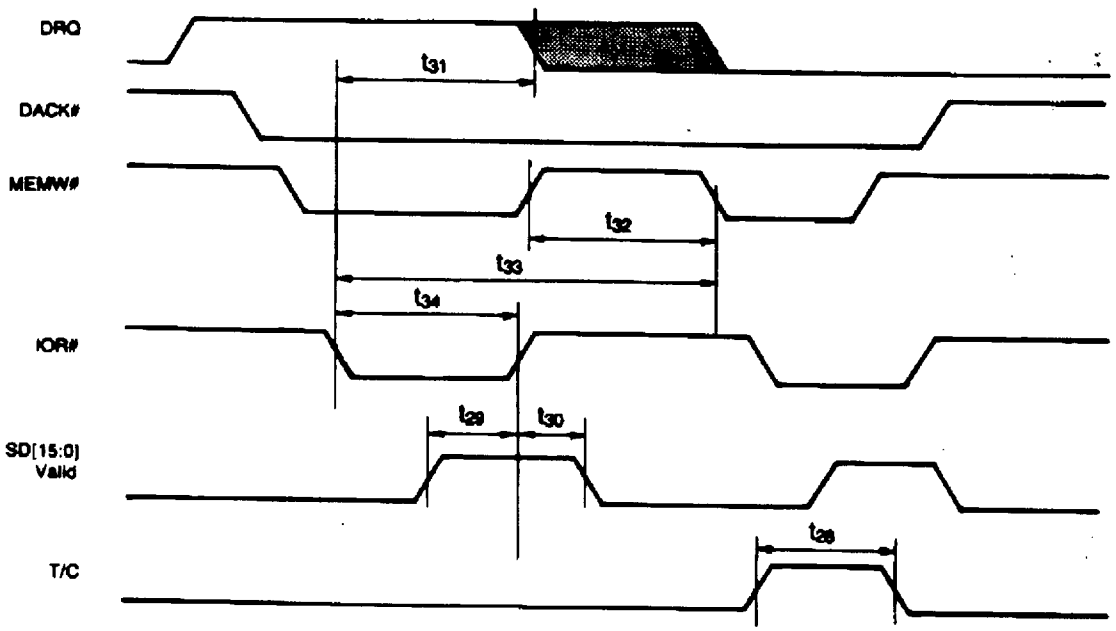


Fig 7. DMA Data Write Cycle

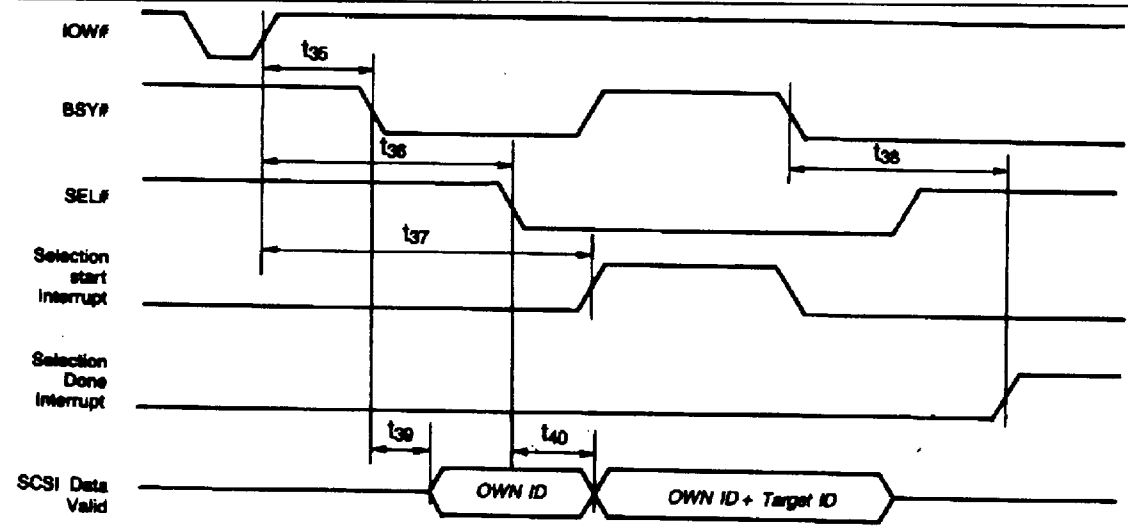


Fig 8. SCSI Bus Arbitration/Selection Timing

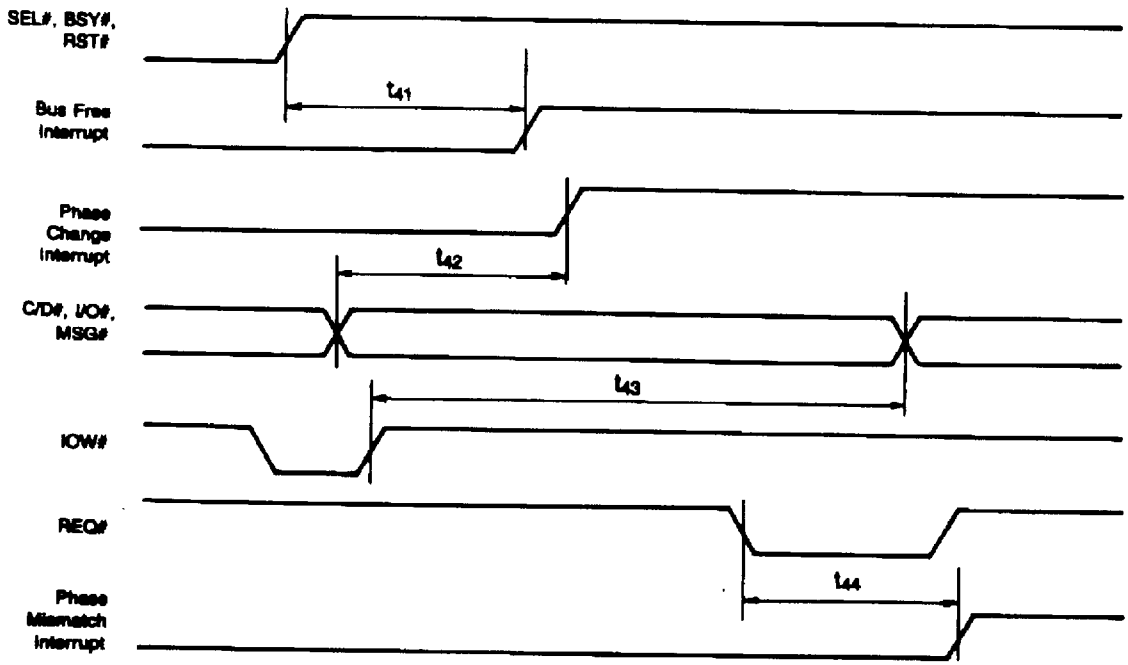


Fig 9. SCSI Bus free Detection and Phase Change Interrupts

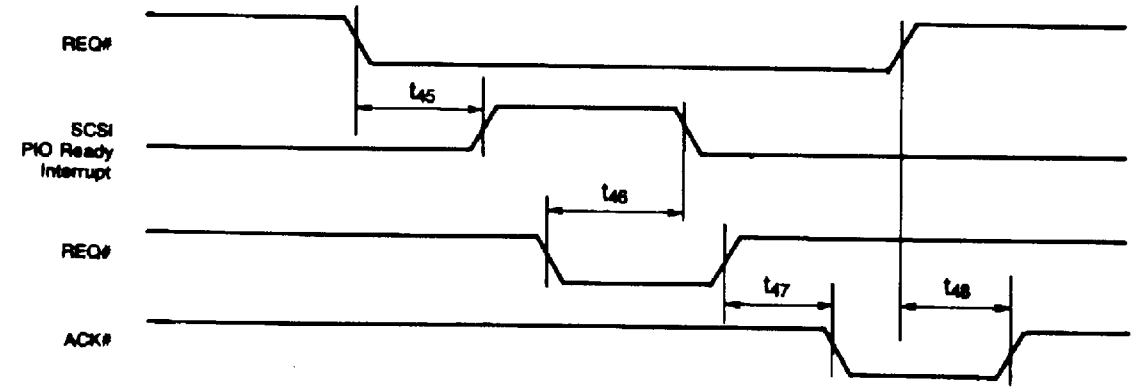


Fig 10. SCSI PIO Timing

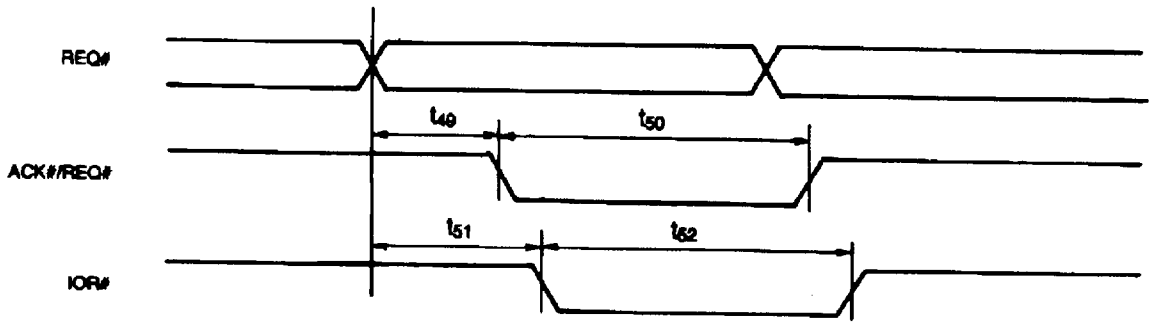
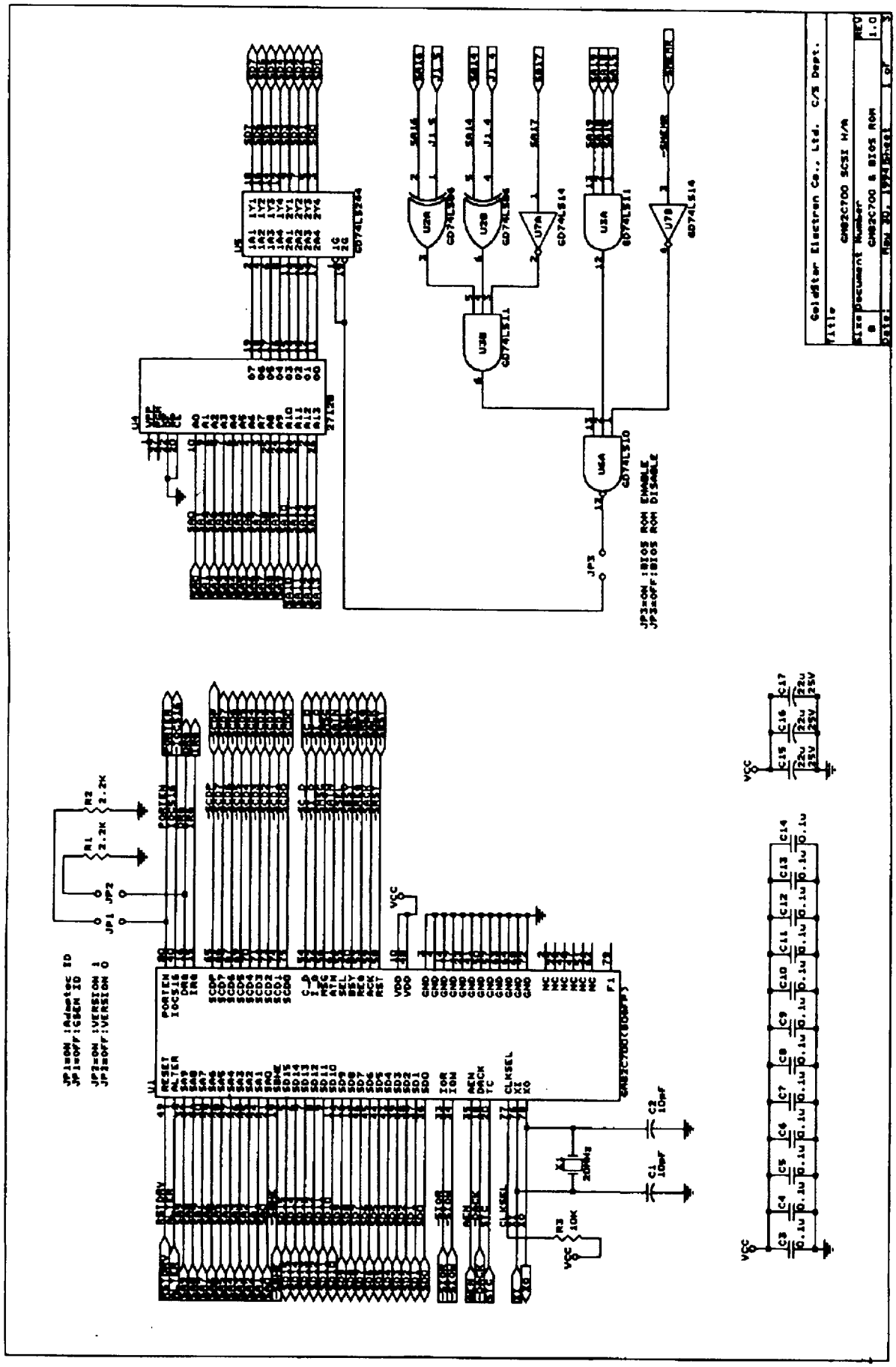
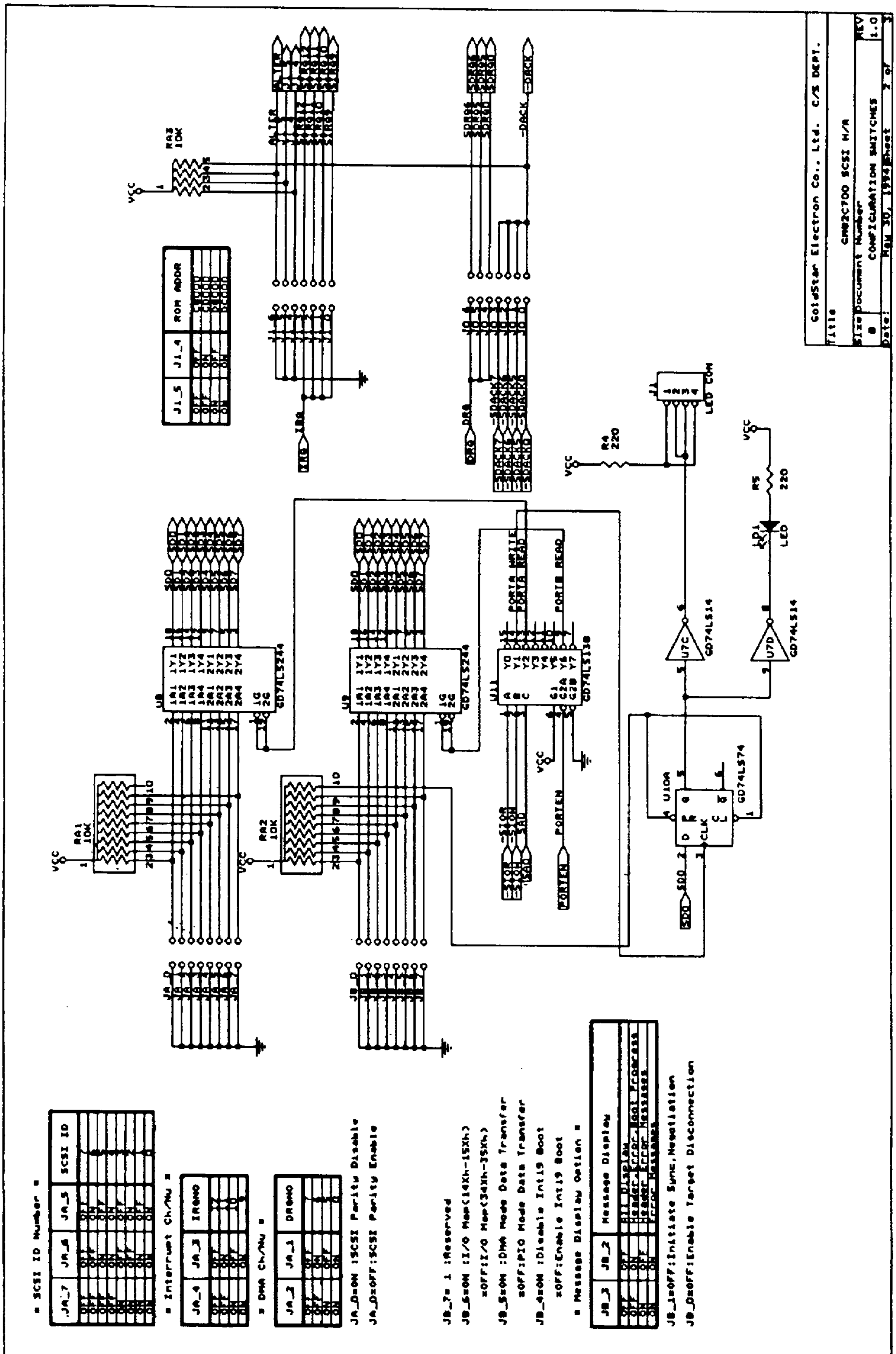


Fig 11. SCSI Data Setup and Hold, Latched Data and PIO


Goldstar Electron Co., Ltd. C/S Dept.
Title
GM82C700 SCSI H/A
Size
Document Number
GM82C700 & BIOS ROM
REV
1.0
Date:
Sheet
JP3=ON :BIOS ROM ENABLE
JP3=OFF:BIOS ROM DISABLE
JP1=ON :Adaptec ID
JP1=OFF:ISACH ID
JP2=ON :VERSION 1
JP2=OFF:VERSION 0
VCC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JA_7 JA_6 JA_5 SCSI ID
* Interrupt Ch/Nu *
JA_4 JA_3 IRQNO
* DMA Ch/Nu *
JA_2 JA_1 DRQNO
JA_0=ON :SCSI Parity Disable
JA_0=OFF:SCSI Parity Enable
JB_7= 1 :Reserved
JB_6=ON :I/O Map(14Xh-15Xh)
=OFF:I/O Map(34Xh-35Xh)
JB_5=ON :DMA Mode Data Transfer
=OFF:PIO Mode Data Transfer
JB_4=ON :Disable Int19 Boot
=OFF:Enable Int19 Boot
* Message Display Option *
JB_3 JB_2 Message Display
All Display
Header,Error,Boot Progress
Header Error Messages
Error Messages
JB_1=OFF:Initiate Sync,Negotiation
JB_0=OFF:Enable Target Disconnection
J1_5 J1_4 ROM ADDR
RA1 10K
RA2 10K
RA3 10K
U8 GD74LS244
U9 GD74LS244
U11 GD74LS138
U10A GD74LS74
U7C GD74LS14
U7D GD74LS14
PORTA WRITE
PORTA READ
PORTB READ
PORTEN
R4 220
R5 220
LD1 LED
J1 LED CON
GoldStar Electron Co., Ltd. C/S DEPT.
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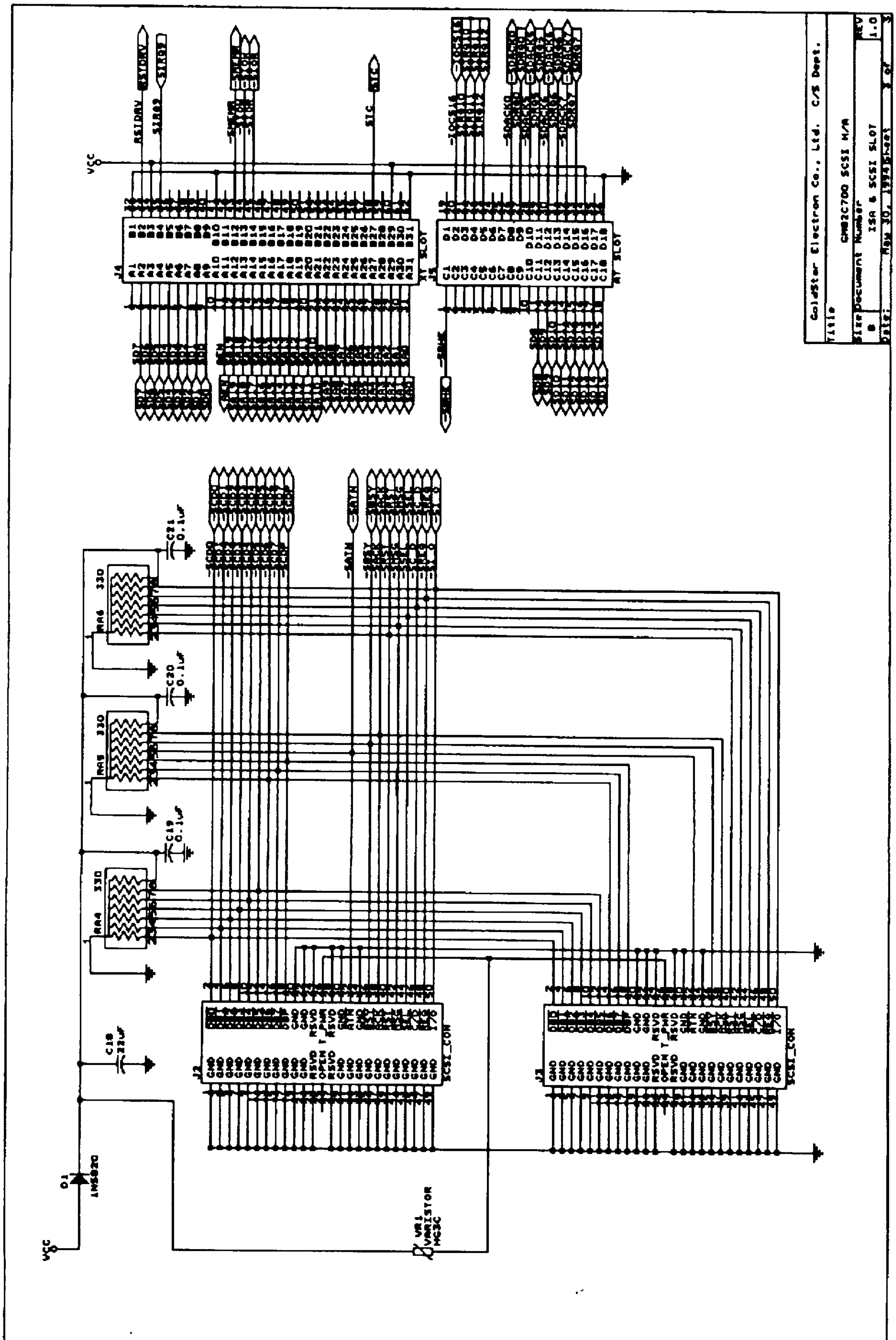
Size B
Document Number CONFIGURATION SWITCHES
REV 1.0
Date: May 30, 1994 Sheet 2 of 3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Size B
Document Number
ISA & SCSI SLOT
REV 1.0
Date: May 30, 1994 Sheet 3 of 3