RoHS

COMPLIANT

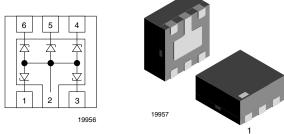
HALOGEN FREE

GREEN



Vishay Semiconductors

5-Line ESD Protection Diode Array in LLP75-6L



MARKING (example only)



Dot = pin 1 marking XX = date code

YY = type code (see table below)

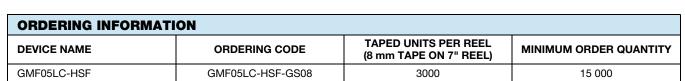
DESIGN SUPPORT TOOLS click logo to get started



FEATURES

- Ultra compact LLP75-6L package
- Low package profile < 0.6 mm
- 5-line ESD protection
- Low leakage current I_R < 0.1 μA
- Low load capacitance of typ. 43 pF at V_B = 0 V
- ESD immunity acc. IEC 61000-4-2 ± 30 kV contact discharge ± 30 kV air discharge
- Working voltage range V_{RWM} = 5 V
- e4 precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912





PACKAGE DATA								
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS		
GMF05LC-HSF	LLP75-6L	1B	4.2 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals		

ABSOLUTE MAXIMUM RATINGS GMF05LC-HSF							
PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT			
Peak pulse current	BiAs-mode: each input (pin 1; 3 to pin 6) to acc. IEC 61000-4-5; t _p = 8/20 μs; sing	I _{PPM}	5	Α			
Peak pulse power	BiAs-mode: each input (pin 1; 3 to pin 6) to acc. IEC 61000-4-5; t _p = 8/20 μs; sing	P _{PP}	70	W			
ESD immunity	BiAs-mode: each input (pin 1; 3 to pin 6) to ground (pin 2); acc. IEC 61000-4-2; 10 pulses	Contact discharge	V_{ESD}	± 30	kV		
Lob initiality		Air discharge	VESD	± 30	kV		
Operating temperature	Junction temperature	T_J	-55 to +125	°C			
Storage temperature			T _{STG}	-55 to +150	°C		



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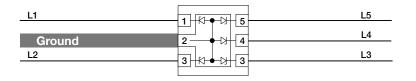
BIAs-MODE (5-line bidirectional asymmetrical protection mode)

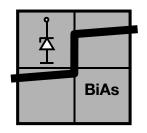
With the GMF05LC-HSF up to 5 signal- or data-lines (L1 to L5) can be protected against voltage transients. With pin 2 connected to ground and pin 1; pin 3 up to pin 6 connected to a signal- or data-line which has to be protected. As long as the voltage level on the data- or signal-line is between 0 V (ground level) and the specified maximum reverse working voltage (V_{RWM}) the protection diode between data-line and ground offer a high isolation to the ground line. The protection device behaves like an open switch.

As soon as any positive transient voltage signal exceeds the break through voltage level of the protection diode, the diode becomes conductive and shorts the transient current to ground. Now the protection device behaves like a closed switch. The clamping voltage (V_C) is defined by the breakthrough voltage (V_{BR}) level plus the voltage drop at the series impedance (resistance and inductance) of the protection device.

Any negative transient signal will be clamped accordingly. The negative transient current is flowing in the forward direction of the protection diode. The low forward voltage (V_F) clamps the negative transient close to the ground level.

Due to the different clamping levels in forward and reverse direction the GMF05LC-HSF clamping behavior is bidirectional and asymmetrical (BiAs).





ELECTRICAL CHARACTERISTICS GMF05LC-HSF								
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT		
Protection paths	Number of lines which can be protected	N _{channel}	-	-	5	lines		
Reverse stand-off voltage	at I _R = 1 μA	V_{RWM}	-	-	5	V		
Reverse current	at $V_R = V_{RWM} = 5 \text{ V}$	I _R	-	0.01	0.1	μΑ		
Reverse breakdown voltage	at I _R = 1 mA V _B		6	-	8	V		
Devenue alemania e velha e	at I _{PP} = 1 A acc. IEC 61000-4-5	V _C	-	8	9.5	V		
Reverse clamping voltage	at I _{PP} = I _{PPM} = 5 A acc. IEC 61000-4-5] VC	-	11.5	12.5	V		
Forward clamping voltage	at I _F = 1 A acc. IEC 61000-4-5	V_{F}	-	1.5	2	V		
	at I _{PP} = I _{PPM} = 5 A acc. IEC 61000-4-5	V _F	=	3.1	4	V		
Capacitance	at V _R = 0 V; f = 1 MHz		-	43	50	pF		
	at V _R = 2.5 V; f = 1 MHz	- C _D	-	25	-	pF		

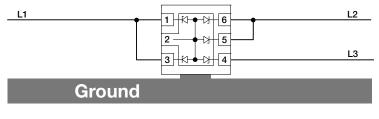
Note

Ratings at 25 °C ambient temperature, unless otherwise specified. BiAs mode: each input (pin 1, 2, 3, to 6) to ground (pin 2).

If a higher surge current or peak pulse current (I_{PP}) is needed, some protection diodes in the GMF05LC-HSF can also be used in parallel in order to "multiply" the performance.

If two diodes are switched in parallel you get

- double surge power = double peak pulse current (2 x I_{PPM})
- half of the line inductance = reduced clamping voltage
- half of the line resistance = reduced clamping voltage
- double line capacitance (2 x C_D)
- double reverse leakage current (2 x I_R)



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TYPICAL CHARACTERISTICS

T_{amb} = 25 °C, unless otherwise specified

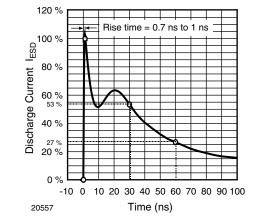


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330 Ω /150 pF)

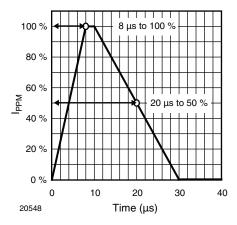


Fig. 2 - 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5

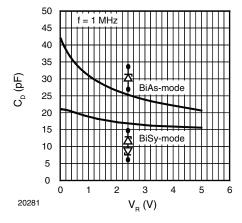


Fig. 3 - Typical Capacitance C_D vs. Reverse Voltage V_R

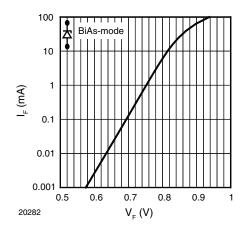


Fig. 4 - Typical Forward Current I_{F} vs. Forward Voltage V_{F}

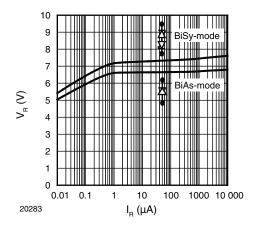


Fig. 5 - Typical Reverse Voltage V_{R} vs. Reverse Current I_{R}

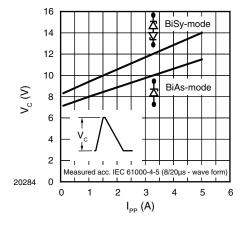


Fig. 6 - Typical Peak Clamping Voltage V_{C} vs. Peak Pulse Current I_{PP}

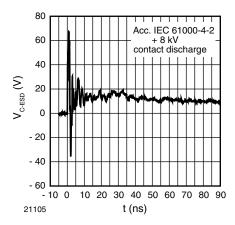


Fig. 7 - Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)

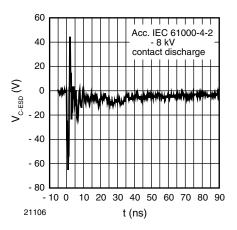


Fig. 8 - Typical Clamping Performance at - 8 kV Contact Discharge (acc. IEC 61000-4-2)

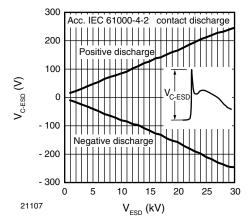
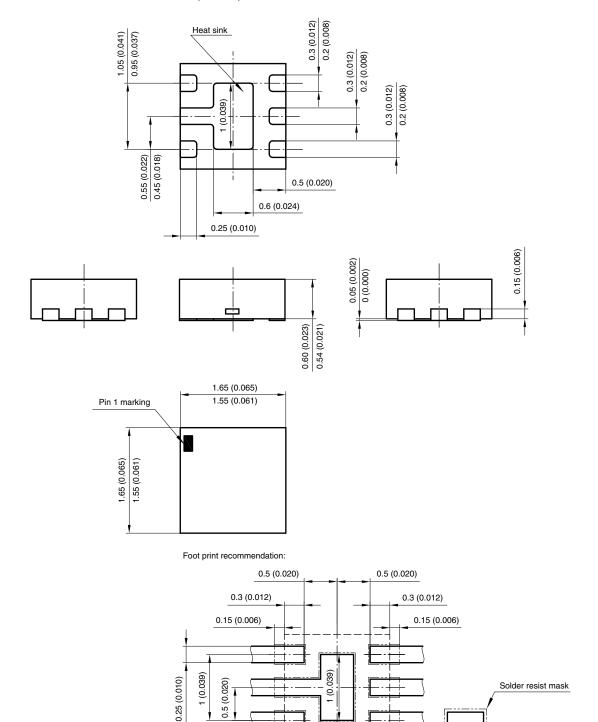


Fig. 9 - Typical Peak Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)

Solder pad

PACKAGE DIMENSIONS in millimeters (inches): LLP75-6L

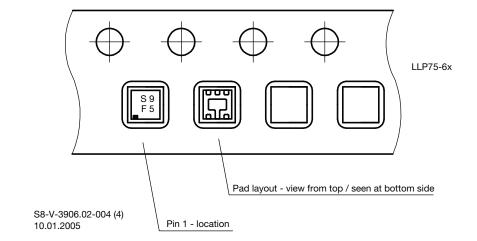


Document no.:S8-V-3906.02-010 (4) Created - Date: 04. MAY 2005 Rev. 4 - Date: 21. March 2006

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