GMS81504
CMOS SINGLE-CHIP 8-BIT MICROCONTROLLER

OVERVIEW

Description

The GMS81504 is a high-performance CMOS 8-bit microcontroller with 4K bytes of ROM. The device is one of GMS800 family. The HYUNDAI GMS81504 is a powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. The GMS81504 provides the following standard features: 4K bytes of ROM, 128 bytes of RAM, 23 I/O lines(21 lines for 28SOP), 16-bit or 8-bit timer/counter, a precision analog to digital converter, on-chip oscillator and clock circuitry. In addition, the GMS81504 supports power saving modes to reduce power consumption. The Stop Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset or external interrupt.

ROM size	RAM size	Package	Device name
4K bytes	128 bytes	30SDIP	GMS81504 K
		28SOP	GMS81504 D
4K bytes (OTP)	128 bytes	30SDIP	GMS81504T K

Features

- **4K On-chip Program Memory**
- **128 Bytes of On-Chip Data RAM**
- **Instruction execution time: 0.5us at 8MHz**
- **2.7V to 5.5V Wide Operating Range**
- **1~8 MHz Operating frequency**
- **Basic Interval Timer**
- **Two 8-Bit Timer/ Counters (can be used as one 16-bit)**
- **Two external interrupt ports**
- **One Programmable Clock Out port**
- **One Buzzer Driving port**
- **23 Programmable I/O Lines**
- **Seven Interrupt Sources**
- **All LED Direct Drive Output Ports**
- **4-Channel 8-Bit On-Chip Analog to Digital Converter**
- **Power Down Mode (STOP Mode)**

Development Tools

The GMS800 family is supported by a full-featured macro assembler, an in-circuit emulators CHOICE-Jr.TM, socket adapters for OTP device.

The availability of OTP devices are especially useful for customers expecting frequent code changes and updates. The OTP devices, packaged in plastic packages permit the user to program them once. In addition to the program memory, the configuration fuses must be programmed.

In-Circuit Emulators	CHOICE-Jr.TM
OTP devices	GMS81504T K (30 SDIP)
Socket Adapters for OTP Devices	OA815A-30SD (30 SDIP)
Assembler	HME Macro Assembler

BLOCK DIAGRAM

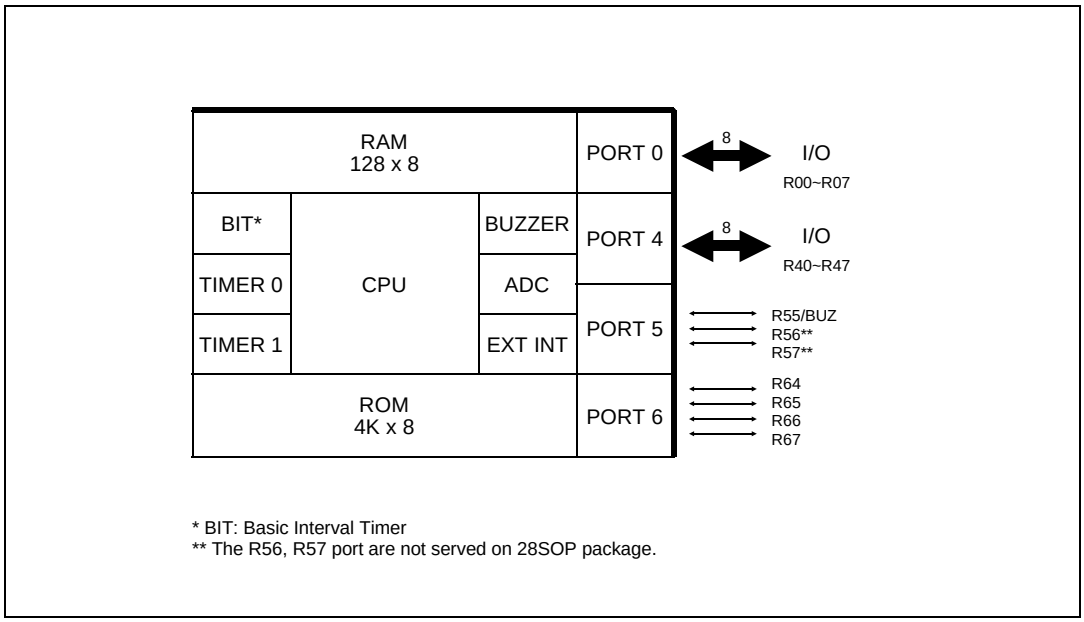
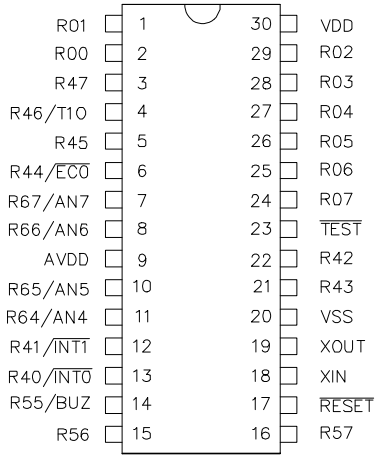
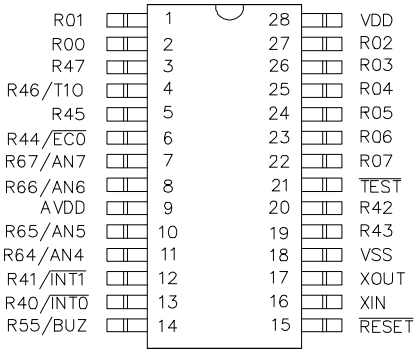


Figure 1. Block Diagram

PIN ASSIGNMENT



30 SDIP



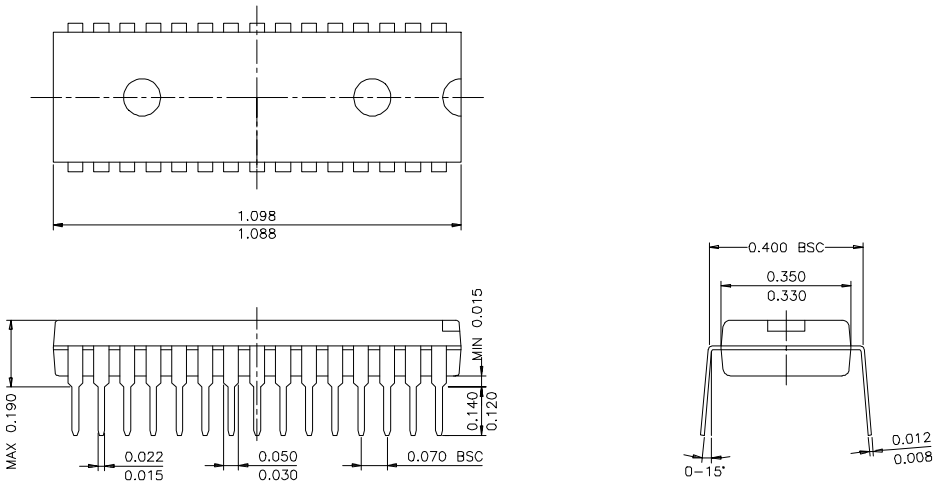
28 SOP

Figure 2. Pin Connections

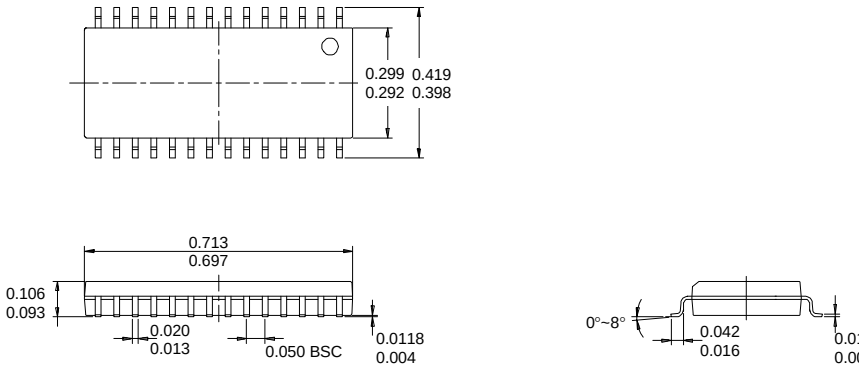
PACKAGES

Unit: INCH

30 SDIP



28 SOP



PIN DESCRIPTIONS

V_{DD}: Supply voltage.

V_{SS}: Circuit Ground.

$\overline{TEST}$: For test purposes only. Connect it to V_{DD}.

$\overline{RESET}$: Reset the MCU.

X_{IN}: Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

X_{OUT}: Output from the inverting oscillator amplifier.

R00~R07: R0 is an 8-bit, CMOS, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. R0 pins that have 1 or 0 written to their Port Direction Mode Register, can be used as outputs or inputs.

R40~R47: R4 is an 8-bit, CMOS, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. R4 pins that have 1 or 0 written to their Port Direction Mode Register, can be used as outputs or inputs.

In addition, Port R40, R41, R44, R46 serve the functions of the various following special features.

Port Pin	Alternate Function
R40	INT0 (External Interrupt 0)
R41	INT1 (External Interrupt 1)
R44/$\overline{EC0}$	EC0 (External Count Input to Timer/Counter 0)
R46	T1O (Timer 1 Clock-Out)

R55, R56, R57: R5 is a 3-bit, CMOS, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. R5 pins that have 1 or 0 written to their Port Direction Mode Register, can be used as outputs or inputs. R56 and R57 differs in having internal pull-ups.

Port R55 serves the functions of special features.

Port Pin	Alternate Function
R55	BUZ (Square wave output for Buzzer driving)

R64~R67: R6 is an 4-bit, CMOS, bidirectional I/O port. R64~R67 are bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. R64~R67 pins that have 1 or 0 written to their Port Direction Mode Register, can be used as outputs or inputs.

R6 serves the analog to digital converter functions of following.

Port Pin	Alternate Function
R64	AN4 (ADC input 4)
R65	AN5 (ADC input 5)
R66	AN6 (ADC input 6)
R67	AN7 (ADC input 7)

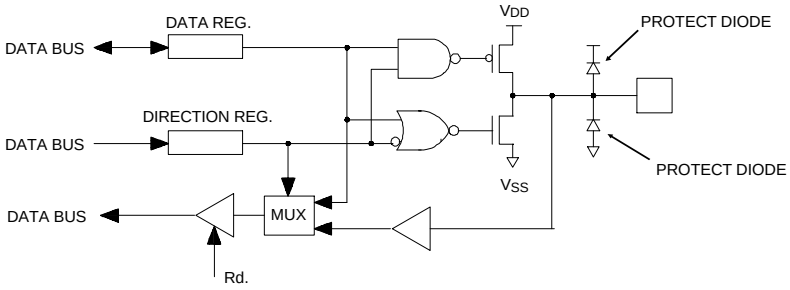
AV_{DD}: Supply voltage to the ladder resistor of ADC circuit. To enhance the resolution of analog to digital converter, use independent power source as well as possible, other than digital power source.

Port Pin	I/O	Descriptions		Pull-up/ Pull-down	RESET	STOP Mode
		Primary Functions	Secondary Functions			
V_{DD}	-	Power supply to MCU	-	-	-	-
V_{SS}	-	Ground	-	-	-	-
AV_{DD}	-	Power supply for ADC	-	-	-	-
$\overline{TEST}$	I	Test mode	-	-	-	-
$\overline{RESET}$	I	Reset the MCU	-	Pull-up	Low	Last state
X_{IN}	I	Oscillation input	-	-	Oscillation	Low
X_{OUT}	O	Oscillation output	-	-	Oscillation	High
R00~R07	I/O	General I/O	-	-	Input 3)	Last state
R40/INT0 R41/INT1 R42 R43 R44/$\overline{EC0}$ R45 R46/T1O R47	I/O I/O I/O I/O I/O I/O I/O I/O	General I/O " " " " " " "	External interrupt 0 External interrupt 1 - - External count input 0 - Timer 1 output -	- - - - - - - -	Input 3)	Last state
R55/BUZ R56 1) R57 1)	I/O I/O I/O	General I/O " "	Buzzer driving output - -	- Pull-up 2) Pull-up 2)	Input 3)	Last state
R64/AN4 R65/AN5 R66/AN6 R67/AN7	I/O I/O I/O I/O	General I/O " " "	Analog input 4 Analog input 5 Analog input 6 Analog input 7	- - - -	Input 3)	Last state

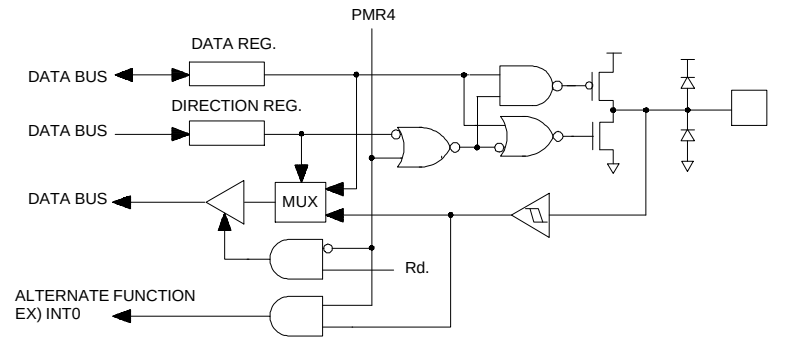
NOTES:
1) R56 and R57 are not physically served on 28 pin SOP package.
2) When input mode is selected, pull-up is activated. In output mode, pull-up is de-activated.
3) During MCU reset, status of R56,R57 are weak high (Typ. impedance 50~100KΩ). Other pin impedance is very high(High-Z).

PORT STRUCTURES

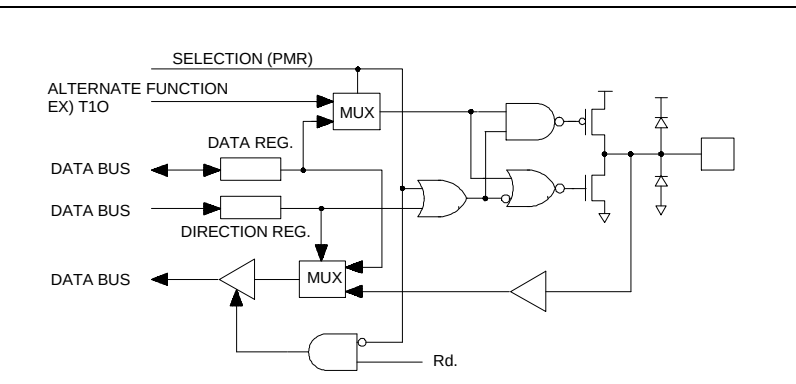
R00~R07, R47



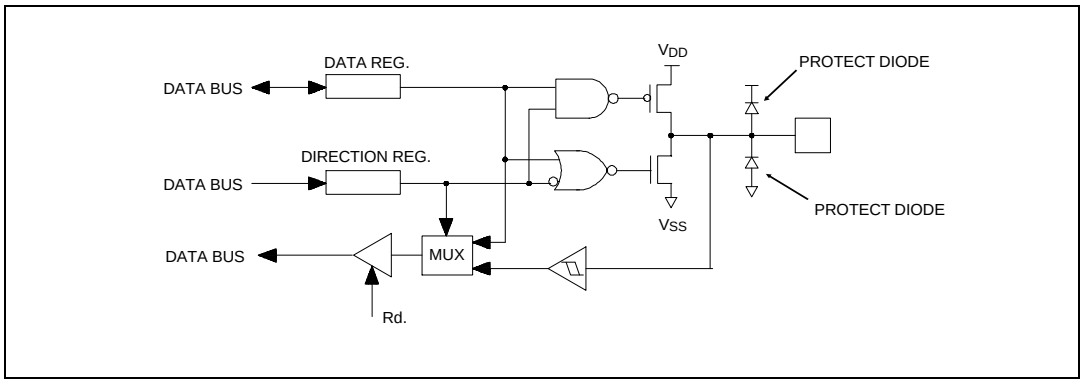
R40/INT0, R41/INT1, R44/$\overline{EC0}$



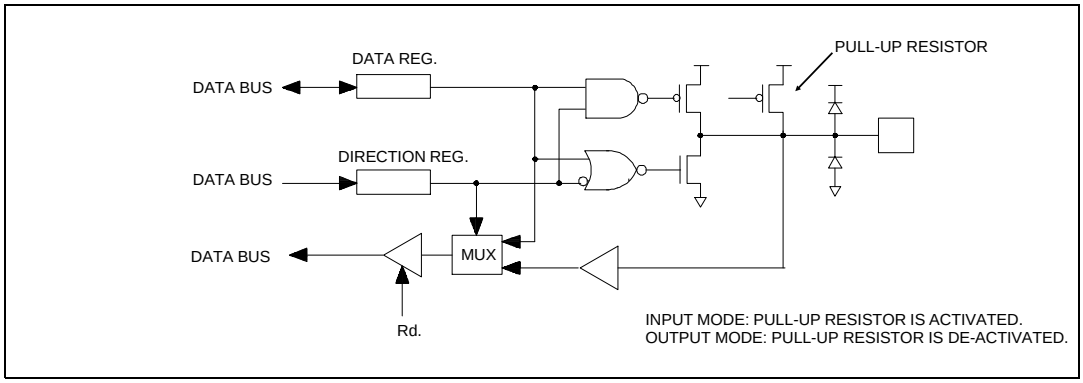
R46/T1O, R55/BUZ



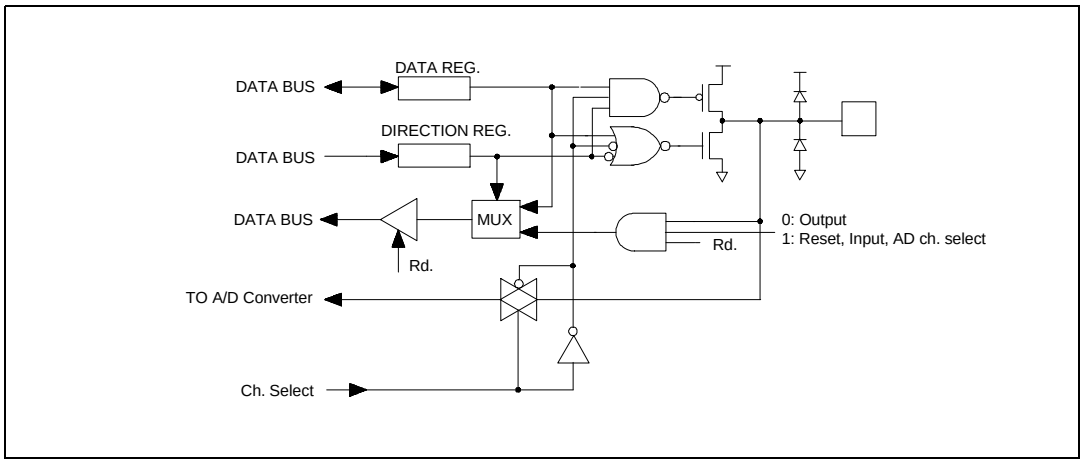
R42, R43, R45



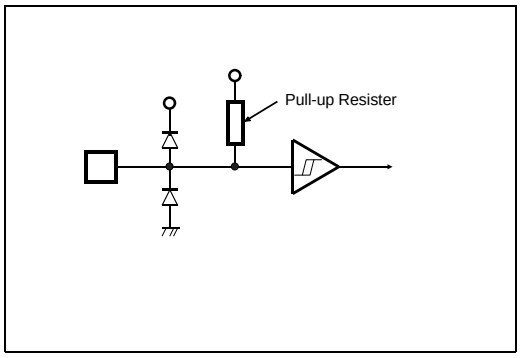
R56, R57



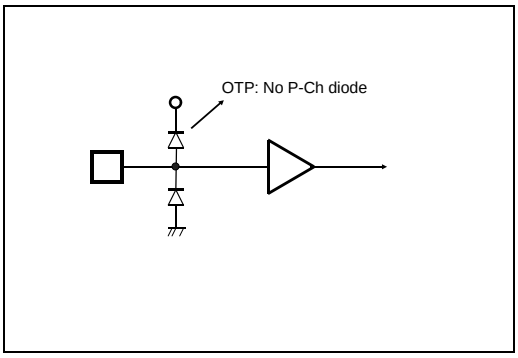
R64/AN4, R65/AN5, R66/AN6, R67/AN7



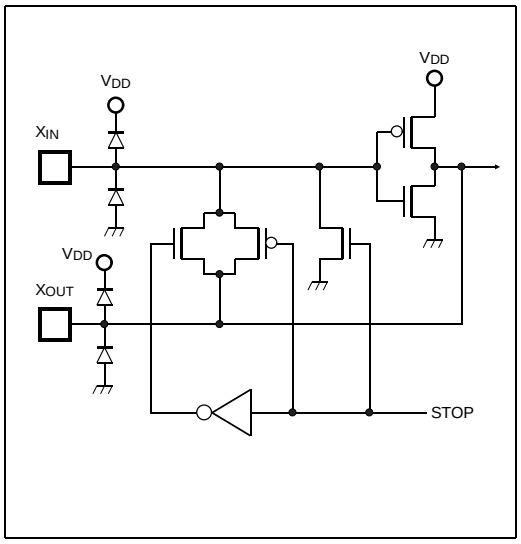
$\overline{\text{RESET}}$



$\overline{\text{TEST}}$



X_{IN}, X_{OUT}



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Supply Voltage . . . . . -0.3 to +6.0 V
Storage Temperature . . . . . -40 to +125 °C
Voltage on any pin with
respect to Ground (V_{SS}) . . . . . -0.3 to V_{DD}+0.3 V
Maximum current out of V_{SS} pin . . . . . 150 mA
Maximum current into V_{DD} pin . . . . . 100 mA
Maximum output current sunk by (I_{OL} per I/O Pin)
R00~R07, R42, R43, R56, R57 . . . . . 30 mA
R40, R41, R44~R47, R55, R64~67 . . . . . 20 mA
Maximum output current sourced by (I_{OH} per I/O Pin)
R00~R07, R42, R43, R56, R57 . . . . . 24 mA
R40, R41, R44~R47, R55, R64~67 . . . . . 18 mA
Maximum current (ΣI_{OL}) . . . . . 120 mA
Maximum current (ΣI_{OH}) . . . . . 100 mA

Notice:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these of any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	Specifications		Unit
			Min.	Max.	
Supply Voltage	V_{DD}	f_{XIN} = 8 MHz f_{XIN} = 4 MHz	4.5 2.7	5.5 5.5	V
Operating Frequency	f_{XIN}	V_{DD} = 4.5~5.5V V_{DD} = 2.7~5.5V	1.0 1.0	8.0 4.2	MHz
Operating Temperature	T_{OPR}		-20	80	°C

DC Characteristics (5V)

(V_{DD} = 5.0V± 10%, V_{SS} = 0V, T_A = -20 ~ 80 °C, f_{XIN} = 8 MHz)

Parameter	Pin	Symbol	Test Condition	Specifications			Unit
				Min.	Typ.*	Max.	
Input High Voltage	X_{IN}	V_{IH1}	-	$0.9V_{DD}$	-	V_{DD}	V
	$\overline{RESET}$, R0, R4, R5, R6	V_{IH2}	-	$0.8V_{DD}$	-	V_{DD}	V
Input Low Voltage	X_{IN}	V_{IL1}	-	0	-	$0.1V_{DD}$	V
	$\overline{RESET}$, R0, R4, R5, R6	V_{IL2}	-	0	-	$0.2V_{DD}$	V
Output High Voltage	R0, R4, R5, R6	V_{OH}	V_{DD} = 5V I_{OH} = -2mA	V_{DD}-1.0	V_{DD}-0.2	-	V
Output Low Voltage	R40, R41, R44~R47, R55, R6	V_{OL1}	V_{DD} = 5V I_{OL} = 5mA	-	0.3	1.0	V
	R0, R42, R43, R56, R57	V_{OL2}	V_{DD} = 5V I_{OL} = 10mA	-	0.6	1.0	V
Input Leakage Current	$\overline{RESET}$, R0, R4, R5, R6	I_{IH}	$V_I = V_{DD}$	-5.0	-	5.0	uA
		I_{IL}	V_I = 0V	-5.0	-	5.0	uA
Input Pull-up Current	$\overline{RESET}$	I_{P1}	V_{DD} = 5V	-180	-120	-30	uA
	R56, R57	I_{P2}	V_{DD} = 5V	-90	-60	-15	uA
Power Current	Operating mode	I_{DD}	f_{XIN}=8MHz	-	5	40	mA
	STOP mode	I_{STOP}	V_{DD} = 5V	-	2	30	uA
Hysteresis	$\overline{RESET}$, R40~R45	V_T+ ~V_T-	V_{DD} = 5V	0.5	0.8	-	V

* : Data in "Typ" column is at 5 V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

A/D Converter Characteristics (5V)

(V_{DD} = 5.0V± 10%, V_{AIN} = 5.0V, V_{SS} = 0V, T_A = 25 °C)

Parameter	Symbol	Specifications			Unit
		Min.	Typ.*	Max.	
Analog Input Range	V_{AIN}	V_{SS}	-	AV_{DD}	V
Overall Accuracy	A_{CC}	-	±2.0	±3.0	LSB
Conversion Time	T_{CONV}	-	-	40	uS
Analog power supply Input Range	V_{AVDD}	4.5	5.0	5.5	V

* : Data in "Typ" column is at 5 V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

DC Characteristics (3V)

(V_{DD} = 3.0V± 10%, V_{SS} = 0V, T_A = -20 ~ 80 °C, f_{XIN} = 4 MHz)

Parameter	Pin	Symbol	Test Condition	Specifications			Unit
				Min.	Typ.*	Max.	
Input High Voltage	X_{IN}	V_{IH1}	-	$0.9V_{DD}$	-	V_{DD}	V
	$\overline{RESET}$, R0, R4, R5, R6	V_{IH2}	-	$0.8V_{DD}$	-	V_{DD}	V
Input Low Voltage	X_{IN}	V_{IL1}	-	0	-	$0.1V_{DD}$	V
	$\overline{RESET}$, R0, R4, R5, R6	V_{IL2}	-	0	-	$0.2V_{DD}$	V
Output High Voltage	R0, R4, R5, R6	V_{OH}	V_{DD} = 3V I_{OH} = -2mA	V_{DD} -1.0	V_{DD}-0.4	-	V
Output Low Voltage	R40, R41, R44~R47, R55, R6	V_{OL1}	V_{DD} = 3V I_{OL} =2mA	-	0.3	1.0	V
	R0, R42, R43, R56, R57	V_{OL2}	V_{DD} = 3V I_{OL} = 5mA		0.4	1.0	V
Input Leakage Current	$\overline{RESET}$, R0, R4, R5, R6	I_{IH}	$V_I = V_{DD}$	-3.0	-	3.0	uA
		I_{IL}	V_I = 0V	-3.0	-	3.0	uA
Input Pull-up Current	$\overline{RESET}$	I_{P1}	V_{DD} = 3V	-15	-30	-60	uA
	R56, R57	I_{P2}	V_{DD} = 3V	-7.5	-15	-30	uA
Power Current	Operating mode	I_{DD}	f_{XIN}=4MHz	-	1	5	mA
	STOP mode	I_{STOP}	V_{DD} = 3V	-	1	10	uA
Hysteresis	$\overline{RESET}$, R40~R45	V_T+ ~V_T-	V_{DD} = 3V	0.3	0.6	-	V

* : Data in "Typ" column is at 3 V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
**: Power Fail Detection function is not available.

A/D Converter Characteristics (3V)

(V_{DD} = 3.0V± 10%, V_{AIN} = 3.0V, V_{SS} = 0V, T_A = 25 °C)

Parameter	Symbol	Specifications			Unit
		Min.	Typ.*	Max.	
Analog Input Range	V_{AIN}	V_{SS}	-	AV_{DD}	V
Overall Accuracy	A_{CC}	-	±1.5	±2.5	LSB
Conversion Time	T_{CONV}	-	-	40	uS
Analog power supply Input Range	V_{AVDD}	2.7	3.0	3.3	V

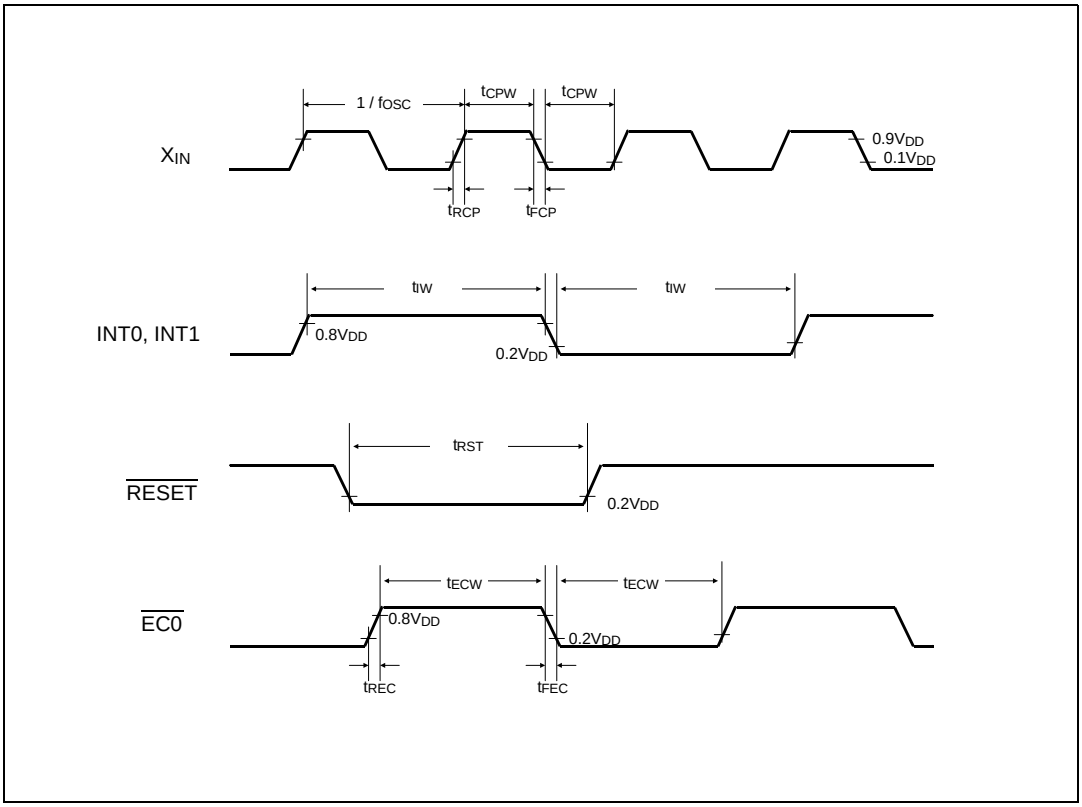
* : Data in "Typ" column is at 3 V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

AC Characteristics

(V_{DD} = 2.7~5.5V, V_{SS} = 0V, T_A = -20 ~ 80 °C)

Parameter	Pin	Symbol	Specifications			Unit
			Min.	Typ.	Max.	
Main clock frequency	X_{IN}	f_{XIN}	1	-	8	MHz
Oscillation stabilization Time	X_{IN}, X_{OUT}	t_{ST}	20	-	-	ms
External Clock Pulse Width	X_{IN}	t_{CPW}	80	-	-	ns
External Clock Transition Time	X_{IN}	t_{RCP}, t_{FCP}	-	-	20	ns
Interrupt Pulse Width	INT0, INT1	t_{IW}	2	-	-	t_{SYS}
RESET Input Low Width	$\overline{RESET}$	t_{RST}	8	-	-	t_{SYS}
Event Counter Input Pulse Width	$\overline{EC0}$	t_{ECW}	2	-	-	t_{SYS}
Event Counter Transition Time	$\overline{EC0}$	t_{REC}, t_{FEC}	-	-	20	ns

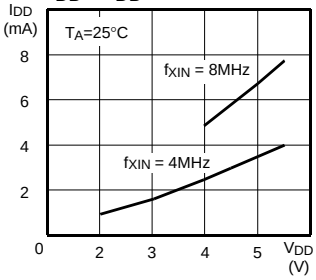
Timing Chart



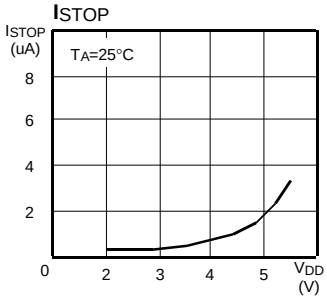
TYPICAL CHARACTERISTICS

These parameters are for design guidance only and are not tested.

I_{DD} - V_{DD}

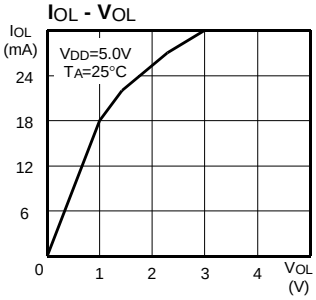


I_{STOP}



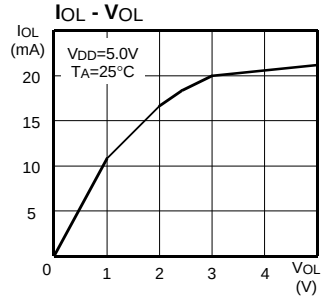
V_{DD}=5V

I_{OL} - V_{OL}



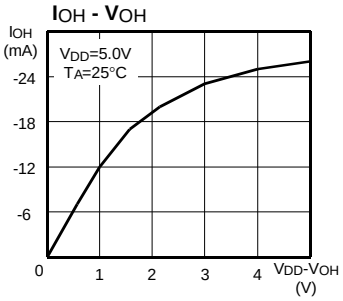
R00~R07, R42, R43, R56, R57

I_{OL} - V_{OL}



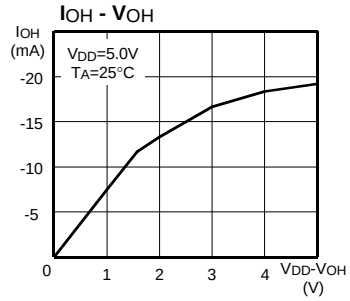
R40, R41, R44~R47, R55, R64~67

I_{OH} - V_{OH}



R00~R07, R42, R43, R56, R57

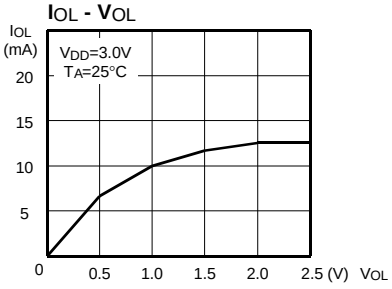
I_{OH} - V_{OH}



R40, R41, R44~R47, R55, R64~67

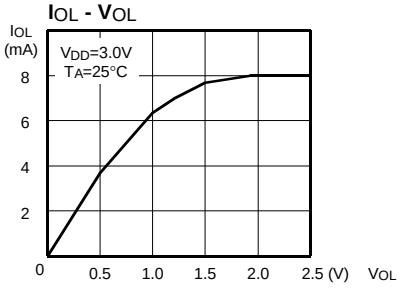
V_{DD}=3.0V

I_{OL} - V_{OL}



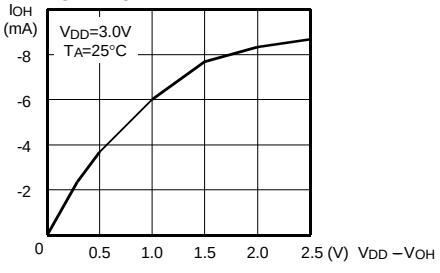
R00~R07, R42, R43, R56, R57

I_{OL} - V_{OL}



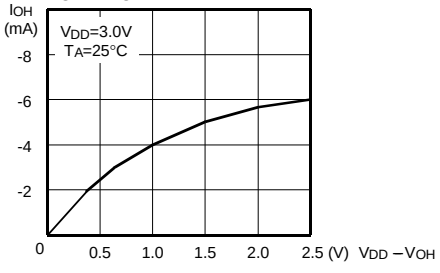
R40, R41, R44~R47, R55, R64~67

I_{OH} - V_{OH}



R00~R07, R42, R43, R56, R57

I_{OH} - V_{OH}



R40, R41, R44~R47, R55, R64~67

MEMORY ORGANIZATION

The GMS81504 has separate address spaces for Program and Data Memory. Program memory can only be read, not written to. It can be up to 4K bytes of Program Memory. Data memory can be read and written to up to 128 bytes including the stack area.

Registers

This device has six registers that are the Program Counter (PC), a Accumulator (A), two Index registers (X,Y), the Stack Pointer (SP) and the Program Status Word (PSW). The Program Counter consists of 16-bit register.

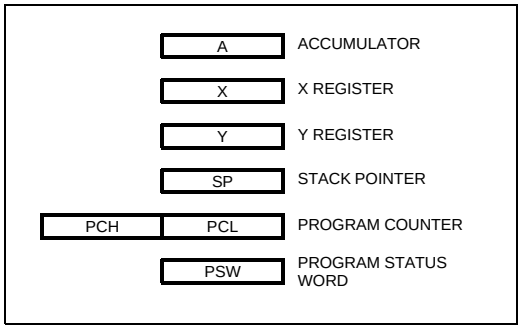


Figure 3. Configuration of Registers

Accumulator: The accumulator is the 8-bit general purpose register, used for data operation such as transfer, temporary saving and conditional judgment, etc.

The accumulator can be used as a 16-bit register with Y register as shown below.

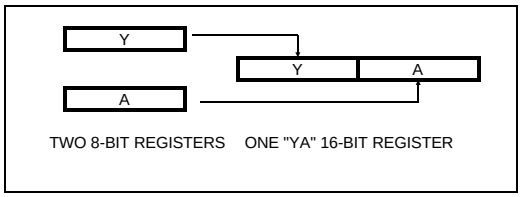


Figure 4. Configuration of YA 16-bit register

X register, Y register: In the addressing modes which use these index registers, the register contents are added to the specified address and this becomes the actual address. These modes are extremely effective for referencing subroutine tables and memory tables.

The index registers also have increment, decrement, compare and data transfer functions and they can be used as simple accumulators.

Stack Pointer: The stack pointer is an 8-bit register used for occurrence interrupts and calling out subroutines. The stack can be located at any position within 00_H to $7F_H$ of the internal data memory.

Caution:
The stack pointer must be initialized by software because its value is undefined after reset.

```
Ex)  LDX    #07FH
     TXSP               ; SP ← 7FH
```

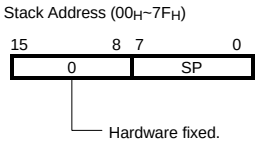


Figure 5. Stack Pointer

Caution:
To prevent overrapped between user RAM an system stack area, user have to consider using RAM.

Reset Routine Example:

```
          ORG     0F000H
RESET:    LDX     #0
          LDA     #0
CLR_LP:   STA     {X}+        ;RAM CLEAR
          CMPX    #80H
          BNE     CLR_LP
          LDX     #07FH       ;INITIALIZE SP.
          TXSP
          :
```

Program Counter: The program counter is a 16-bit wide which consists of two 8-bit registers, PCH, PCL. This counter indicates the address of the next instruction to be executed. In reset state, the program counter has reset vector address (PCH: FF_H, PCL: FE_H). .

Program Status Word : The Program Status Word (PSW) contains several status bits that reflect the current state of the CPU. The PSW shown in Figure 6. It contains the Negative flag, the Overflow flag, the Direct page flag, the Break flag, the Half Carry (for BCD operations), the Interrupt enable flag, the Zero

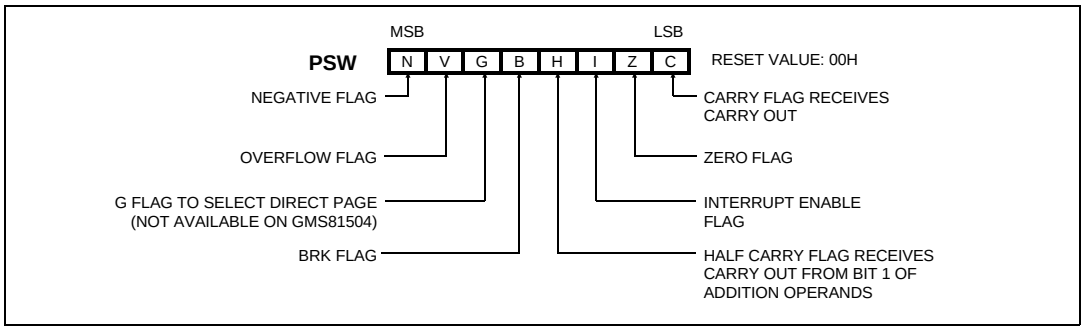


Figure 6. PSW (Program Status Word) Register

flag and the Carry bit.

[Carry flag C]
This flag stores any carry or borrow from the ALU of CPU after an arithmetic operation and is also changed by the Shift instruction or rotate instruction.

[Zero flag Z]
This flag is set when the result of an arithmetic operation or data transfer is "0" and is cleared by any other result.

[Interrupt disable flag I] This flag enables/disables all interrupts except interrupt caused by Reset or software BRK instruction. All interrupts are disabled when cleared to "0". This flag immediately becomes "0" when an interrupt is served. It is set by the EI instruction, cleared by the DI instruction.

[Half carry flag H]
After operation, set when there is a carry from bit 3 of ALU or there is not a borrow from bit 4 of ALU. This bit can not be set or cleared except CLRV instruction, clearing with Overflow flag (V).

[Break flag B]
This flag set by software BRK instruction to distinguish BRK from TCALL instruction which as the same vector address.

[Direct page flag G]
This flag is not available on GMS81504 because this flag is usable over 256 bytes RAM other than the GMS81504, assign direct page for direct addressing mode. In the direct addressing mode, addressing area is within zero page 00_H to FF_H when this flag is "0". If it is set to "1", addressing area is 100_H to $1FF_H$.
It is set by SETG instruction, and cleared by CLRG.

[Overflow flag V]
This flag is set to "1" when an overflow occurs in the result of an arithmetic operation involving signs. An overflow occurs when the result of an addition or subtraction exceeds +127($7F_H$) or -128(80_H).
The CLRV instruction clears the overflow flag. There is no set instruction. When the BIT instruction is executed, for other than the above, bit 6 of memory is copy to this flag.

[Negative flag N]
This flag is set to match the sign bit (bit 7) status of the result of a data or arithmetic operation. When the BIT instruction is executed, bit 7 of memory is copy to this flag.

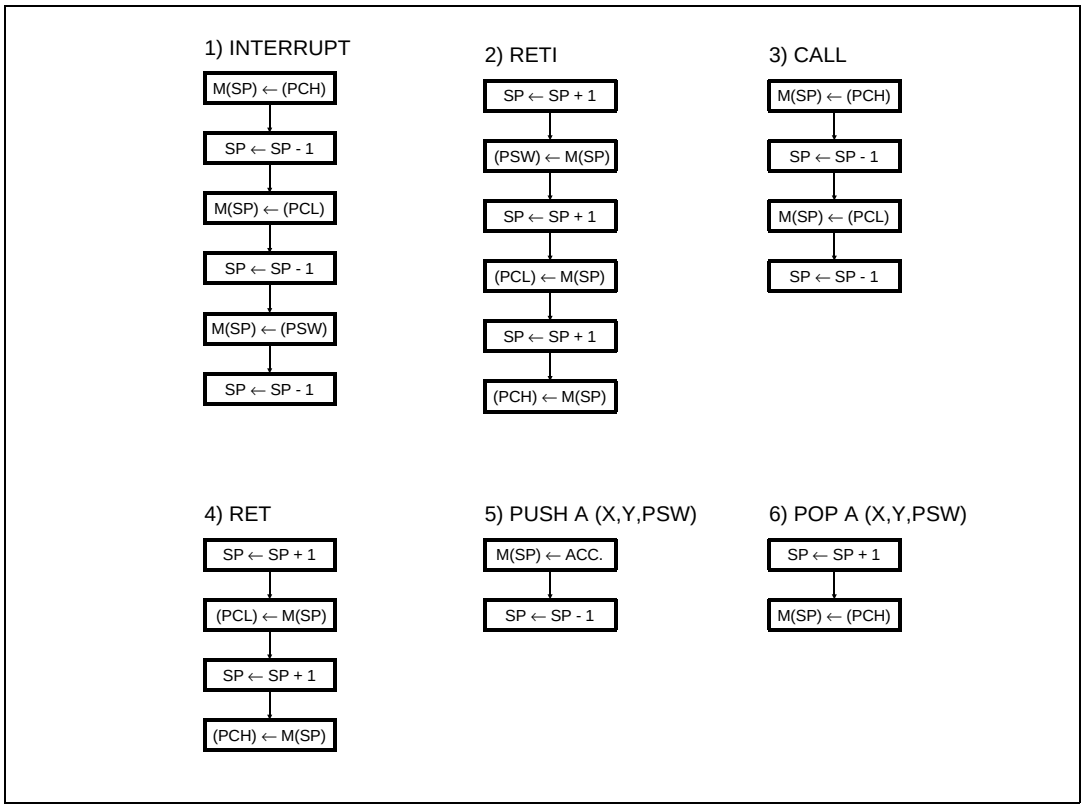


Figure 7. Stack Operation

Program Memory

A 16-bit program counter is capable of addressing up to 64K bytes, but this devices have 4K bytes (8K for GMS81608) program memory space only the physically implemented. Accessing a location above $FFFF_H$ will cause a wrap-around to 0000_H.

Figure 8, shows a map of the upper part of the Program Memory. After reset, the CPU begins execution from reset vector which is stored in address $FFFE_H$, $FFFF_H$.

As shown in Figure 8, each area is assigned a fixed location in Program Memory. Program Memory area contains the user program, Page Call (PCALL) area contains subroutine program, to reduce program byte length because of using by 2 bytes PCALL instead of 3 bytes CALL instruction. If it is frequently called, more useful to save program byte length.

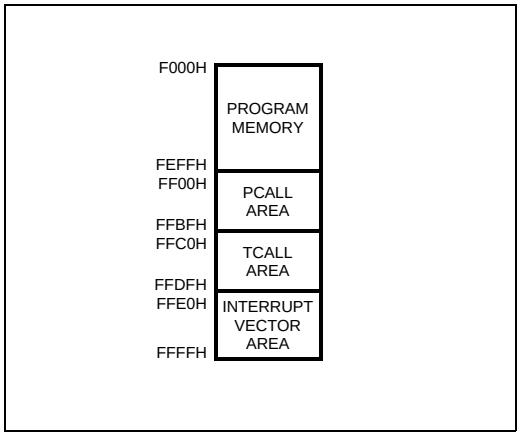


Figure 8. Program Memory

Table Call (TCALL) causes the CPU to jump to each TCALL address, where it commences execution of the service routine. The Table Call service locations are spaced at 2-byte interval : $FFC0_H$ for TCALL15, $FFC2_H$ for TCALL14, etc.

Address	TCALL Name
$FFC0_H$	TCALL15
$FFC2_H$	TCALL14
$FFC4_H$	TCALL13
$FFC6_H$	TCALL12
$FFC8_H$	TCALL11
$FFCA_H$	TCALL10
$FFCC_H$	TCALL9
$FFCE_H$	TCALL8
$FFD0_H$	TCALL7
$FFD2_H$	TCALL6
$FFD4_H$	TCALL5
$FFD6_H$	TCALL4
$FFD8_H$	TCALL3
$FFDA_H$	TCALL2
$FFDC_H$	TCALL1
$FFDE_H$	TCALL0/ BRK[1)]

1) The BRK software interrupt is using same address with TCALL0.

The interrupt causes the CPU to jump to specific location, where it commences execution of the service routine. The External interrupt 0, for example, is assigned to location $FFFA_H$. The interrupt service locations are spaced at 2-byte interval : $FFF8_H$ for External Interrupt 1, $FFFA_H$ for External Interrupt 0, etc.

Any area from $FF00_H$ to $FFFF_H$, if it not going to be used, its service location is available as general purpose Program Memory.

Address	Vector Name
FFE0H	-
FFE2H	-
FFE4H	-
FFE6H	Basic Interval Timer
FFE8H	-
FFEAH	Analog to Digital Converter
FFECH	-
FFEEH	-
FFF0H	Timer/ Counter 1
FFF2H	Timer/ Counter 0
FFF4H	-
FFF6H	-
FFF8H	External Interrupt 1
FFFAH	External Interrupt 0
FFFCH	-
FFFEH	RESET

Data Memory

Figure 9 shows the internal Data Memory space available. Data Memory are divided into three groups, a user RAM, control registers and Stack.

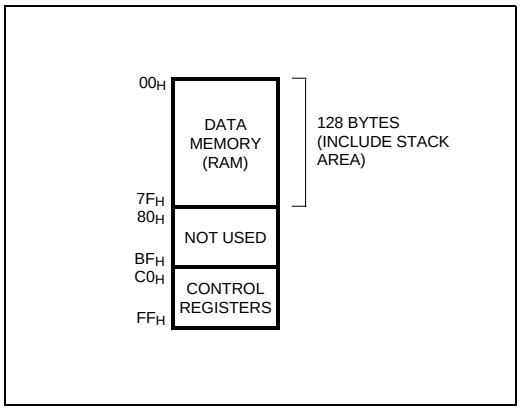


Figure 9. Data Memory

The stack pointer should be initialized within 00_H to $7F_H$ by software because of implemented area of internal data memory.

The control registers are used by the CPU and Peripheral functions for controlling the desired operation of the device.
Therefore these registers contain control and status bits for the interrupt system, the timer/ counters, analog to digital converters, I/O ports. The control registers are in address $C0_H$ to FF_H.

Note that unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

More detail informations of each register are explained in each peripheral sections.

Caution:
Write only registers can not be accessed by bit manipulation instruction.

Address	Symbol	R/W	Power-on Reset Value MSB LSB
C0H	R0	R/W	X
C1H	R0DD	W 1)	00000000
C8H	R4	R/W	X
C9H	R4DD	W 1)	00000000
CAH	R5	R/W	X
CBH	R5DD	W 1)	000-----
CCH	R6	R/W	X
CDH	R6DD	W 1)	0000----
D0H	PMR4	W 1)	-0-0--00
D1H	PMR5	W 1)	--0-----
D3H 2)	BITR	R	00000000
D3H 2)	CKCTLR	W 1)	---10111
E2H	TM0	R/W	00000000
E4H	☞ Note 3	R/W	X
E5H	☞ Note 3	R/W	X
E8H	ADCM	R/W 4)	--000001
E9H	ADR	R	X
ECH	BUR	W 1)	X
F4H	IENL	R/W	0-0-----
F5H	IRQL	R/W	0-0-----
F6H	IENH	R/W	00--00--
F7H	IRQH	R/W	00--00--
F8H	IEDS	W 1)	00000000

Legend - = Unimplemented locations.
X= Undefined value.

NOTES:
1) The all write only registers can not be accessed by bit manipulation instruction.
2) The register BITR and CKCTLR are located at same address. Address D3H is read as BITR, as written to CKCTLR.
3) Several names are given at same address. Refer to below table.

Address	When read		When write
	Timer mode	Capture Mode	
E4H	T0	CDR0	TDR0
E5H	T1	CDR1	TDR1

4) Only bit 0 of ADCM can be read.

Control Registers for the GMS81504

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$C0_H$	R0	R0 port data register							
$C1_H$	R0DD	R0 port direction register							
$C8_H$	R4	R4 port data register							
$C9_H$	R4DD	R4 port direction register							
CA_H	R5	R5 port data register							
CB_H	R5DD	R5 port direction register							
CC_H	R6	R6 port data register							
CD_H	R6DD	R6 port direction register							
$D0_H$	PMR4	-	T1S	-	EC0S	-	-	INT1S	INT0S
$D1_H$	PMR5	-	-	BUZS	-	-	-	-	-
$D3_H$[1)]	BITR	Basic Interval Timer data register							
$D3_H$[1)]	CKCTLR	-	-	-	ENPCK	BTCL	BTS2	BTS1	BTS0
$E2_H$	TM0	CAP0	T1ST	T1SL1	T1SL0	T0ST	T0CN	T0SL1	T0SL0
$E4_H$	T0/ TDR0/ CDR0	Timer 0 register/ Timer data register 0/ Capture data register 0							
$E5_H$	T1/ TDR1/ CDR1	Timer 1 register/ Timer data register 1/ Capture data register 1							
$E8_H$	ADCM	-	-	ADEN	ADS2	ADS1	ADS0	ADST	ADSF
$E9_H$	ADR	ADC result data register							
EC_H	BUR	BUCK1	BUCK0	BU5	BU4	BU3	BU2	BU1	BU0
$F4_H$	IENL	AE	-	BITE	-	-	-	-	-
$F5_H$	IRQL	AIF	-	BITIF	-	-	-	-	-
$F6_H$	IENH	INT0E	INT1E	-	-	T0E	T1E	-	-
$F7_H$	IRQH	INT0IF	INT1IF	-	-	T0IF	T1IF	-	-
$F8_H$	IEDS	-	-	-	-	IED1H	IED1L	IED0H	IED0L

Legend - = Unimplemented locations.

NOTES:
1) The register BITR and CKCTLR are located at same address. Address $D3_H$ is read as BITR, written to CKCTLR.

I/O PORTS

The GMS81504/08 have five ports, R0, R1, R4, R5, R6. These ports pins may be multiplexed with an alternate function for the peripheral features on the device. In general, when a initial reset state, all ports are used as a general purpose input port.

All pins have data direction registers which can configure these pins as output or input.
A "1" in the port direction register configures the corresponding port pin as output. Conversely, write "0" to the corresponding bit to specify as an input pin. For example, to use the even numbered bit of R1 as output ports and the odd numbered bits as input ports, write "55_H" to address $C1_H$ (R0 direction register) during initial setting as shown in Figure 10.

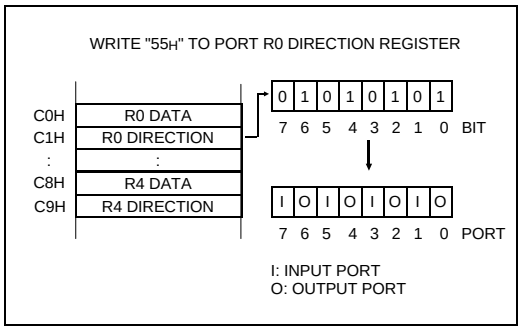
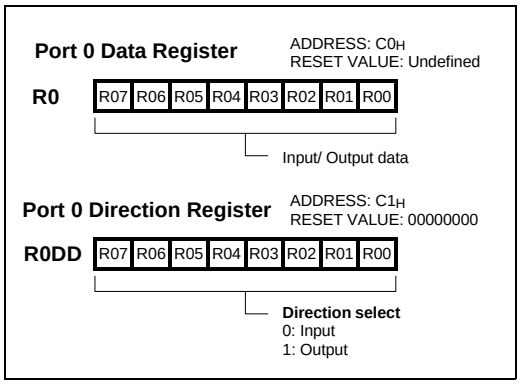


Figure 10. Example port I/O assignment

Reading data register reads the status of the pins whereas writing to it will write to the port latch.

R0 and R0DD registers: R0 is a 8-bit bidirectional I/O port (address $C0_H$). Each pin is individually configurable as input and output through the R0DD register (address $C1_H$).

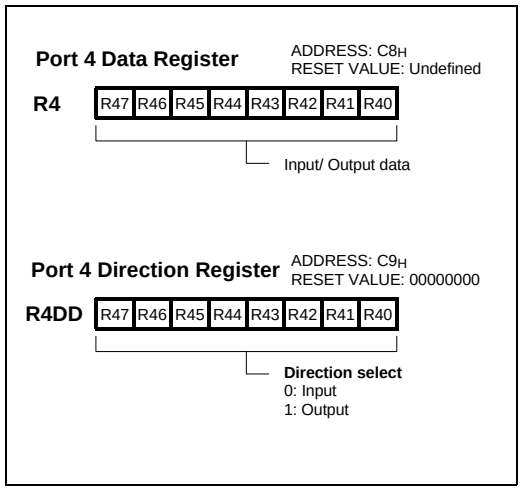


R4 and R4DD registers: R4 is an 8-bit bidirectional I/O port (address $C8_H$). Each pin is individually configurable as input and output through the R4DD register (address $C9_H$).

In addition, Port R4 is multiplexed with various special features. The control register PMR4 (address $D0_H$) controls to select alternate function. After reset, this value is "0", port may be used as general I/O ports. To select alternate function such as External interrupt or External counter or Timer clock out, write "1" to the corresponding bit of PMR4.

Port Pin	Alternate Function
R40	INT0 (External Interrupt 0)
R41	INT1 (External Interrupt 1)
R44	$\overline{EC0}$ (External Count Input to Timer/ Counter 0)
R46	T1O (Timer 1 Clock-Out)

Regardless of the direction register R4DD, PMR4 is selected to use as alternate functions, port pin can be used as a corresponding alternate features.



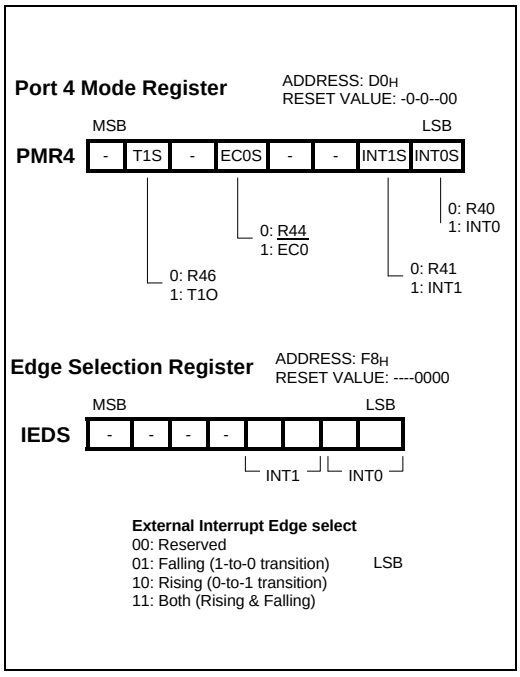
R5 and R5DD registers: R5 is a 3-bit bidirectional I/O port (address CA_H). R55, R56 and R57 only are physically implemented on this device.
R56, R57 have internal pullups which is activated on input but deactivated on output. As input, these pins that are externally pull low will source current (I_{P2} on the DC characteristics) because of the internal pullups.

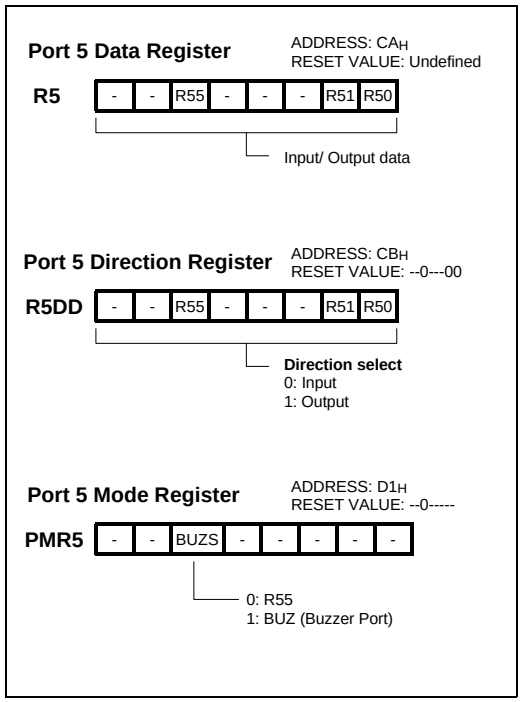
Caution:
Pins R56, R57 are served on 30SDIP package only, but not served on 28SOP . Refer to Pin assignment.

Each pin is individually configurable as input and output through the R5DD register (address CB_H).

Port Pin	Alternate Function
R55	BUZ (Square-wave output for Buzzer driving)

The control register PMR5 (address $D1_H$) controls the selection alternate function. After reset, this value is "0", port may be used as general I/O ports. To use buzzer function, write "1" to the PMR5.

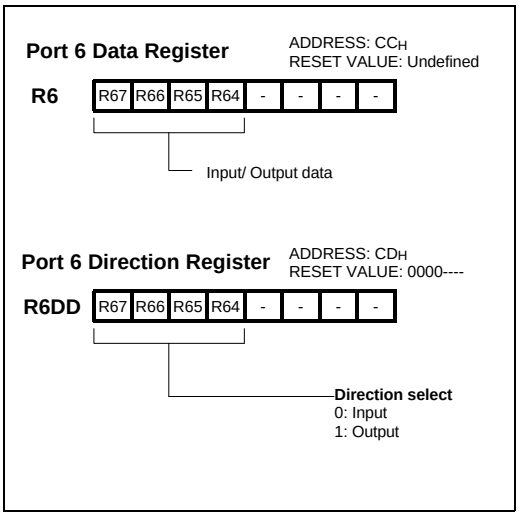




R6 and R6DD registers: R6 is a 4-bit port (address CC_H). Pins R64~R67 are individually configurable as input and output through the R6DD register (address CD_H).

Port Pin	Alternate Function
R64	AN4 (ADC input 4)
R65	AN5 (ADC input 5)
R66	AN6 (ADC input 6)
R67	AN7 (ADC input 7)

R6DD (address CD_H) controls the direction of the R6 pins, even when they are being used as analog inputs. The user must make sure to keep the pins configured as inputs when using them as analog inputs.



BASIC INTERVAL TIMER

The GMS81504 has one 8-bit Basic Interval Timer that is free-run, can not stop. Block diagram is shown in Figure 11.
The 8-bit Basic interval timer register (BITR) is incremented every internal count pulse which is divided by prescaler. Since prescaler has divided ratio by 16 to 2048, the count rate is 1/16 to 1/2048 of the oscillator frequency. As the count overflows from FF_H to 00_H, this overflow causes to generate the Basic interval timer interrupt. The BITR is interrupt request flag of Basic interval timer.

Caution:
All control bits of Basic interval timer are in CKCTLR register which is located at same address with BITR (address $D3_H$). Address $D3_H$ is read as BITR, written to CKCTLR.

When write "1" to bit BTCL of CKCTLR, data register is cleared to "0" and restart to count-up. It becomes "0" after one machine cycle by hardware.

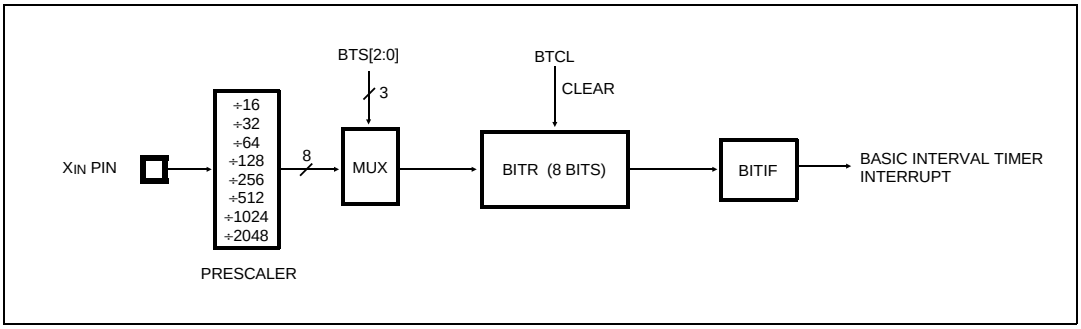


Figure 11. Block Diagram of The Basic Interval Timer

CKCTLR

-	-	-	ENPCK	BTCL	BTS2	BTS1	BTS0

ADDRESS: $D3_H$
RESET VALUE: ---10111

Symbol	Position	Name and Significance
ENPCK	CKCTLR.4	Enable Peripheral clock. 1: Supply clock to every peripherals 0: Stop clock
BTCL	CKCTLR.3	BTCL is set to "1", BITR is cleared. BTCL becomes "0" automatically after one machine cycle, and starts counting.

BASIC INTERVAL TIMER CLOCK SELECTION

BTS2	BTS1	BTS0	Prescale value
0	0	0	16
0	0	1	32
0	1	0	64
0	1	1	128
1	0	0	256
1	0	1	512
1	1	0	1024
1	1	1	2048

Figure 12. CKCTLR: Control Clock Register

TIMER/COUNTER

The GMS81504 has two Timer/Counter registers. Each module can generate an interrupt to indicate that an event has occurred (i.e. timer match).

Timer 0 and Timer 1 are can be used either the two 8-bit Timer/Counter or one 16-bit Timer/Counter to combine them.

In the "timer" function, the register is incremented every internal clock input. Thus, one can think of it as counting internal clock input. Since a least clock consists of 4 and most clock consists of 64 oscillator periods, the count rate is 1/4 to 1/64 of the oscillator frequency.

In the "counter" function, the register is incremented in response to a 1-to-0 (falling edge) transition at its corresponding external input pin, $\overline{EC0}$.

In addition the "capture" function, the register is incremented in response external or internal clock sources same with timer or counter function. When external clock edge input, the count register is captured into Timer data register correspondingly.

It has four operating modes: "8-bit timer/counter", "16-bit timer/counter", "8-bit capture", "16-bit capture" which are selected by bit in Timer mode register TM0 as shown in right Table.

TM0 FOR TIMER 0, TIMER 1

CAP0	T1SL1	T1SL0	Timer 0	Timer 1
0	0	0	16-bit Timer/Counter	
1	0	0	16-bit Capture	
0	X	X	8-bit Timer	8-bit Timer
1	X	X	8-bit Capture	8-bit Timer

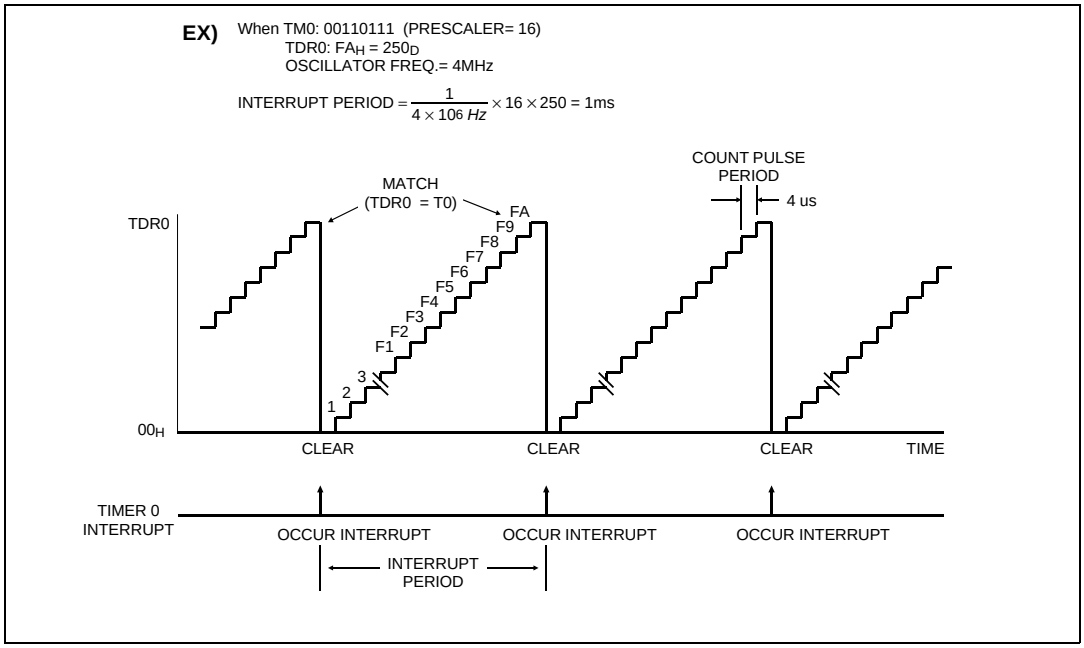


Figure 13. Timer Count Operation Example

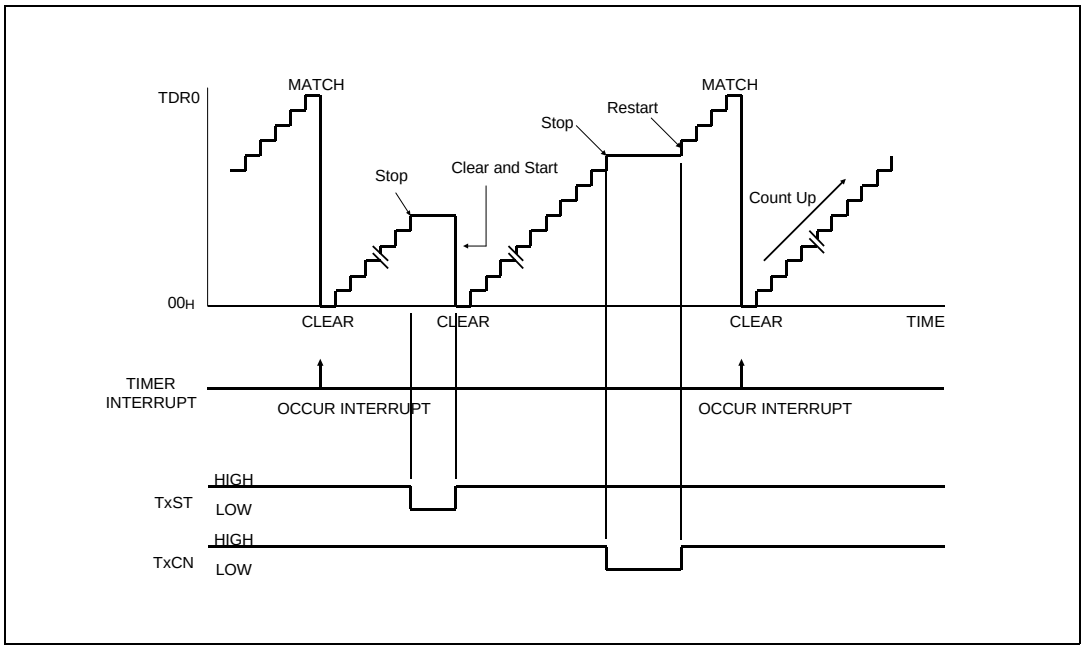


Figure 14. Timer Count Operation

8-bit Timer/Counter Mode

The GMS81504 has two 8-bit Timer/Counters, Timer 0, Timer 1. The Timer 0, Timer 1 only as shown in Figure 15.

The "timer" or "counter" function is selected by control registers TM0 as shown in Figure 17. To use as an 8-bit timer/counter mode, bit CAP0 of TM0 should be cleared to "0" and bits T1SL1, T1SL0 of TM0 should not set to zero (Figure 15).
These timers have each 8-bit count register and data register. The count register is incremented by every internal or external clock input. The internal clock has a prescaler divide ratio option of 4, 16, 64 (selected by control bits T1SL1, T1SL0 of register TM0).

In the Timer 0, timer register T0 increments from 00_H until it matches TDR0 and then reset to 00_H. The match output of Timer 0 generates Timer 0 interrupt (latched in T0IF bit)

As TDRx and Tx register are in same address, when reading it as a Tx, written to TDRx.

Caution:
The contents of Timer data register TDRx should be initialized 1_H~FF_H except 0_H, because it is undefined after reset.

In counter function, the counter is incremented every 1-to-0 (falling edge) transition of $\overline{EC0}$ pin. In order to use counter function, the bit EC0S of the Port mode register PMR4 are set to "1". The Timer 0 can be used as a counter by pin $\overline{EC0}$ input, but Timer 1 can not.

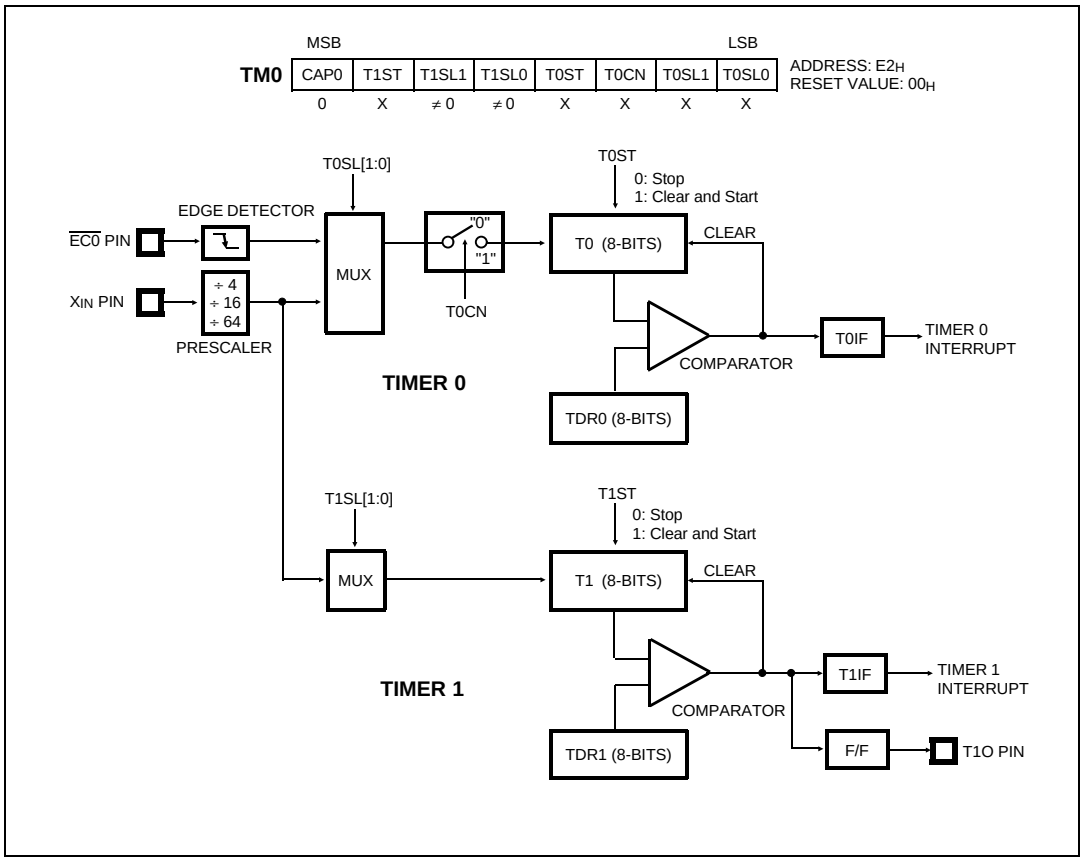


Figure 15. 8-bit Timer/Counter Mode

To pulse out, the timer match can goes to port pin as shown in Figure 15. Thus, pulse out is generated by the timer match. These operation is implemented to pin T1O. The pin T1O is output from Timer 1. Output frequency is calculated as following equation.

$$f_{T1O}\,(Hz) = \frac{f_{XIN}}{2 \cdot Prescaler \cdot TDR}$$

f_{T1O}: Pin T1O output pulse frequency
f_{XIN}: Oscillator frequency
Prescaler: Refer to bit T1SL1,T1SL0 of TM0 at Figure 17.

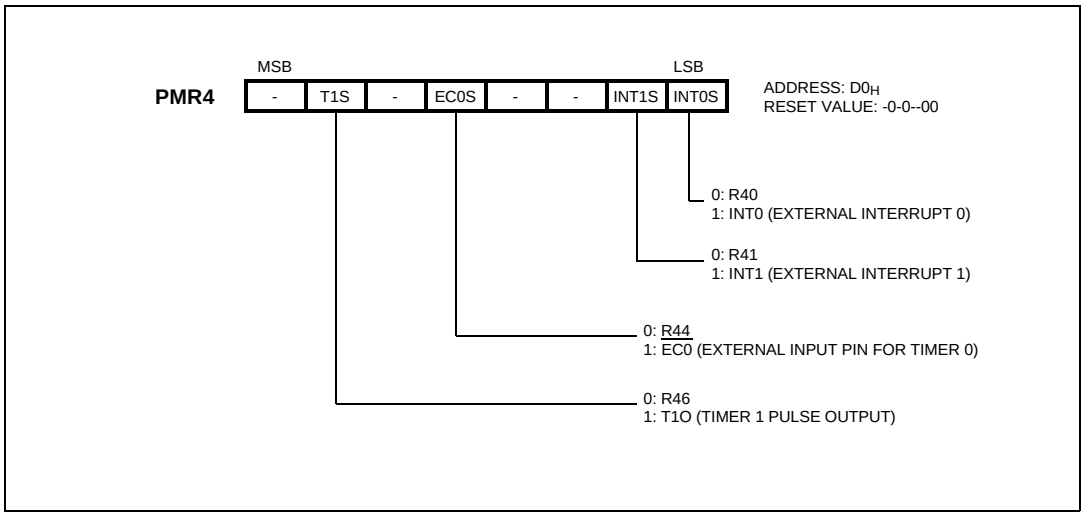
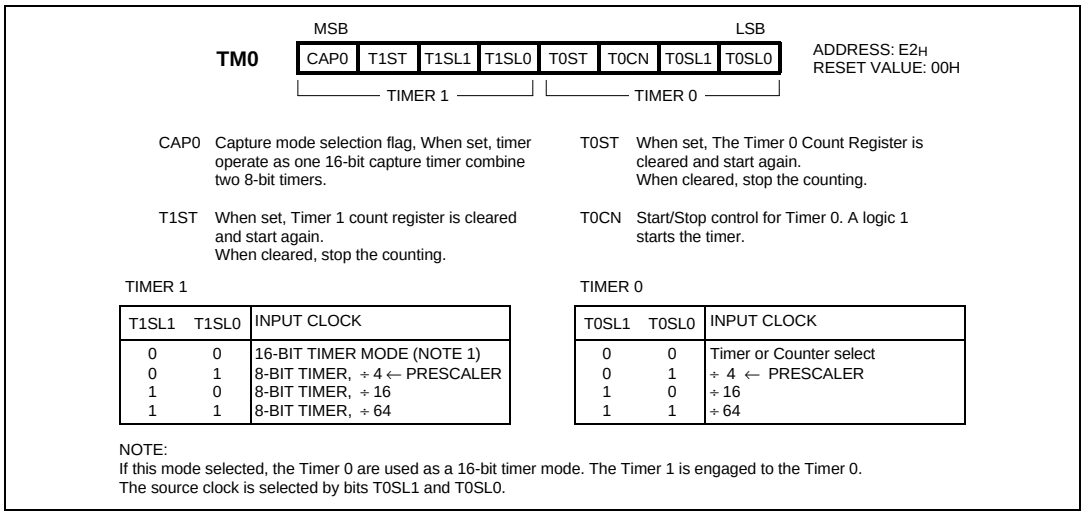


Figure 16. PMR4: R4 Port Mode Register



TIMER 1

T1SL1	T1SL0	INPUT CLOCK
0	0	16-BIT TIMER MODE (NOTE 1)
0	1	8-BIT TIMER, ÷ 4 ← PRESCALER
1	0	8-BIT TIMER, ÷ 16
1	1	8-BIT TIMER, ÷ 64

TIMER 0

T0SL1	T0SL0	INPUT CLOCK
0	0	Timer or Counter select
0	1	÷ 4 ← PRESCALER
1	0	÷ 16
1	1	÷ 64

NOTE:
If this mode selected, the Timer 0 are used as a 16-bit timer mode. The Timer 1 is engaged to the Timer 0. The source clock is selected by bits T0SL1 and T0SL0.

Figure 17. TM0: Timer 0, Timer 1 Mode Register

16-bit Timer/Counter Mode

The Timer register is being run with all 16 bits. A 16-bit timer/counter register T0, T1 are incremented from 0000_H until it matches TDR0, TDR1 and then resets to 0000_H. The match output generates Timer 0 interrupt.

The clock source of the Timer 0 is selected either internal or external clock by bit T0SL1, T0SL0.

Bit T1ST is not effect in this 16-bit mode.

Bit T0SL1 and T0SL0 select the clock source among three prescaler divide ratio and external $\overline{EC0}$ clock.

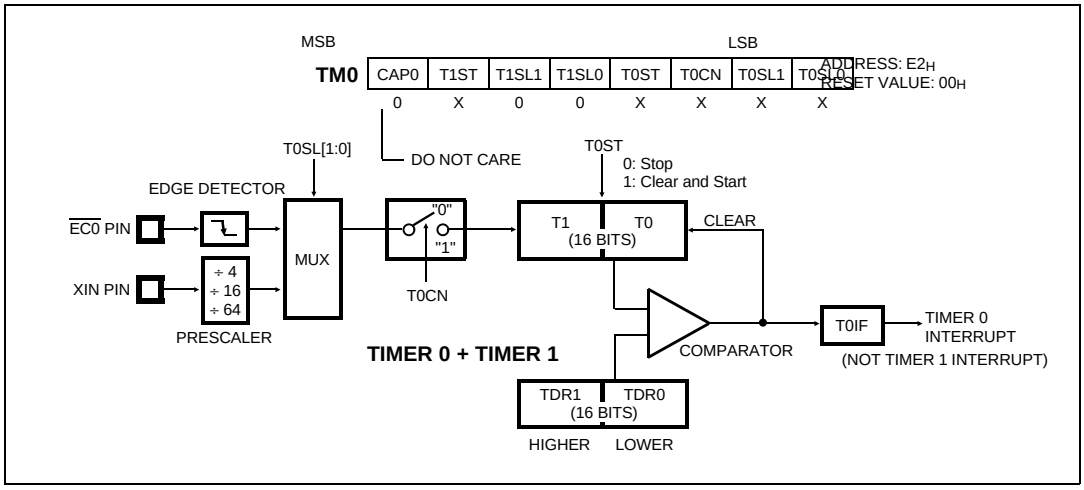


Figure 18. 16-bit Timer/Counter Mode

8-bit Capture Mode

The Timer 0 capture mode is set by bit CAP0 of timer mode register TM0 as shown in Figure 19. In this mode, Timer 1 still operates as an 8-bit timer/counter.

In 8-bit capture mode, Timer 1 can not be used as capture mode.

The Timer/Counter register is incremented in response internal or external input. This counting function is same with normal timer mode, but Timer interrupt is not generated. Timer/Counter still does the above, but with the added feature that a edge transition at external input INT0 pin causes the current value in the Timer 0 register T0, to be captured into registers CDR0, respectively. After captured, Timer 0 register T0 is cleared and restarts by hardware.

Caution:
The CDRx and TDRx are in same address.
In the capture mode, reading operation is read the CDRx, not TDRx because path is opened to the CDRx.

It has three transition modes: "falling edge", "rising edge", "both edge" which are selected by interrupt edge selection register IEDS (Refer to External interrupt section). In addition, the transition at INT0 pin generates an interrupt signal.

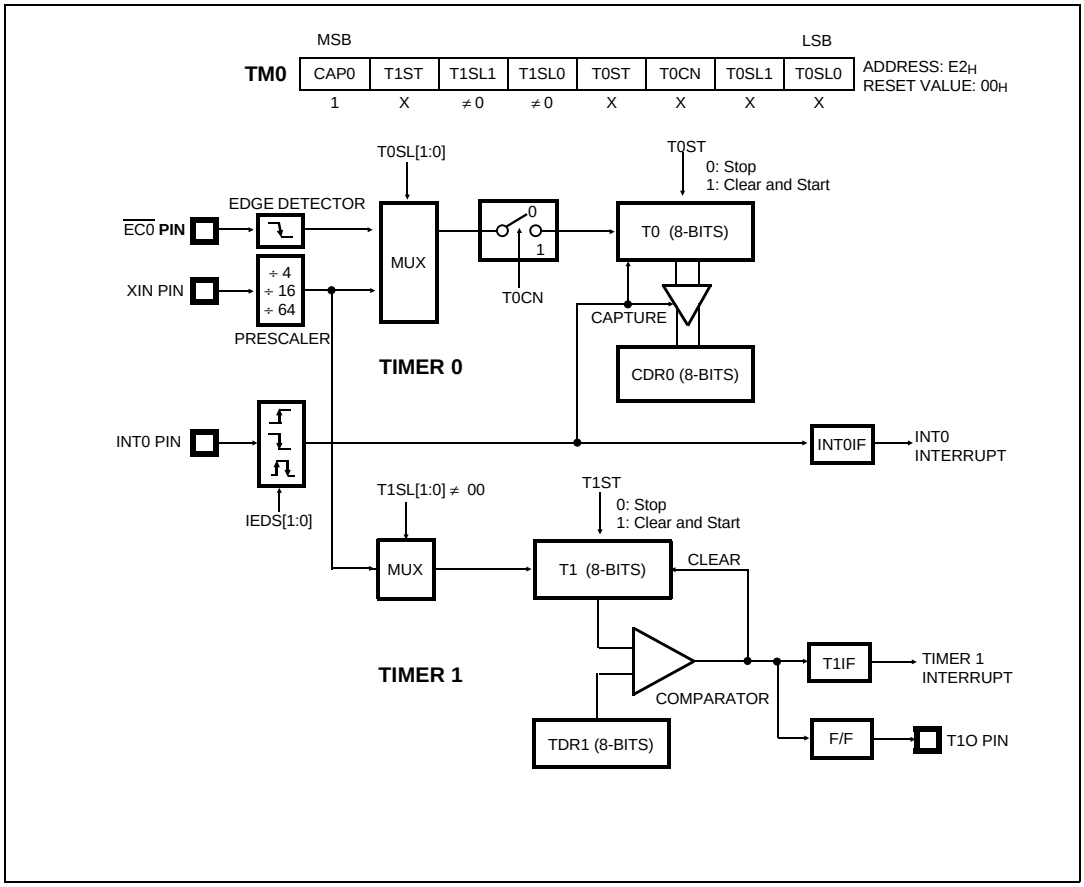


Figure 19. 8-bit Capture Mode

16-bit Capture Mode

16-bit capture mode is the same as 8-bit capture, except that the Timer register is being run will 16 bits.

Bit T1ST is not effect in this 16-bit mode.

Bit T0SL1 and T0SL0 select the clock source among three prescaler divide ratio and external $\overline{EC0}$ clock.

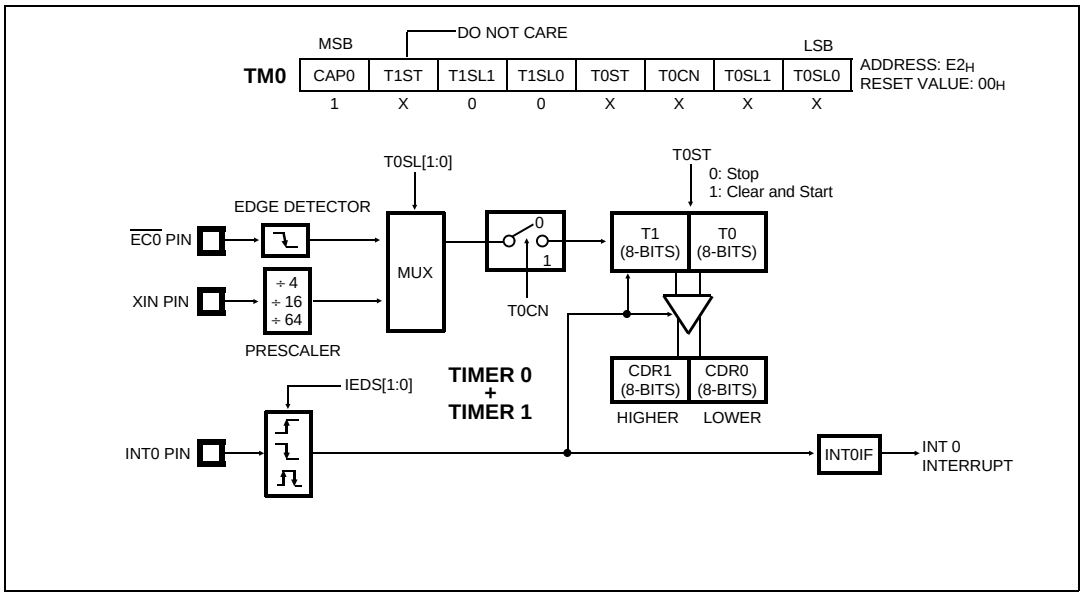


Figure 20. 16-bit Capture Mode

ANALOG TO DIGITAL CONVERTER

The analog-to-digital converter (A/D) allows conversion of an analog input signal to a corresponding 8-bit digital value. The A/D module has eight analog inputs, which are multiplexed into one sample and hold. The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog supply voltage is connected to AV_{DD} of ladder resistance of A/D module.

The A/D module has two registers which are the control register ADCM and A/D result register ADR. The register ADCM, shown in Figure 22, controls the operation of the A/D converter module. The port pins can be configured as analog inputs or digital I/O. To use analog inputs, I/O is selected input mode by R6DD direction register.

How to Use A/D Converter

The processing of conversion is start when the start bit ADST is set to "1". After one cycle, it is cleared by hardware. The register ADR contains the results of the A/D conversion. When the conversion is completed, the result is loaded into the ADR, the A/D conversion status bit ADSF is set to "1", and the A/D interrupt flag AIF is set. The block diagram of the A/D module is shown in Figure 21. The A/D status bit ADSF is set automatically when A/D conversion is completed, cleared when A/D conversion is in process. The conversion time takes maximum 40 uS (at f_{XIN}=4 MHz).

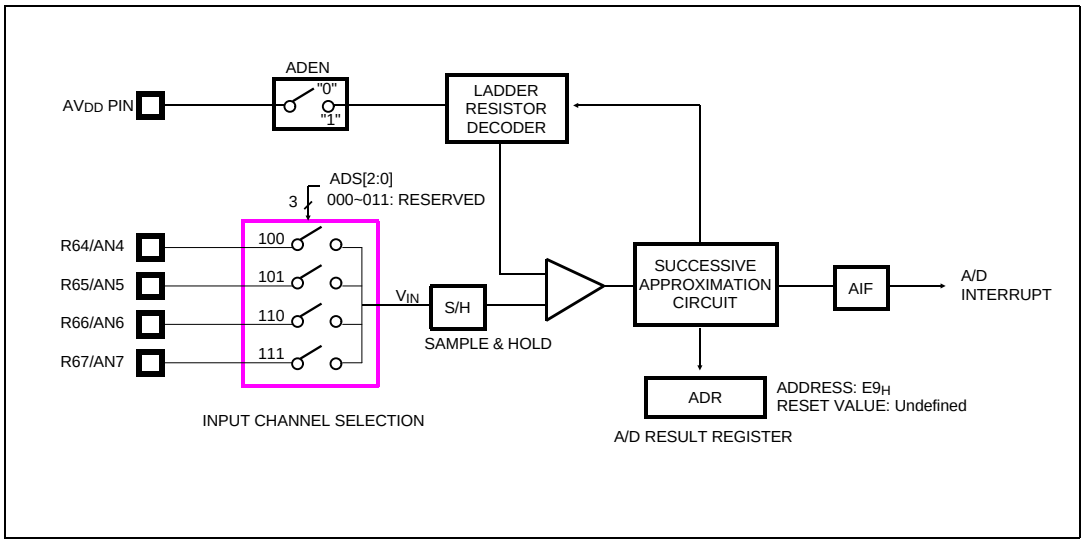


Figure 21. A/D Block Diagram

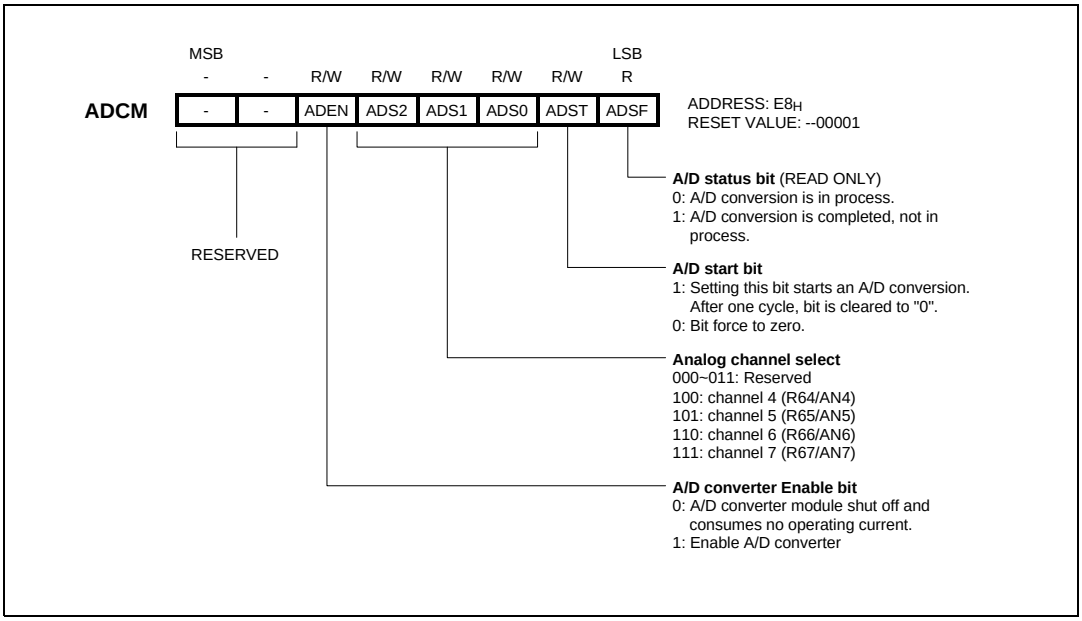


Figure 22. ADCM: A/D Converter Control Register

BUZZER FUNCTION

The buzzer driver consists of 6-bit binary counter, the buzzer register BUR and the clock selector. It generates square-wave which is very wide range frequency (250 Hz~125 kHz at f_{XIN}=4 MHz) by user programmable counter.

Pin R55 is assigned for output port of Buzzer driver by setting the bit 5 of PMR5 (address $D1_H$) to "1". At this time, the pin R55 must be defined as output mode (the bit 5 of R5DD=1). In the emulator, even if pin R55 is defined as input, buzzer output is available.

The bit 0 to 5 of BUR determines output frequency for buzzer sound.
Frequency calculation is following below.

$$f_{BUZ}(Hz) = \frac{f_{XIN}}{2 \cdot Prescaler\ \ ratio \cdot BUR\,value}$$

f_{BUZ}: Buzzer frequency
f_{XIN}: Oscillator frequency
Prescaler: Prescaler divide ratio by BUCK1, BUCK0
BUR:Lower 6-bit of BUR. Buzzer period data value

The bits BUCK1, BUCK0 of BUR selects the source clock from prescaler output.

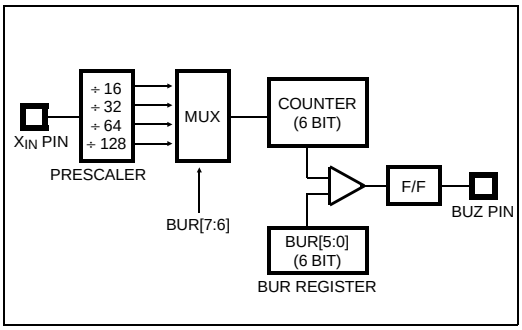


Figure 23. Buzzer Driver

The 6-bit buzzer counter is cleared and start the counting by writing signal to the register BUR. It is increment from 00_H until it matches 6-bit register BUR.

Caution:
The register BUR contains undefined value after reset. It must be initialized with 1_H~$3F_H$ (none 0_H).

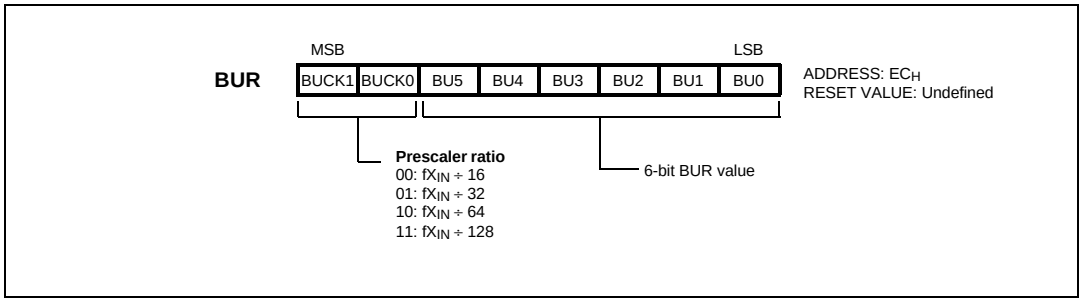


Figure 24. BUR: Buzzer Period Data Register

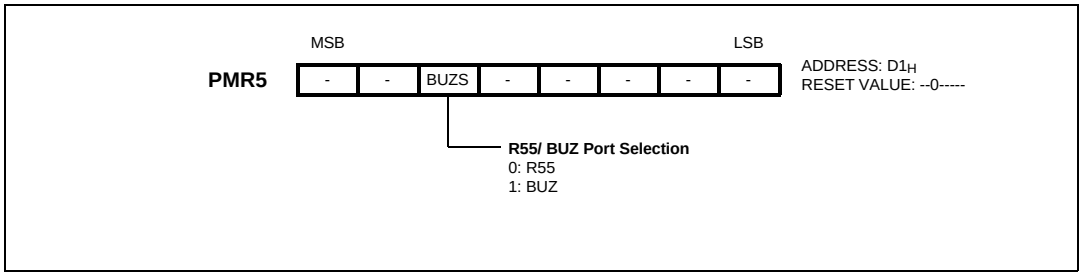


Figure 25. PMR5: Port 5 Mode Register

INTERRUPTS

The GMS81504 interrupt circuits consist of Interrupt enable register (IENH, IENL), Interrupt request flags of IRQH, IRQL, priority circuit and Master enable flag(I flag of PSW). The configuration of interrupt circuit is shown in Figure 1-26.

12 interrupt sources are provided including the Reset.

Interrupt source	Symbol	Priority
Hardware RESET	RESET	1
External Interrupt 0	INT0IF	2
External Interrupt 1	INT1IF	3
Timer/Counter 0	T0IF	4
Timer/Counter 1	T1IF	5
AD Converter	AIF	6
Basic interval timer	BITIF	7

*Vector addresses are shown in Program Memory section.

The External Interrupts INT0, INT1 can each be transition-activated, depending on interrupt edge selection register.

The Timer 0, Timer 1 Interrupts are generated by T0IF, T1IF, which are set by a match in their respective timer/counter register.

The AD converter Interrupt is generated by AIF which is set by finishing the analog to digital conversion.

The Basic Interval Timer Interrupt is generated by BITIF which are set by a overflow in the timer/counter register.

The interrupts are controlled by the interrupt master enable flag I-flag (bit 2 of PSW), the interrupt enable register (IENH, IENL) and the interrupt request flags (in IRQH, IRQL) except Power-on reset and software BRK interrupt.

Interrupt enable registers are shown in Figure 27. These registers are composed of interrupt enable flags of each interrupt source, these flags determines whether an interrupt will be accepted or not. When enable flag is "0", a corresponding interrupt source is prohibited. Note that PSW contains also a master enable bit, I-flag, which disables all interrupts at once.

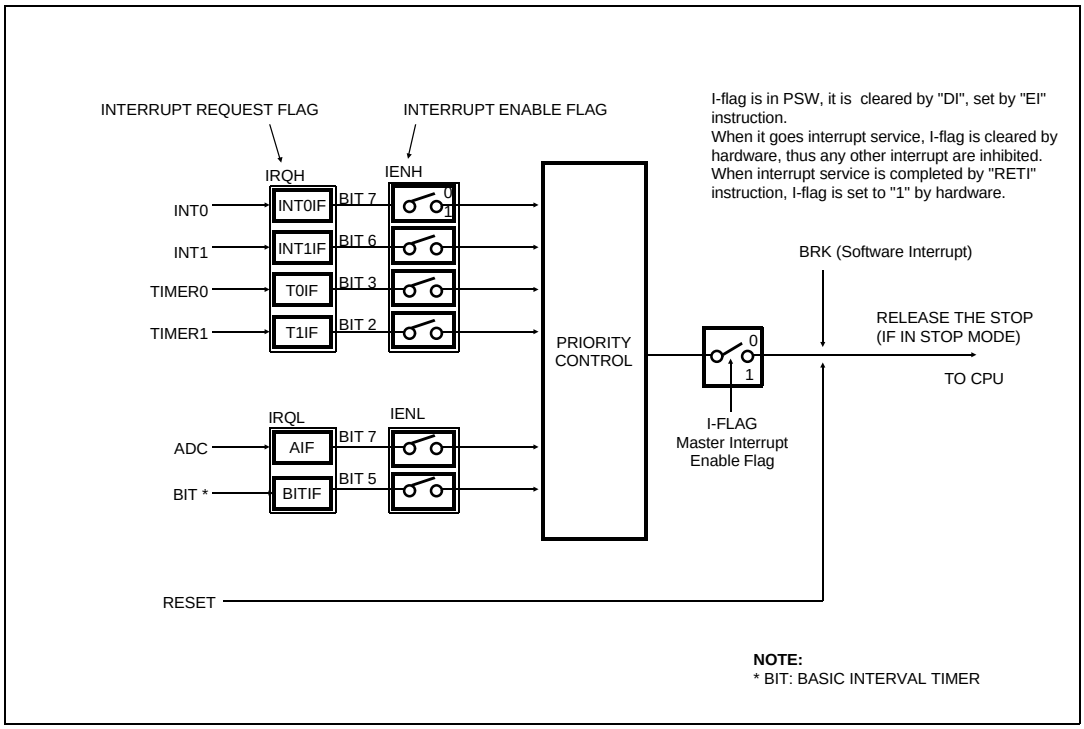


Figure 1-26. Block Diagram of Interrupt Function

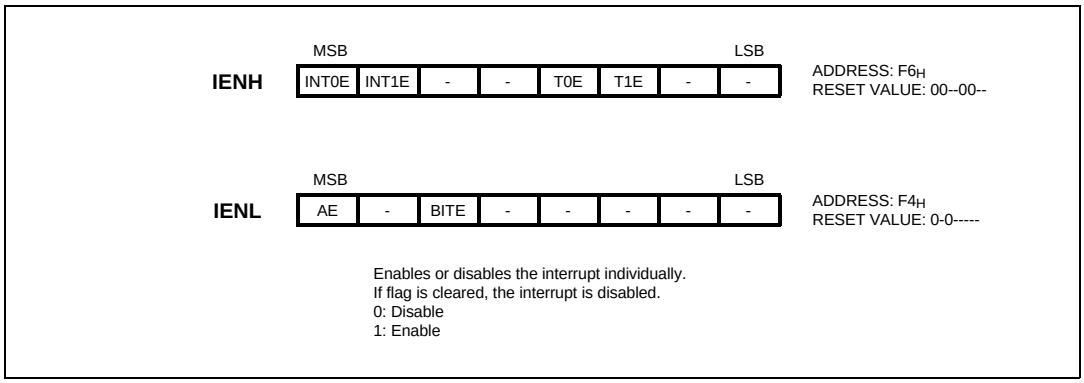


Figure 27. IENH, IENL: Interrupt Enable Registers

When an interrupt is responded to, the I-flag is cleared to disable any further interrupt, the return address is pushed into the stack and the PC is vectored to. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits.

The interrupt flag bit(s) must be cleared in software before reenabling interrupts to avoid recursive interrupts. The Interrupt Request flags are able to be read and write.

External Interrupt

External interrupt on INT0, INT1 pins are edge triggered depending on the edge selection register IEDS.

The edge detection of external interrupt has three transition activated mode: rising edge, falling edge, both edge. INT0, INT1 are multiplexed with general I/O ports (R40, R41). To use external interrupt pin, set bit 0 to bit 3 of the port mode register PMR4.

The PMR4 and IEDS registers are shown in Figure 30.

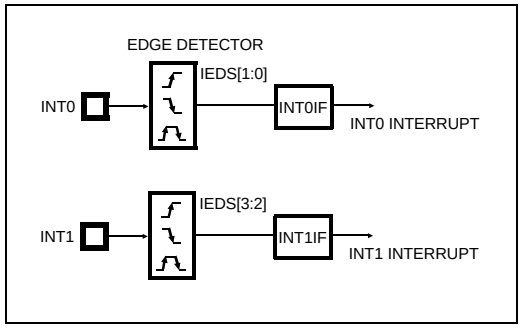


Figure 28. External Interrupt

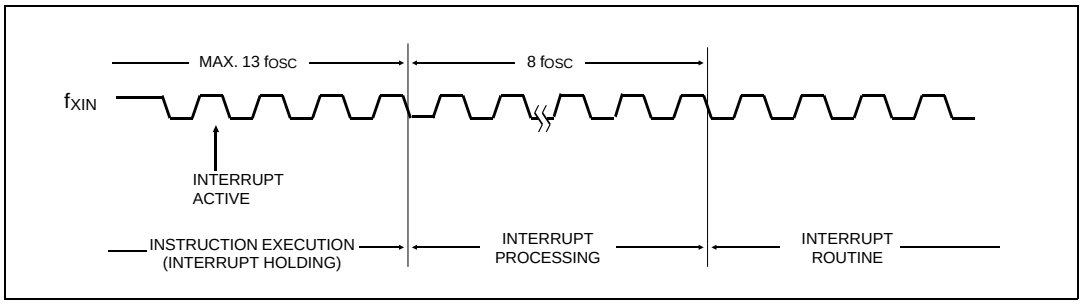


Figure 29. INT Pin Interrupt Timing

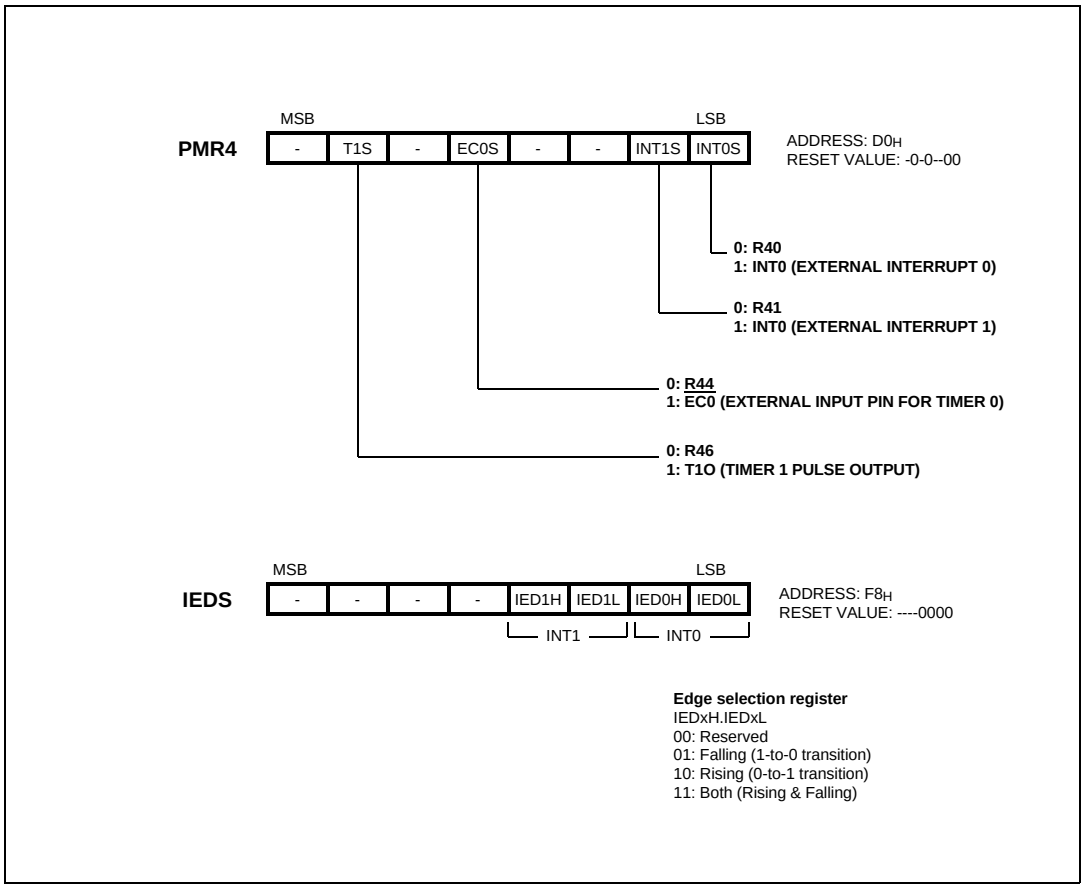


Figure 30. PMR4 and IEDS Registers

BRK Interrupt

Software interrupt can be invoked by BRK instruction, which is the lowest priority order.

Interrupt vector address of BRK is shared with the vector of TCALL0 (Refer to Program Memory Section). When BRK interrupt is generated, B-flag of PSW is set to distinguish BRK from TCALL0.

Each processing step is determined by B-flag as shown below.

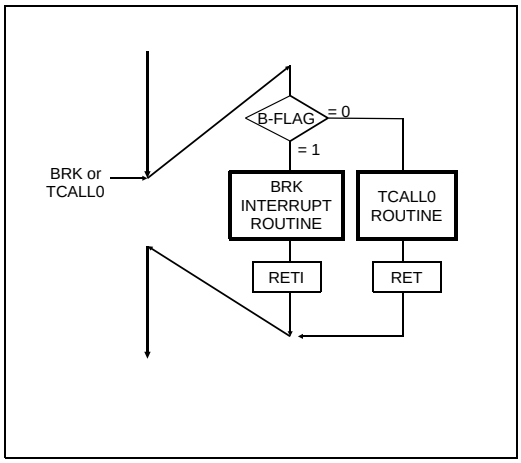


Figure 31. Execution of BRK/ TCALL0

Multiple Interrupt

If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If requests of the same priority level are received simultaneously, an internal polling sequence determines by hardware which request is serviced. Hardware interrupt priority is shown in Page36.

However, multiple processing through software for special features is possible. Generally when an interrupt is accepted, the I-flag is cleared to disable any further interrupt. But as user set I-flag in interrupt routine, some further interrupt can be serviced even if certain interrupt is in progress.

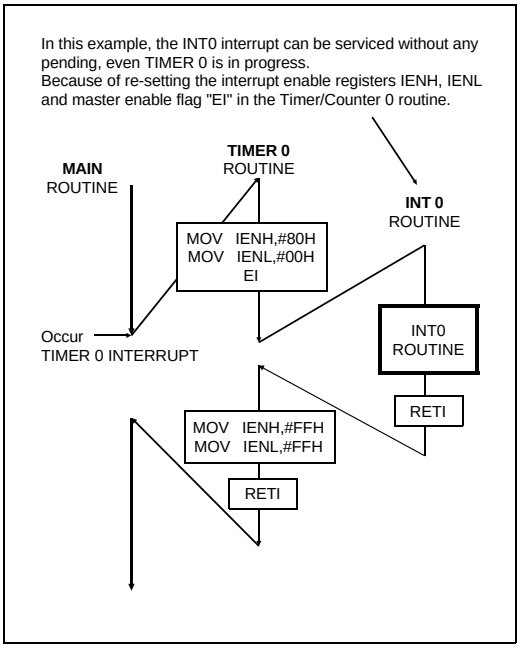


Figure 32. Execution of Multi-Interrupt

STOP MODE

For applications where power consumption is a critical factor, device provides reduced power of STOP.

An instruction that STOP causes that to be the last instruction executed before going into the Stop mode. In the Stop mode, the on-chip oscillator is stopped. With the clock frozen, all functions are stopped, but the on-chip RAM and Control registers are held. The port pins out the values held by their respective port data register Rx, port direction register RxDD. The status of peripherals during Stop mode is shown below.

Peripheral	Status
RAM	Retain
Control registers	Retain
I/O	Retain
Oscillation	Stop
X_{IN}	Low
X_{OUT}	High

In the Stop mode of operation, V_{DD} can be reduced to minimize power consumption. Care must be taken, however, to ensure that V_{DD} is not reduced before the Stop mode is invoked, and that V_{DD} is restored to its normal operating level, before the Stop mode is terminated. The reset should not be activated before V_{DD} is restored to its normal operating level, and must be held active long enough to allow the oscillator to restart and stabilize (minimum 20 msec).

Caution:
The NOP instruction have to be written more than two to next line of the STOP instruction.
Ex)
STOP
NOP
NOP

Release Stop Mode

The exit from Stop mode is hardware reset or external interrupt. Reset redefines all the Control registers but does not change the on-chip RAM. External interrupts allow both on-chip RAM and Control registers to retain their values.

If I-flag = 1, the normal interrupt response takes place. If I-flag = 0, the chip will resume execution starting with the instruction following the STOP instruction. It will not vector to interrupt service routine.

When exit from Stop mode by external interrupt from Stop mode, enough oscillation stabilization time is required to normal operation. Figure 33 shows the timing diagram. When release the Stop mode, the

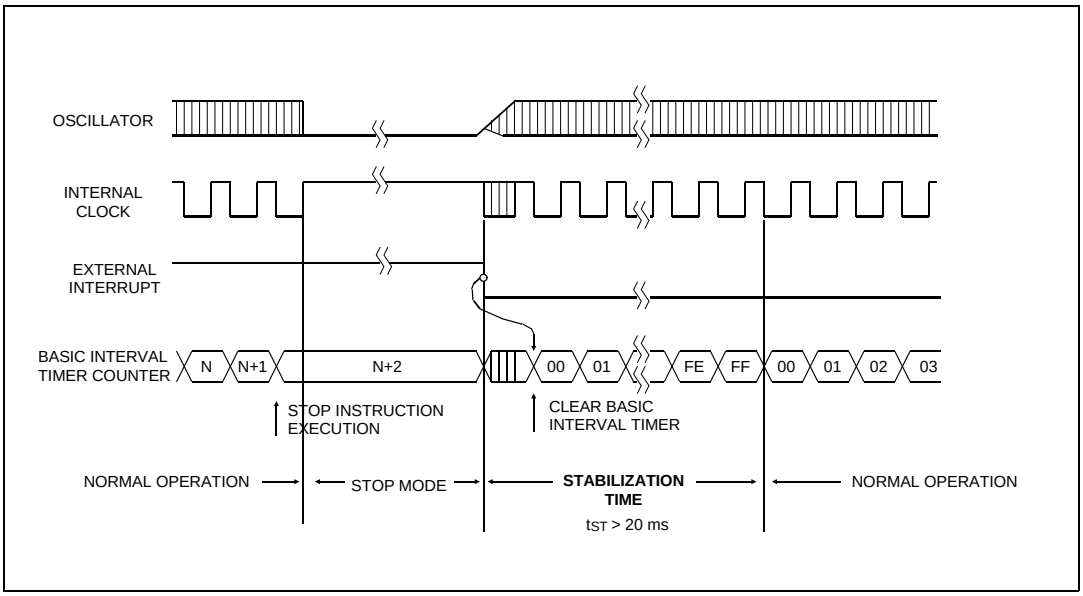


Figure 33. Timing of Stop Release by External Interrupt

Wake-up and Reset Function Table

Event	Chip Status before event	Chip function after event	
		PC	Oscillator Circuit
RESET	Do not care	Vector	on
STOP instruction	Normal operation	N+1	off
External Interrupt	Normal operation	Vector	on
External Interrupt Wake-up	Stop, I-flag = 1 Stop, I-flag = 0	Vector N+1	on on

PC: Program Counter contents after the event.
N: Address of STOP instruction.

Basic interval timer is activated on wake-up. It is incremented from 00_H until FF_H then 00_H. The count overflow is set to start normal operation. Therefore, before STOP instruction, user must be set its relevant prescaler divide ratio to have long enough time. This guarantees that crystal oscillator has started and stabilized.

By reset, exit from Stop mode is shown in Figure 34.

Minimizing Current Consumption in Stop Mode

The Stop mode is designed to reduce power consumption. To minimize current drawn during Stop mode, the user should turn-off output drivers that are sourcing or sinking current, if it is practical. Weak pull-ups on port pins should be turned off, if possible. All inputs should be either as V_{SS} or at V_{DD} (or as close to rail as possible). An intermediate voltage on an input pin causes the input buffer to draw a significant amount of current.

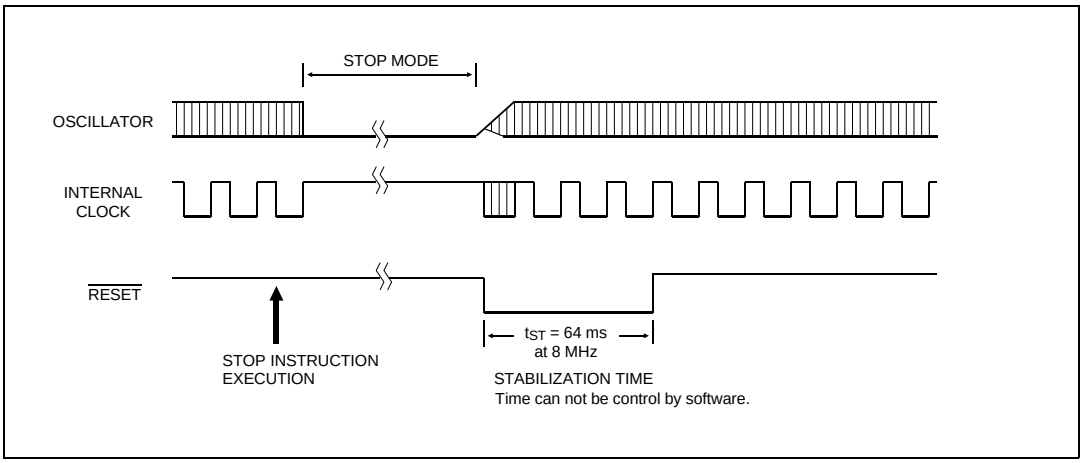


Figure 34. Timing of Stop Mode Release by Reset

RESET

The reset input is the RESET pin, which is the input to a Schmitt Trigger. A reset in accomplished by holding the RESET pin low for at least 8 oscillator periods, while the oscillator running. After reset, 64ms (at 8 MHz) plus 7 oscillator periods are required to start execution as shown in Figure 36.

Internal RAM is not affected by reset. When V_{DD} is turned on, the RAM content is indeterminate. Initial state of each register is as follow. Therefore, this RAM should be initialized before reading or testing it.

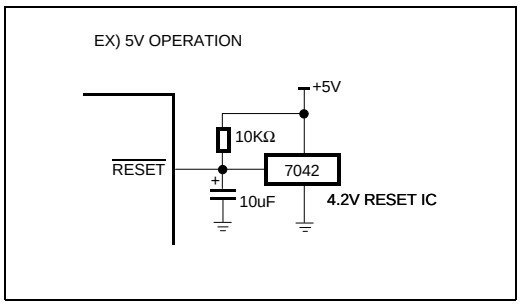


Figure 35. Example of Reset circuit

Register	Content
A	X
X	X
Y	X
PSW	00H
PC	X
SP	X
R0	X
R0DD	00000000
R4	X
R4DD	00000000
R5	X
R5DD	000-----
R6	X
R6DD	0000----
PMR4	-0-0--00
PMR5	--0-----
BITR	00H
CKCTLR	--010111
TM0	00H
TDR0/ T0/ CDR0	X
TDR1/ T1/ CDR1	X
ADCM	--000001
ADR	X
BUR	X
IENH	00--00--
IENL	0-0-----
IRQH	00--00--
IRQL	0-0-----
IEDS	-----000

- = unimplemented bit
X= unknown

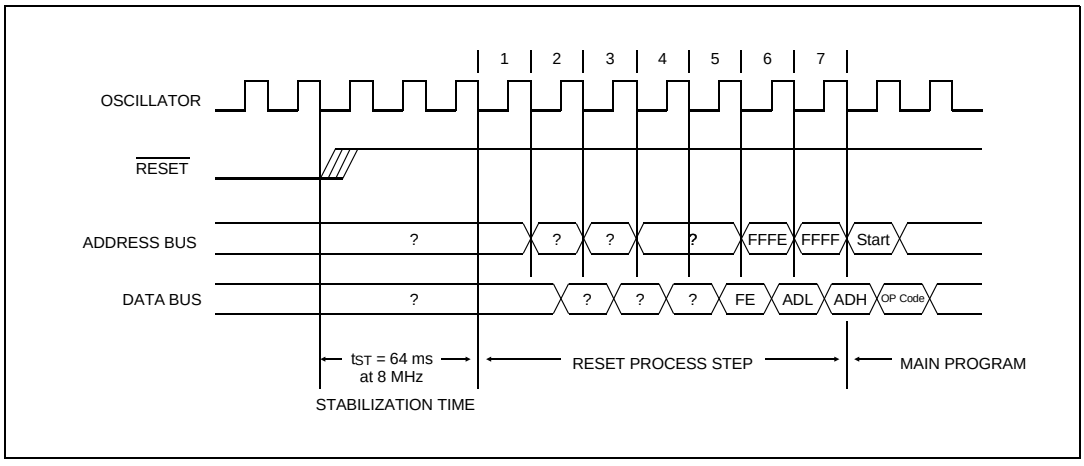


Figure 36. Timing Diagram after Reset

OSCILLATOR CIRCUIT

X_{IN} and X_{OUT} are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 37.

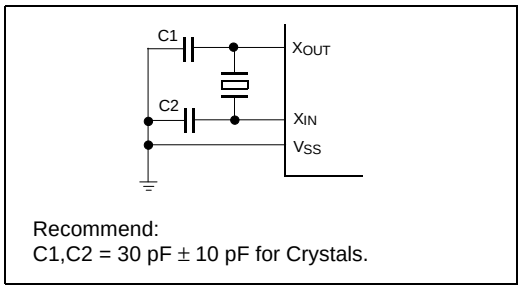


Figure 37. Oscillator Connections

To drive the device from an external clock source, X_{OUT} should be left unconnected while X_{IN} is driven as shown in Figure 39. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

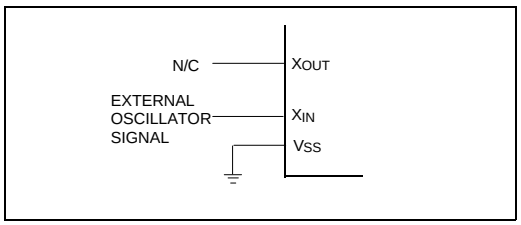


Figure 39. External Clock Drive Configuration

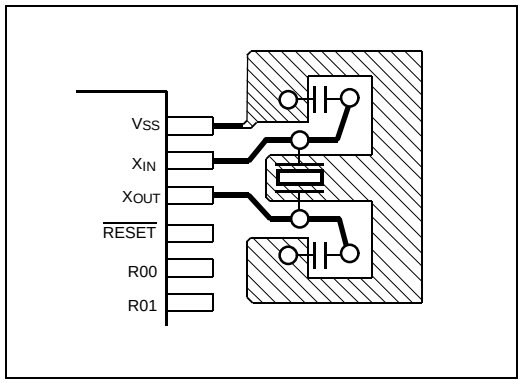


Figure 38. Layout of Crystal

Oscillation circuit is designed to be used either with a ceramic resonator or crystal oscillator. Since each crystal and ceramic resonator have their own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

In addition, see Figure 38. for the layout of the crystal. In all cases, an external clock operation is available.

OTP PROGRAMMING

The GMS81504T is one-time PROM (OTP) microcontroller with 4K bytes electrically programmable read only memory for the GMS81504 system evaluation, first production and fast mass production.

To programming the OTP device, user can have two way. One is using the universal programmer which is support HME microcontrollers, other is using the general EPROM programmer.

1. Using the Universal programmer

Third party universal programmer are shown as below.

Manufacturer: **Advantech**
Web site: http://www.aec.com.tw
Programmer: LabTool-48

Manufacturer: **Hi-Lo systems**
Web site: http://www.hilosystems.com.tw
Programmer: ALL-11, GANG-08

Socket adapters are supported from third party programmer manufacturer.

2. Using the general EPROM(27C256) programmer

When user use general EPROM programmer, socket adaper is essencially necessary. It convert pin to fit the pin of general 27C256 EPROM.

Socket Adapter: OA815A-30SD (30SDIP)

In assembler and file type, two files are generated after compiled. One is "*.HEX", another is "*.OTP". The "*.HEX" file is used for emulation in circuit emulator CHOICE-Jr™ and "*.OTP" file is used for programming to OTP device.

Programming Procedure

1. Select the EPROM device and manufacturer on EPROM programmer (Intel 27C256)

2. Select the programming algorithm as a Intelligent mode (apply 1ms writing pulse).

3. Load the file (*.OTP) to the programmer.

4. Set the programming address range as below table.

Address	Set Value
Buffer start address	7000_H
Buffer end address	$7FFF_H$
Device start address	7000_H

5. Mount the socket adapter with the OTP device onto the PROM programmer.

6. Start the PROM programmer to programming/ verifying.

GMS81504T PROGRAMMING MANUAL

DEVICE OVERVIEW

The GMS81504T is a high-performance CMOS 8-bit microcontroller with 4K bytes of EPROM. The device is one of GMS800 family. The HYUNDAI GMS81504T is a powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. The GMS81504T provides the following standard features: 4K bytes of EPROM, 128 bytes of RAM, 23 I/O lines, 16-bit or 8-bit timer/counter, a precision analog to digital converter, on-chip oscillator and clock circuitry.

PIN DESCRIPTION

Pin No.	MCU Mode		OTP Mode	
1	R01	I/O	O1	I/O
2	R00	I/O	O0	I/O
3	R47	I/O	A0	I
4	R46	I/O	A1	I
5	R45	I/O	$\overline{CE}$	I
6	R44	I/O	$\overline{OE}$	I
7	R67/AN7	I/O	A2	I
8	R66/AN6	I/O	A3	I
9	AV_{REF}	I	(1)	I
10	R65/AN5	I/O	A4	I
11	R64/AN4	I/O	(1)	I
12	R41/INT1	I/O	A5	I
13	R40/INT0	I/O	A6	I
14	R55/BUZ	I/O	A7	I
15	R56	I/O	A8	I

Pin No.	MCU Mode		OTP Mode	
16	R57	I/O	A9	I
17	$\overline{RESET}$	I	(1)	I
18	X_{IN}	I	(1)	I
19	X_{OUT}	O	(2)	O
20	V_{SS}	V_{SS}	V_{SS}	V_{SS}
21	R43	I/O	A10	I
22	R42	I/O	A11	I
23	$\overline{TEST}$	I/O	V_{PP}	V_{PP}
24	R07	I/O	O7	I/O
25	R06	I/O	O6	I/O
26	R05	I/O	O5	I/O
27	R04	I/O	O4	I/O
28	R03	I/O	O3	I/O
29	R02	I/O	O2	I/O
30	V_{DD}	V_{DD}	V_{DD}	V_{DD}

NOTES:

1. Check marked pins must be connected on V_{SS}, because these pins are input ports during programming, program verify and reading
2. X_{OUT} pin must be opened during programming.

I/O: Input/Output Pin
I: Input Pin
O: Output Pin

PIN FUNCTION (OTP Mode)

V_{PP} (Program Voltage)

V_{PP} is the input for the program voltage for programming the EPROM.

$\overline{CE}$ (Chip Enable)

$\overline{CE}$ is the input for programming and verifying internal EPROM.

$\overline{OE}$ (Output Enable)

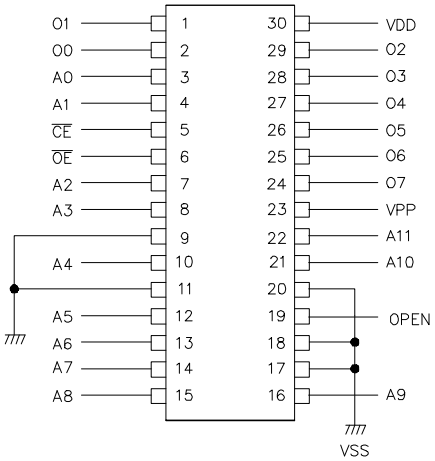
$\overline{OE}$ is the input of data output control signal for verify.

A_0~A_{11} (Address Bus)

A_0~A_{11} are address input pins for internal EPROM.

O_0~O_7 (EPROM Data Bus)

These are data bus for internal EPROM.



Pin connection during programming

PROGRAMMING

The GMS81504T has address A_0~A_{11} pins. Therefore, the programmer just program 4K bytes data (address 7000_H to $7FFF_H$) into the GMS81504T OTP device. During the programming, addresses A_{12}~A_{15} of the programmer must be pulled to a logic high.
When the programmer write the data from 7000_H to $7FFF_H$, consequently, the data actually will be written into addresses $F000_H$ to $FFFF_H$of the OTP device.

1. The data format to be programmed is made up of Motorola S1 format.

Ex) "Motorola S1" format;

```
S00800005741544348 80
S1247000E1FF3BFF04A13F8F06E101711B821B1BE01D1B3B191BF6181BF01C1BFF081BFF0AB0
S12470211BF5091BFF0B1BFF3F1B003E1B003D1B003C1BFF3B1B003A1BFF391BFF381BFF350D
:
:
S1057FF2983FB2
S1057FFEFF0F6F
S9030000FC
```

2. Down load above data into programmer from PC.

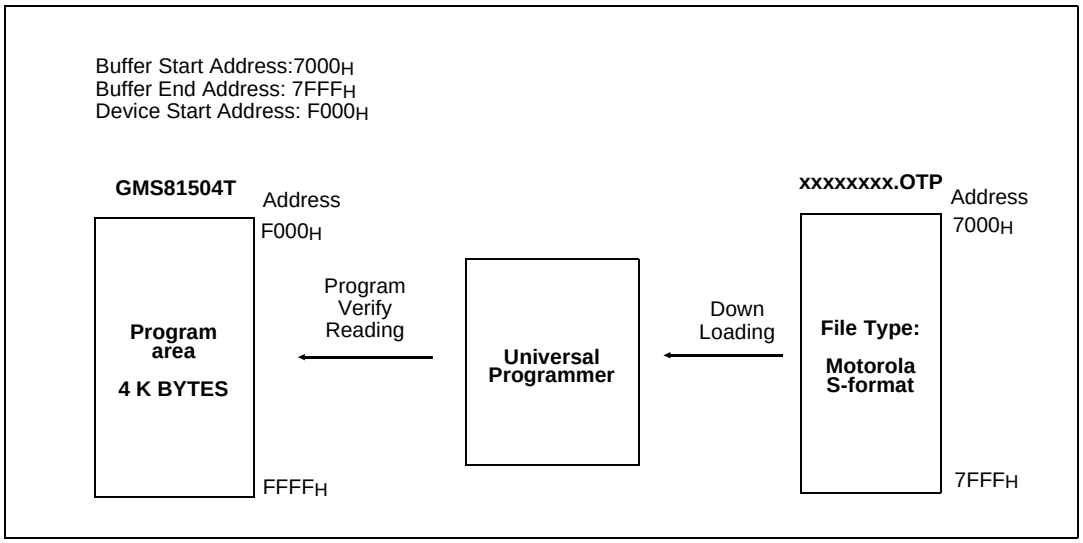
3. Programming the data from address 7000_H to $7FFF_H$ into OTP MCU, the data must be turned over respectively, and then record the data.When read the data, it also must be turned over.
Ex) 00(00000000)→FF(11111111), 76(01110110)→89(10001001), FF(11111111)→00(00000000) etc.

4. Of course, the check sum is result of the sum of whole data from address 7000_H to $7FFF_H$ in the file (not reverse

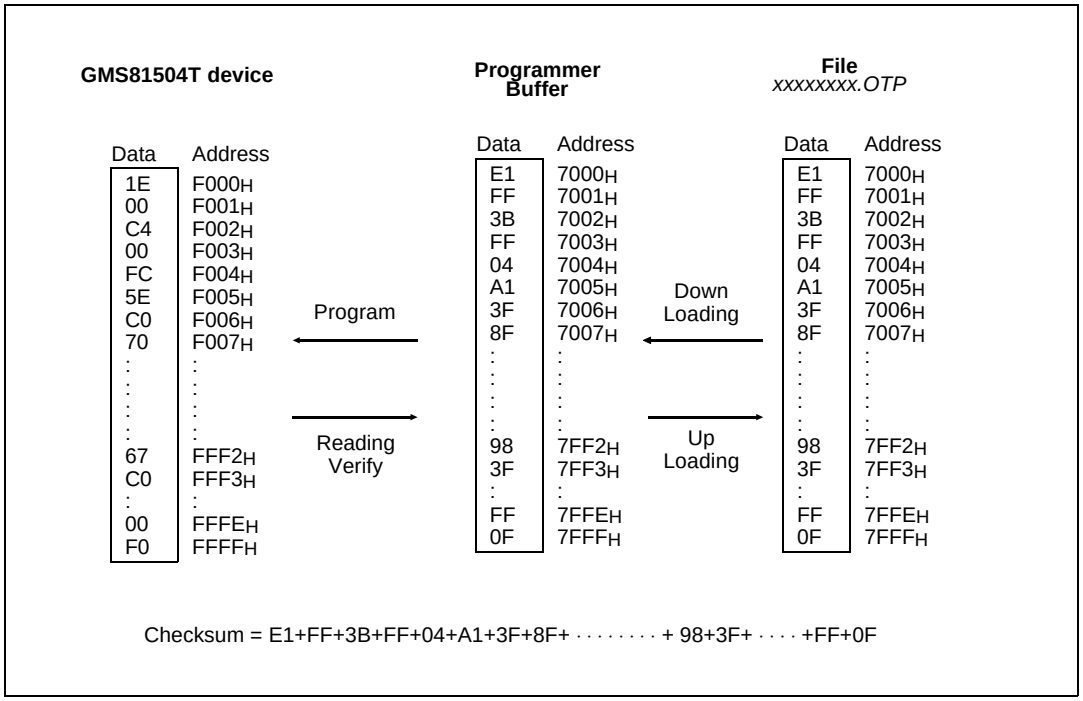
data of theOTP MCU).

* When GMS81504T shipped, the blank data of it is initially 00_H (not FF_H).

Programming Flow



Programming Example



DEVICE OPERATION MODE

(T_A = 25°C ±5°C)

Mode	$\overline{CE}$	$\overline{OE}$	A0~A11	VPP	VDD	O0~O7
Read	X		X	V_{DD}	5.0V	D_{OUT}
Output Disable	V_{IH}	V_{IH}	X	V_{DD}	5.0V	Hi-Z
Programming	V_{IL}	V_{IH}	X	V_{PP}	V_{DD}	D_{IN}
Program Verify	X		X	V_{PP}	V_{DD}	D_{OUT}

NOTES:
1. X = Either V_{IL} or V_{IH}
2. See DC Characteristics Table for V_{DD} and V_{PP} voltages during programming.

DC CHARACTERISTICS

(V_{SS}=0 V, T_A = 25°C ±5°C)

Symbol	Item	Min	Typ	Max	Unit	Test condition
V_{PP}	Intelligent Programming	12.0	-	13.0	V	
	Quick-pulse Programming	12.5	-	13.0	V	
V_{DD}(1)	Intelligent Programming	5.75	-	6.25	V	
	Quick-pulse Programming	6.0	-	6.5	V	
I_{PP} (2)	V_{PP} supply current			50	mA	$\overline{CE}$=V_{IL}
I_{DD} (2)	V_{DD} supply current			30	mA	
V_{IH}	Input high voltage	0.8 V_{DD}			V	
V_{IL}	Input low voltage			0.2 V_{DD}	V	
V_{OH}	Output high voltage	V_{DD}-1.0			V	I_{OH} = -2.5 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 2.1 mA
I_{IL}	Input leakage current			5	uA	

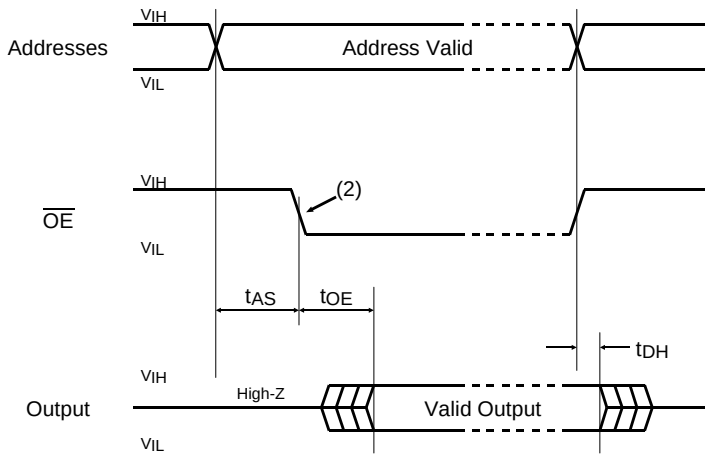
NOTES:

1. V_{DD} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The maximum current value is with outputs O_0 to O_7 unloaded.

SWITCHING WAVEFORMS

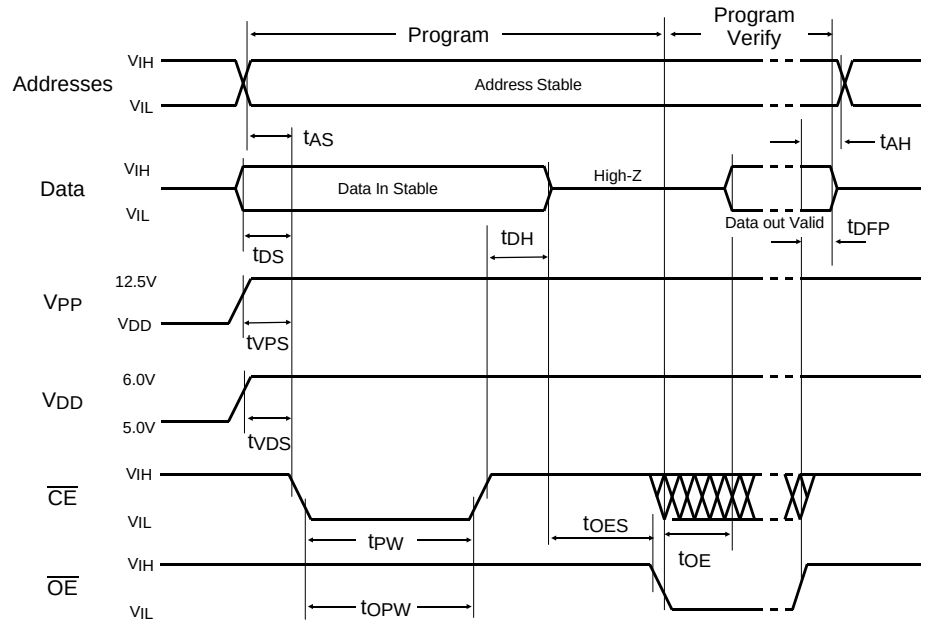
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from H to L	Will be changing from H to L
	May change from L to H	Will be changing from L to H
	Do not care any change permitted	Changing state unknown
	Does not apply	Center line is high impedance "Off" state

READING WAVEFORMS



NOTES:
1. The input timing reference level is 1.0 V for a V_{IL} and 4.0V for a V_{IH} at V_{DD}=5.0V
2. To read the output data, transition requires on the $\overline{OE}$ from the high to the low after address setup time t_{AS}.

PROGRAMMING ALGORITHM WAVEFORMS



NOTES:
1. The input timing reference level is 1.0 V for a V_{IL} and 4.0V for a V_{IH} at V_{DD}=5.0V

AC READING CHARACTERISTICS

(V_{SS}=0 V, T_A = 25°C ± 5°C)

Symbol	Item	Min	Typ	Max	Unit	Test condition
t_{AS}	Address setup time	2			us	
t_{OE}	Data output delay time			200	ns	
t_{DH}	Data hold time	0			ns	

NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC PROGRAMMING CHARACTERISTICS

(V_{SS}=0 V, T_A = 25°C ± 5°C; See DC Characteristics Table for V_{DD} and V_{PP} voltages.)

Symbol	Item	Min	Typ	Max	Unit	Condition* (Note 1)
t_{AS}	Address set-up time	2			us	
t_{OES}	$\overline{OE}$ set-up time	2			us	
t_{DS}	Data setup time	2			us	
t_{AH}	Address hold time	0			us	
t_{DH}	Data hold time	1			us	
t_{DFP}	Output disable delay time	0			us	
t_{VPS}	V_{PP} setup time	2			us	
t_{VDS}	V_{DD} setup time	2			us	
t_{PW}	Program pulse width	0.95	1.0	1.05	ms	
t_{OPW}	$\overline{CE}$ pulse width when over programming	2.85		78.75	ms	(Note 2)
t_{OE}	Data output delay time			200	ns	

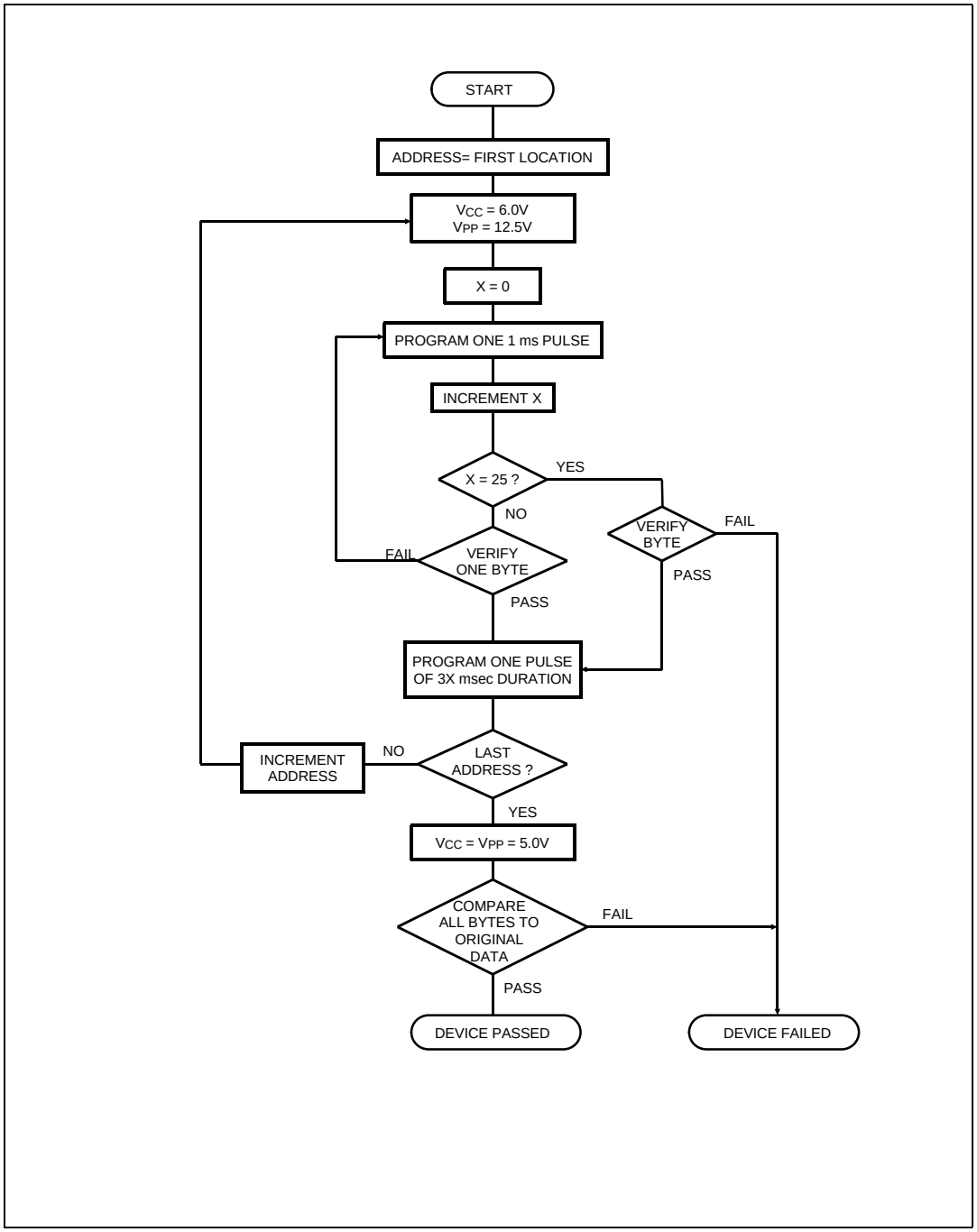
***AC CONDITIONS OF TEST**

Input Rise and Fall Times (10% to 90%) . . . . 20 ns
Input Pulse Levels . . . . . 0.45V to 4.55V
Input Timing Reference Level . . . . . 1.0V to 4.0V
Output Timing Reference Level . . . . . 1.0V to 4.0V

NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X (Intelligent Programming Algorithm only). Refer to page 8.

Intelligent Programming Algorithm



MASK ORDER & VERIFICATION SHEET

GMS81504-HB☐☐☐

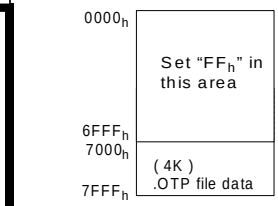
Customer should write inside thick line box.

1. Customer Information

Company Name	
Application	
Order Date	YYYY . MM . DD
Tel: Fax:	
Name & Signature:	

2. Device Information

Package	☐ 30SDIP ☐ 28SOP	
Mask Data	☐ Hitel ☐ Chollian ☐ Internet	
	File Name	.OTP
	Check Sum	( ) ☐ 27256



(Please check mark into ☐)

3. Marking Specification

☐ *Customer's logo*

GMS81504-HBxxx
YYWW KOREA

☐ **HME**
GMS81504-HBxxx
YYWW KOREA

Customer logo is not required ☐

Customer's part number ☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐

HME ROM code number ☐☐☐

Note: If the customer logo must be used in the special mark
Please submit a clean original of the logo.

4. Delivery Schedule

	Date	Quantity	HME Confirmation
Customer Sample	YYYY . MM . DD	pcs	
Risk Order	YYYY . MM . DD	pcs	

5. ROM Code Verification

Verification Date: YYYY . MM . DD
Please confirm our verification data.
Check Sum:
Tel: Fax:
Name & Signature:

This box is written after "5.Verification".

Approval Date: YYYY . MM . DD
I agree with your verification data and confirm you to make mask set.
Tel: Fax:
Name & Signature:

HYUNDAI MicroElectronics