2.5 Gbps CMOS Burst Mode Laser Driver & Limiting Post Amplifier with On-Chip Digital Diagnostic Monitoring

Main Features

- 100 mA bias current and 90 mA modulation current output drive capability
- On-chip **Digital Diagnostic Monitoring (DDMI)**
- Automatic Mean Power and **Automatic Extinction Ratio control**
- Fast burst-mode loop settling time
- Current DAC output for APD bias control
- TX_SD and rogue ONU alarm function
- True average Tx burst power monitor
- Tx fault detection and safety logic
- Power down and sleep mode support
- CSFP I^2C addressing support

Applications

- EPON & GPON FTTh ONU/ONT
- BOSA-on-Board ONU
- SFF/SFP & CSFP modules

General Description

The GN25L95 is a combined burst mode laser driver and limiting post amplifier designed for fiber optic transceiver modules.

The GN25L95 features on-chip digital diagnostic monitoring and digital set-up. This enables a complete solution for SFP/SFF optical transceiver modules.

A **fully compliant SFF-8472 digital diagnostic monitoring** solution can be realised by connecting an external 8k EEPROM.

The GN25L95 features automatic mean power and **automatic extinction ratio** control functions for robust and reliable control of laser operating conditions over temperature.

Auto-ranging A/D converters with digitized monitoring, an internal temperature sensor and an on-chip DAC for controlling an external APD bias circuit are also included.

Consuming 90 mA from a 3.3 V supply the GN25L95 is packaged in a 4x4 mm QFN 28 pin RoHS package rated from -40 to +95 °C.

Block Diagram

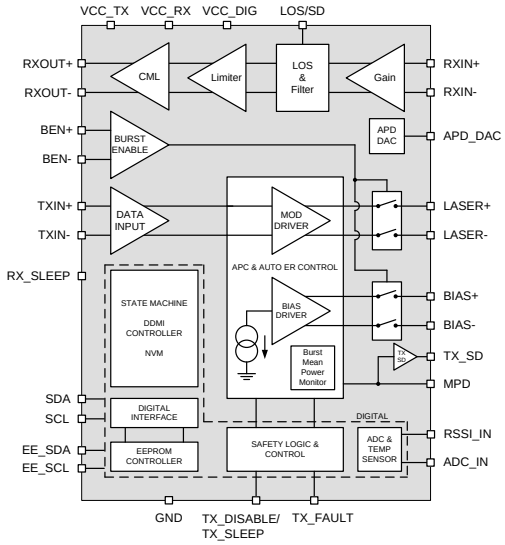

Figure 1 – GN25L95 Functional Block diagram

Package

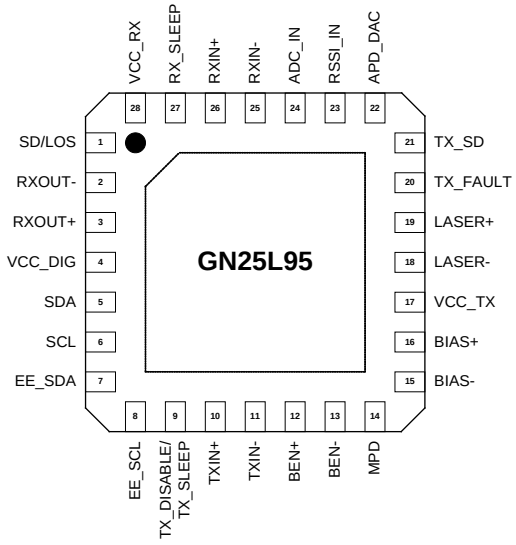

Figure 2 – GN25L95 Package

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Package Diagram & Pin Descriptions

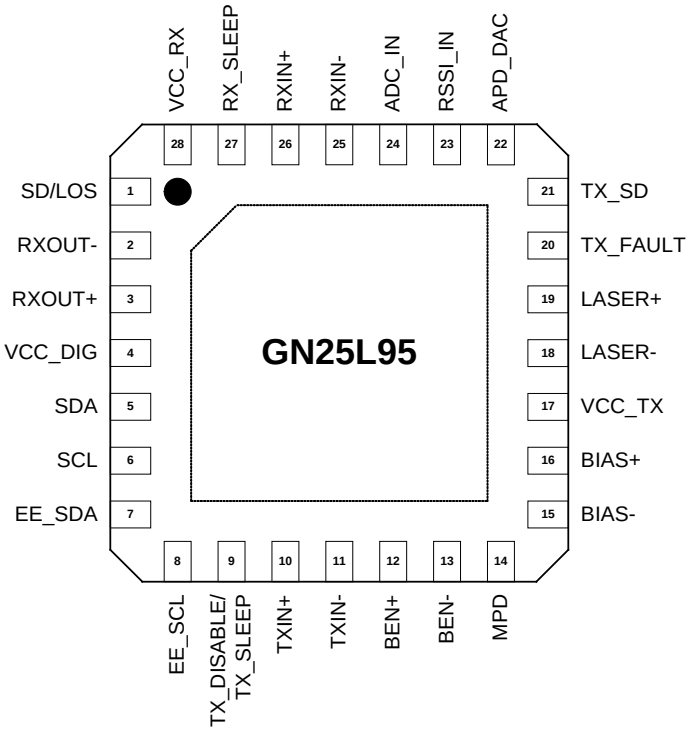

Figure 3 – GN25L95 Package Diagram

Table 1 – Package Pin Descriptions

Pin	Name	Function
1	SD/LOS	Signal Detect / Loss of Signal status output. Polarity and output type programmable: TTL or Open Drain. Connect to VCC_RX using a 4k7 to 10k Ω resistor for Open Drain output. [1]
2	RXOUT-	Receiver inverting CML data output. Typically AC-coupled.
3	RXOUT+	Receiver non-inverting CML data output. Typically AC-coupled.
4	VCC_DIG	+3.3 V power supply for digital block. Connect to VCC_RX using suitable power supply filtering.
5	SDA	Slave I^2C serial data interface connection. On-chip 10k Ω pull-up.
6	SCL	Slave I^2C serial clock interface connection. On-chip 10k Ω pull-up.
7	EE_SDA	Master I^2C serial data interface connection. On-chip 10k Ω pull-up.
8	EE_SCL	Master I^2C serial clock interface connection. On-chip 10k Ω pull-up.
9	TX_DISABLE/ TX_SLEEP	TX_DISABLE control input. Active high. Connect to VCC_TX using a 4k7 to 10k Ω resistor. Also used to enable Tx sleep modes. TX_SLEEP modes selectable via register settings.
10	TXIN+	Transmit data high speed non-inverting input. Internally biased.

11	TXIN-	Transmit data high speed inverting input. Internally biased.
12	BEN+	Burst enable non-inverting input. Internally biased. [1]
13	BEN-	Burst enable inverting input. Internally biased. [1]
14	MPD	Monitor photodiode input for automatic power & extinction ratio control. DO NOT connect any external capacitance to this pin.
15	BIAS-	Laser bias current complementary sink. DO NOT use to drive laser. Connect to VCC_TX via a dummy resistive load of 15 Ω.
16	BIAS+	Laser bias current sink. Always used to drive laser. Connect to laser cathode.
17	VCC_TX	+3.3 V power supply input for transmitter block.
18	LASER-	Laser modulation inverting current sink. [2]
19	LASER+	Laser modulation non-inverting current sink. [2]
20	TX_FAULT	TX_FAULT status output. Polarity and output type programmable: TTL or Open Drain. Connect to VCC_TX using a 4k7 to 10k Ω resistor for Open Drain output.
21	TX_SD	Transmitter signal detect LVTTL output. Polarity programmable.
22	APD_DAC	DAC output. Provides a current sink or source output for controlling an external APD bias control circuit.
23	RSSI_IN	Receiver signal strength indicator input from preceding transimpedance amplifier (TIA). Current input. Programmable Sink or Source.
24	ADC_IN	ADC input. Can be used for external temperature sensor or similar.
25	RXIN-	Received data inverting input.
26	RXIN+	Received data non-inverting input.
27	RX_SLEEP	Digital input control to enable Rx sleep mode.
28	VCC_RX	+3.3 V power supply input for the receiver block.
CP	GND	Common ground pad for IC. Also acts as thermal sink for package.

[1] Semtech recommends adding a 220 Ω series resistor between this pin and the host interface to protect from electrical overstress events during optical transceiver manufacture (sometimes SFF modules are hot-plugged with pin misalignment).
[2] In default mode the LASER+ is used to drive the laser cathode and the LASER- output is connected to VCC_TX via a dummy load resistor (15 Ω). To enable PCB design flexibility the polarity can be inverted so that the LASER- output can be used to drive the laser cathode and the LASER+ is connected to VCC_TX via a dummy load resistor (15 Ω). This can be done by setting the TX_MOD_STEER register bit control.

Table 2 – Absolute Maximum Ratings

These are the absolute maximum ratings beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Symbol	Parameter	Rating	Units
VCC	Power supply (VCC to GND)	-0.4 to 4.0	V
T_{stg}	Storage temperature	-65 to +150	°C
T_{Solder}	Soldering temperature (JEDEC J-STD-020C)	260	°C
$V_{IN\_RX\_MAX}$	Maximum receiver differential input (pk-pk)	1600	mV
$RSSI_{MAX}$	Maximum current on RSSI pin	8.0	mA

Table 3 – Recommended Operating Conditions

Symbol	Parameter	Rating	Units
VCC	Power supply voltage (VCC to GND)	+3.3 ± 10%	V
T_a	Ambient operating temperature	-40 to +95	°C
DR	Data rate	155 to 2700	Mbps
C_{MPD}	Maximum MPD capacitance	20	pF
B_{MPD}	Minimum MPD bandwidth (for AutoER loop)	50	MHz

Table 4 – Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
I_{DD}	Power supply current [1]		92	110	mA

[1] – Includes receiver output CML termination current. Specified for receiver output swing of 900mVpp. Does not include laser bias and modulation currents. Indicated supply current assumes 20 mA bias and 20 mA modulation currents flowing through laser diode. Indicated supply current assumes that automatic extinction ratio control is enabled.

Table 5 – Transmitter Section Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
Transmitter Input Stage					
V_{TxIN}, V_{BEN}	Differential input voltage, pk-pk [1]	200		2400	mV
V_{BEN_TTLLOW}	BEN single-ended TTL low input			0.9	V
$V_{BEN\_TTLHIGH}$	BEN single-ended TTL high input	1.9			V
I_{BEN}	Maximum current on BEN pin			20	mA
V_{TxIN_CM}	TxIN Common mode input voltage		VCC–1.32		V
V_{BEN_CM}	BEN Common mode input voltage		1.4		V
Transmitter Bias Stage					
I_{BIAS}	Bias current	1		100	mA
I_{BIAS_OFF}	Bias current disabled			100	µA

Symbol	Parameter	Min.	Typ.	Max.	Units
Acc_{IBIAS}	Bias current setting accuracy [2]	-10		+10	%
$Stab_{APC}$	APC loop setting stability		±100	±300	ppm/°C
Acc_{MON}	MPD current setting accuracy	-10		+10	%
I_{MPD}	MPD averaged input current	25		1800	µA
V_{MPD_IN}	Voltage at MPD relative to ground		1.0		V
t_{APC_INIT}	APC loop initialisation time [3]			1.0	µs
V_{LASER}	Laser forward voltage [4]		1.5	2.0	V
Laser Modulator Stage					
I_{MOD}	Modulation current	5		90	mA
I_{MOD_OFF}	Modulation current disabled			100	µA
Acc_{MOD}	Modulation current setting accuracy	-10		+10	%
$Stab_{MOD}$	Modulation current temperature stability across operating range			±2	%
T_{RISE} / T_{FALL}	Modulation current rise / fall times [5]		60	80	ps
DJ_{Tx}	Deterministic Jitter, pk-pk [6]		15	40	ps
RJ_{Tx}	Random jitter, rms [7]			1.5	ps
Automatic Extinction Ratio Control					
ER_{TARGET}	Target extinction ratio	5.0		28.0	x:1
		7.0		14.5	dB
ER_{STAB}	ER operating stability [8]		±1.0		dB
Burst Control Stage					
BEN_{ON}	Burst enable time [9]		5.0	12.8	ns
BEN_{OFF}	Burst disable time [10]		5.0	12.8	ns
$T_{B\_ON\_START}$	Burst on time (start-up, 5 ≤ bursts)	200			ns
T_{B_SETTLE}	Burst on settling time (5x burst-on)			1	µs
T_{B_ON}	Burst on time (after APC settled)	200			ns
T_{B_OFF}	Burst off time	96			ns
Transmitter Fault and Control Timing					
t_init	From power on or negation of TX_FAULT by TX_DISABLE [11]		30	50	ms
t_off	TX_DISABLE assert time [12]			10	µs
t_on	TX_DISABLE de-assert time [13]			1	ms
TX_SD_{DELAY}	TX_SD output delay time [14]		40	100	ns
TX_SD_{VAR}	TX_SD output width variation [14]			100	ns

Symbol	Parameter	Min.	Typ.	Max.	Units
t_delay	Time from READY set to transmitter output currents enabled [15]		500		µs
t_fault	TX_FAULT assert time			100	µs
t_reset	Time TX_DISABLE must be asserted to reset TX_FAULT	10			µs

[1] Internally biased differential inputs. TXIN (+/-) and BEN (+/-) inputs require external high speed termination. See transmitter section for further details.
[2] Ibias setting accuracy applies to operation in bias open loop mode.
[3] VCC = 3.0V to 3.6V; TX_DISABLE is de-asserted; BEN changes from low to high. Initialisation of automatic power control loop during burst start-up. Time for monitor current to settle to 90% of the target APCSET monitor value within 3 burst on periods.
[4] Performance parameters measured with V_{LASER} equal to 1.5V typical.
[5] Rise and Fall times indicated are 20% - 80%.
[6] Deterministic jitter measured with a continuous data pattern (no bursting) of 2^7-1 PRBS + 80 consecutive ones + 2^7-1 PRBS + 80 consecutive zeros at 2.5 Gbps. Includes data dependent jitter and periodic jitter.
[7] Random jitter measured with a 1010 test pattern at 2.5 Gbps.
[8] Target ER of 10dB used as reference for specifying ER operating stability. Applies across full operating temperature range.
[9] Assertion of laser bias and modulation currents to within 90% of target values. Valid after APC loop initialised.
[10] De-assertion of laser bias and modulation currents to less than 10% of target values. Valid after APC loop initialised.
[11] Time for GN25L95 transmitter to initialize immediately after power on. Also time to initialize after TX_DISABLE is used to negate a TX_FAULT after a TX_FAULT event has occurred.
[12] Time from rising edge of TX_DISABLE input to when the bias and modulation currents fall below 10% of nominal value.
[13] Time from falling edge of TX_DISABLE input to when the bias and modulation currents rise above 90% of nominal value.
[14] TX_SD delay and variation time measured with respect to BEN timing. See Figure 33 for more details. TX_SD function is derived from actual status of laser bias and modulation currents or MPD current, not BEN input control.
[15] During power up sequence or after a TX_FAULT condition. READY is a soft indicator of an internal hardware status flag that indicates the GN25L95 is powered-up correctly and the NVM content has been copied to volatile register memory.

Table 6 – Receiver Section Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
Receiver Input Stage					
V_{RxIN}	Differential input sensitivity, pk-pk [1]		4.0	8.0	mV
$V_{OVERLOAD}$	Differential input overload, pk-pk [1]	1200			mV
V_{RxCM}	Common mode input voltage		1.65		V
f_{LFC}	Low frequency cut-on			15	kHz
Receiver Output Stage					
$VOUT_{DIFF}$	Output swing setting, pk-pk [2]	600		1000	mV
$VOUT_{VAR}$	Output swing variation	-15		+15	%
$VOUT_{CM}$	Common mode output voltage		1.8		V
T_{RISE} / T_{FALL}	Output rise/fall time, No Slew [3]		90	120	ps
	Output rise/fall time, Fast Slew [3]		160	200	ps
	Output rise/fall time, Med Slew [3]		320	400	ps
	Output rise/fall time, Slow Slew [3]		1280	1600	ps
DCD_{Rx}	Duty Cycle Distortion, pk-pk [4]		5.5	30	ps
DJ_{Rx}	Deterministic jitter, pk-pk [5]		8	30	ps
RJ_{Rx}	Random jitter, rms [6]		1.1	3	ps

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{SQU_EN}	Differential output voltage, pk-pk (squelched)			10	mV
Receiver Signal Detect Stage					
V_{LOS}	LOS programming range [7]	10.0		60.0	mV
HYS	LOS Hysteresis programmable Range (optical) [8]	0.5		3.0	dB
VAR_{THRESH}	LOS/SD threshold variation [9]	-0.5		+0.5	dB
SD_{ASSERT}	LOS/SD assert time [10]	2.3		100	µs
$SD_{DE-ASSERT}$	LOS/SD de-assert time [10]	2.3		100	µs
Receiver APD DAC Control					
APD_{SOURCE}	Full scale DAC source current [11]		1980		µA
APD_{SINK}	Full scale DAC sink current [12]		495		µA
APD_{SRC_ACC}	DAC source ouput accuracy		± 4		%
APD_{SNK_ACC}	DAC sink output accuracy		± 4		%
APD_{SRC_CP}	APD output compliance (sinking)			0.8	V
APD_{SNK_CP}	APD output compliance (sourcing)	V_{CC}-0.8			V

[1] Input sensitivity and overload specified for a BER = 1E-10 and a PRBS 2^{23}-1 at 2.5 Gbps.
[2] Differential pk-to-pk output amplitude swing. Measured using a 11110000 square wave pattern. 1000 mVpp setting not advised for use above 622 Mbps.
[3] Measured using a 11110000 square wave for receiver settings shown in Table 25. Between 20%-80% levels.
[4] Duty cycle distortion value specified (measured differentially) is valid at 2.5Gbps.
[5] Deterministic jitter measured with a 2^7-1 PRBS + 80 consecutive ones + 2^7-1 PRBS + 80 consecutive zeros at 2.5 Gbps. Input amplitudes > 20mVpp differential swing.
[6] Random jitter measured with a 1010 test pattern at 2.5 Gbps. input amplitudes > 20 mVpp differential swing.
[7] Differential input. Equivalent to the optical modulation amplitude. Within the specified range the actual LOS level is within 0.5 dB of the target programmed LOS level. The LOS programming range stated is for hysteresis values of 2.5 dB and below. With 3 dB hysteresis the programming range is reduced to 50 mVpp.
[8] $HYS_{Optical} = 10 \times \log_{10}\left(\frac{V_{LOS\_ASSERT}}{V_{LOS\_DEASSERT}}\right)$, LOS Hysteresis can be set by user to 0.5, 1,1.5, 2, 2.5 or 3 dB optical.
[9] Valid across operating temperature range, supply voltage range and wafer fabrication process corners.
[10] LOS timing measured using open drain LOS output into a 10k Ω resistor pull-up to VCC. From LOS_{ASSERT} threshold +1dB to overload.
[11] APD DAC output has two ranges when used in source mode: 0-1980 µA and 0-990 µA. See page 66 for details.
[12] APD DAC output has two ranges when used in sink mode: 0-495 µA and 0-247.5 µA. See page 66for details.

Table 7 – Digital Monitoring & Interface Section Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
Digital Diagnostic Monitoring Functions					
T_{RANGE}	Temperature sensor range [1]	- 40		+ 95	°C
T_{ACC}	Temperature absolute accuracy		± 2	± 3	°C

Symbol	Parameter	Min.	Typ.	Max.	Units
TxP_{ADC}	Tx power monitor range [1]	30		1800	µA
TxP_{ACC}	Tx power monitor accuracy [2]		± 10	± 25	%
TxB_{ADC}	Tx bias current monitor range [1]	1		100	mA
TxB_{ACC}	Tx bias current monitor accuracy			± 10	%
TxM_{ADC}	Tx mod current monitor range [1]	5		90	mA
TxM_{ACC}	Tx modulation monitor accuracy			± 10	%
VCC_{ADC}	Supply voltage monitor range [1, 3]	2.6		4.0	V
VCC_{ACC}	Supply voltage monitor accuracy			± 3	%
$RSSI_{ADC}$	RSSI monitor input range [1, 4]	1		2048	µA
$RSSI_{ACC}$	RSSI monitor input accuracy		± 10	± 25	%
ADC_{RANGE}	ADC input range	0		2.5	V
ADC_{ACC}	ADC accuracy (Inputs ≥ 100mV)		± 2	± 10	%
ADC_{Ω}	ADC input impedance		1 M		Ω
PO_{RAMP}	Power-On Ramp [5]			100	ms
POR_{DELAY}	Power-On Reset Delay		20	30	ms
T_{TXPWR_VAL}	Length of time sampled MPD value is held on storage capacitor [6]	0.01	10		s
T_{READY}	Time after power-on to READY set			80	ms
T_{DDMI}	DDMI monitor sampling cycle time			8	ms
$T_{DT\_RDY\_BAR}$	Time to DATA_READY_BAR			189	ms
T_{SLEEP_TX}	Time to Sleep/Wake on Tx [7]		500	1000	ns
T_{SLEEP_RX}	Time to Sleep/Wake on Rx [8]			1	ms
I_{SLEEP_TX}	Tx current in fast sleep mode			3	mA
I_{SLEEP_RX}	Rx current during sleep mode			1	mA
t_off	Soft TX_DISABLE assert time			100	ms
T_on	Soft TX_DISABLE de-assert time			100	ms
t_fault	Soft TX_FAULT flag assert time			100	ms
t_loss_on	Soft LOS flag assert time			100	ms
t_loss_off	Soft LOS flag de-assert time			100	ms

Symbol	Parameter	Min.	Typ.	Max.	Units
Slave I^2C Interface					
F_{SCL}	SCL Clock [9]		100	400	kHz
t_{LOW}	Low period of SCL clock	1.2			µs
t_{HIGH}	High period of SCL clock	0.6			µs
t_{DH}	Data hold time	0		150	ns
t_{DS}	Data set-up time	100			ns
t_R	Rise time for SDA and SCL			100	ns
t_F	Fall time for SDA and SCL			100	ns
t_{SS}	Set up for STOP condition	0.6			µs
t_{BUF}	Bus free time between a STOP and START condition	1.2			µs
$C_{I/O}$	Capacitance for each I/O pin			10	pF
Low Speed I/O					
$V_{LOSHIGH}$	LOS/SD output voltage high [10,11]	2.0			V
V_{LOSLOW}	LOS/SD output voltage low [10,11]			0.4	V
I_{LOS_OD}	LOS pin Max current (Open Drain) [10]			20	mA
$I_{LOS\_TTL\_HI}$	LOS output current high (TTL) [10]	-4.0			mA
$I_{LOS\_TTL\_LO}$	LOS output current low (TTL) [11]			4.0	mA
$V_{TX\_FAULT\_HI}$	TX_FAULT output voltage high [10,11]	2.0			V
$V_{TX\_FAULT\_LO}$	TX_FAULT output voltage low [10,11]			0.4	V
$I_{FAULT\_TTL\_HI}$	TX_FAULT current high (TTL) [11]	-4.0			mA
$I_{FAULT\_TTL\_LO}$	TX_FAULT current low (TTL) [11]			4.0	mA
$V_{TX\_SD\_HI}$	TX_SD output voltage high [11]	2.0			V
$V_{TX\_SD\_LO}$	TX_SD output voltage low [11]			0.4	V
$I_{TX\_SD\_HI}$	TX_SD output current high [11]	-4.0			mA
$I_{TX\_SD\_LO}$	TX_SD output current low [11]			4.0	mA
$V_{TX\_DIS\_HI}$	TX_DISABLE input voltage high	2.0		VCC	V
$V_{TX\_DIS\_LO}$	TX_DISABLE input voltage low	0		0.8	V

[1] Actual monitor operating range is limited to GN25L95 operating conditions. Theoretical monitor reporting range indicated in section 'Internal Diagnostic Monitoring' on page 77.
[2] Represents better than ±1.0 dB error on Tx Power monitor reading.
[3] VCC monitor applies to each separate supply: VCC_TX, VCC_RX. Only valid within supply operating range.
[4] RSSI input monitor is a current input. Current input can be sink or source and the current input mode is selected using bit RSSI_POLARITY.
[5] Device will be stable when Vcc = 2.9V
[6] Time taken for the charge on the Tx Power sampling capacitor to reduce to 50% of its initial value. In the event of a TX_DISABLE or TX_FAULT the Tx Power monitor will report the value held on the Tx Power sampling capacitor and will therefore take a finite time to reduce to zero as the charge stored on the capacitor is dissipated away. This value can be digitally held in memory after the most recent BEN assert to maintain a constant TX_POWER value for a programmable amount of time between bursts.

[7] Tx Sleep time is time taken to reach less than 10% of Tx nominal bias and modulation currents; Tx Wake time is time taken to reach more than 90% of Tx nominal bias and modulation currents.
[8] Rx Sleep time is time taken to reach less than 10% of Rx normal supply current; Rx Wake time is time taken to reach more than 90% of Rx normal supply current.
[9] I^2C Slave interface operates at 100kHz and 400kHz without any clock stretching.
[10] Open drain output pulled high externally using a 4k7 Ω to 10k Ω resistor.
[11] TTL output driver.

Table 8 – Default Limits

Symbol	Parameter	Min.	Typ.	Max.	Units
VCC_{HIGH_A}	Internal VCC_TX high limit assert		4.0		V
VCC_{HIGH_D}	Internal VCC_TX high limit de-assert		3.8		V
VCC_{LOW_A}	Internal VCC_TX low limit assert		2.6		V
VCC_{LOW_D}	Internal VCC_TX low limit de-assert		2.8		V

Note: In the event that the TX_VCC supply exceeds the limits specified in table 8, the Transmitter output drive currents will be disabled and a non-latching TX_FAULT output will be asserted. If the TX_VCC supply returns to a value within the limits specified then the TX_FAULT will be de-asserted and the transmitter output drive currents will be reinstated.

Typical Operating Characteristics

Typical operating characteristics of the GN25L95 at +3.3 V, 25 °C unless otherwise stated. Receiver terminated into 100 Ω differential load as shown in Figure 51.

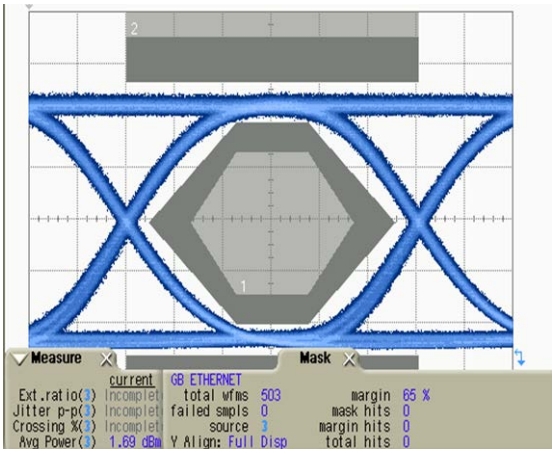

Figure 4 – Tx Optical Eye @ 1.25 Gbps

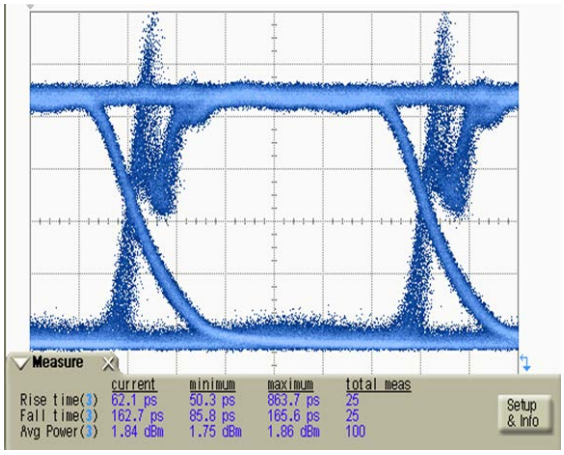

Figure 5 – Tx Unfiltered Optical Eye @ 1.25 Gbps

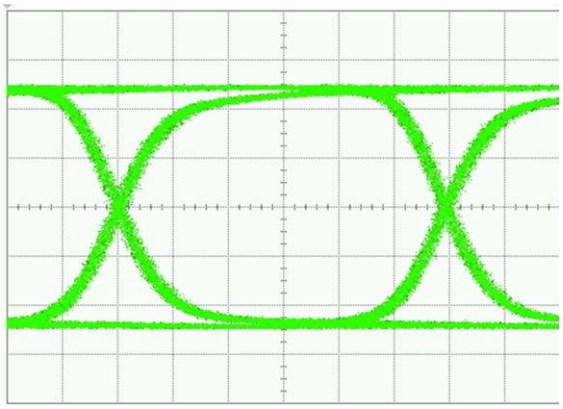

Figure 6 – Rx Single Ended Output @ 2.5 Gbps

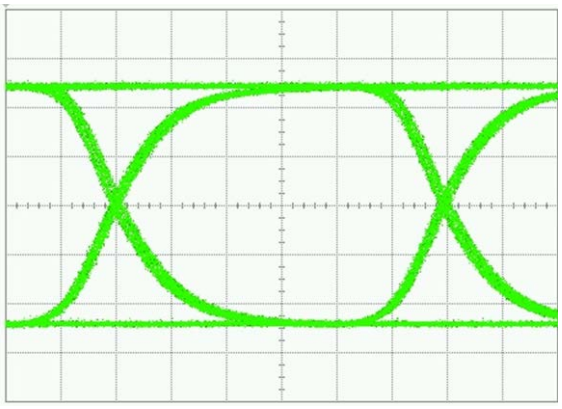

Figure 7 – Rx Single Ended Output @ 1.25 Gbps

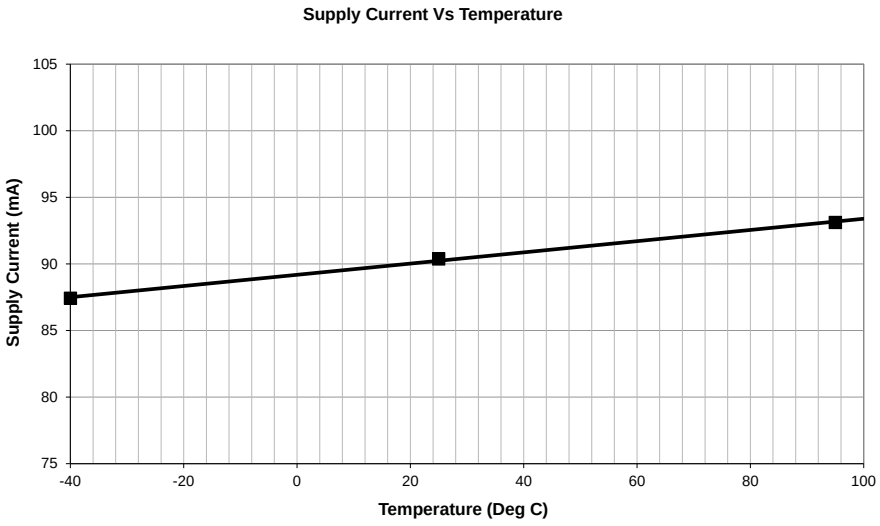

Figure 8 – GN25L95 Typical Supply Current (excluding laser currents)

Functional Block Diagram

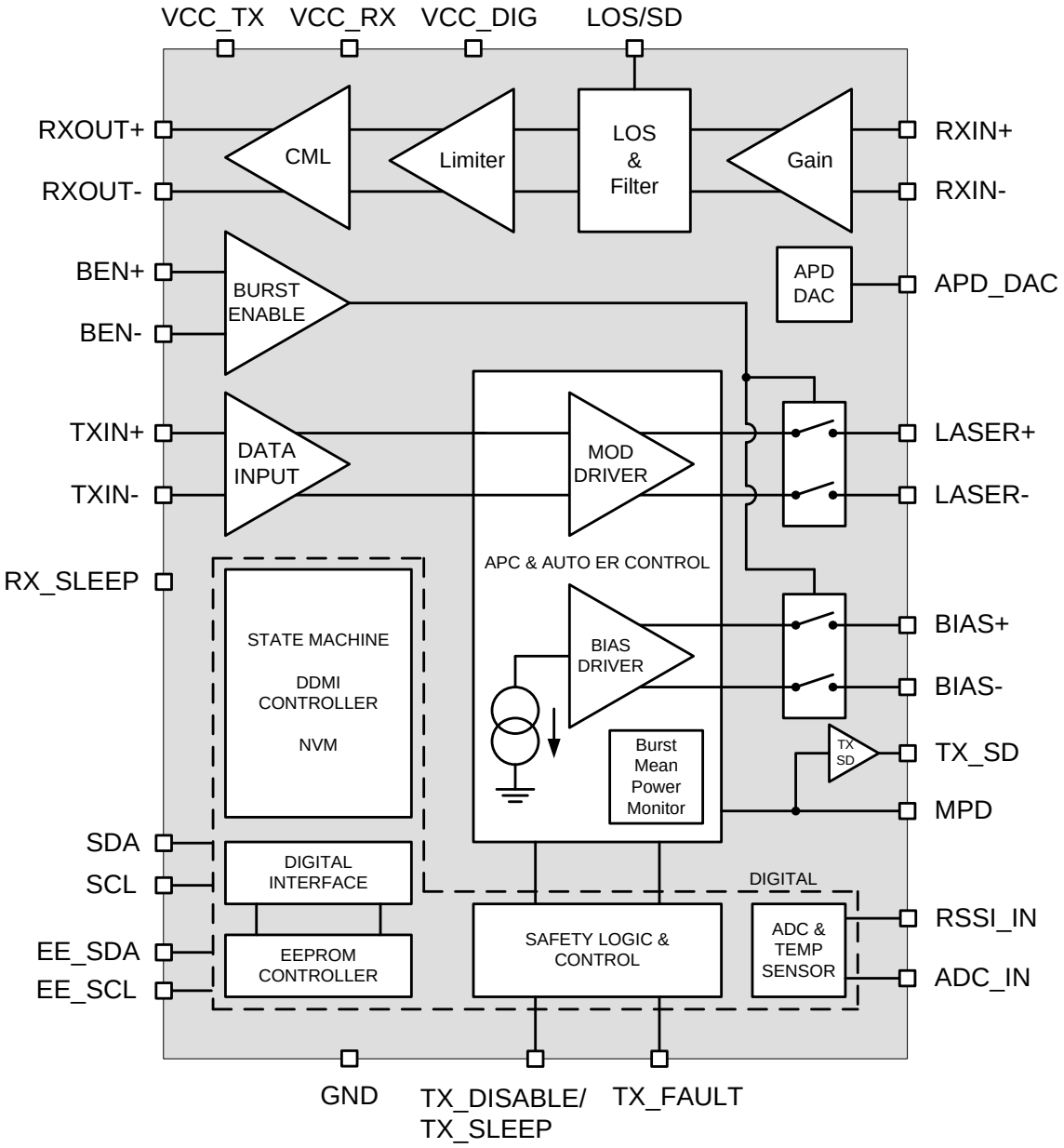

Figure 9 – GN25L95 Functional Block Diagram

The GN25L95 is a pure CMOS combined burst-mode laser driver and limiting amplifier intended for use in both burst-mode and continuous wave (CW), i.e. non-burst, telecom and datacom applications. Both transmitter and receiver signal paths operate up to 2.5 Gbps making the GN25L95 suitable for use in all popular module and protocol applications including BPON, EPON, GPON, OC-3, OC-12, OC-48, GbE, and CSFP transceivers. The GN25L95 includes on-chip fully compliant SFF-8472 digital diagnostics running on an internal state machine controller. The GN25L95 is particular suited to BOSA-on-Board ONU applications that can take advantage of the on-chip APD DAC output. In addition the GN25L95 has on-chip Non Volatile Memory (NVM) to store set-up data and is programmed digitally via an I^2C interface. The GN25L95 also includes on-chip sensors and analogue-to-digital converters required for SFF-8472 DDMI monitoring of optical transceivers. The transmitter contains full safety logic control circuitry to meet IEC-60825 eye safety requirements.

Functional Description

Power Supplies and Start-up Sequence

The GN25L95 features three separate power domains: VCC_TX for the transmitter supply, VCC_RX for the receiver supply and VCC_DIG for the digital supply.

VCC_RX and VCC_DIG can be physically connected and powered together whilst the VCC_TX can be powered independently. If VCC_DIG is connected to the VCC_RX then supply filtering components should be used.

The GN25L95 has been designed so that the transmitter supply can be powered independently of the receiver and digital supplies. This enables the user to power down the transmitter during normal operation whilst continuing to operate the receiver and digital circuits. This feature has been specifically included for use in PON ONU applications.

Recommended filtering and de-coupling of the GN25L95 power supplies is shown in the applications section of this document.

The GN25L95 power-up sequence is shown in Figure 10 below and assumes VCC_TX and VCC_RX are powered at the same time as VCC_DIG.

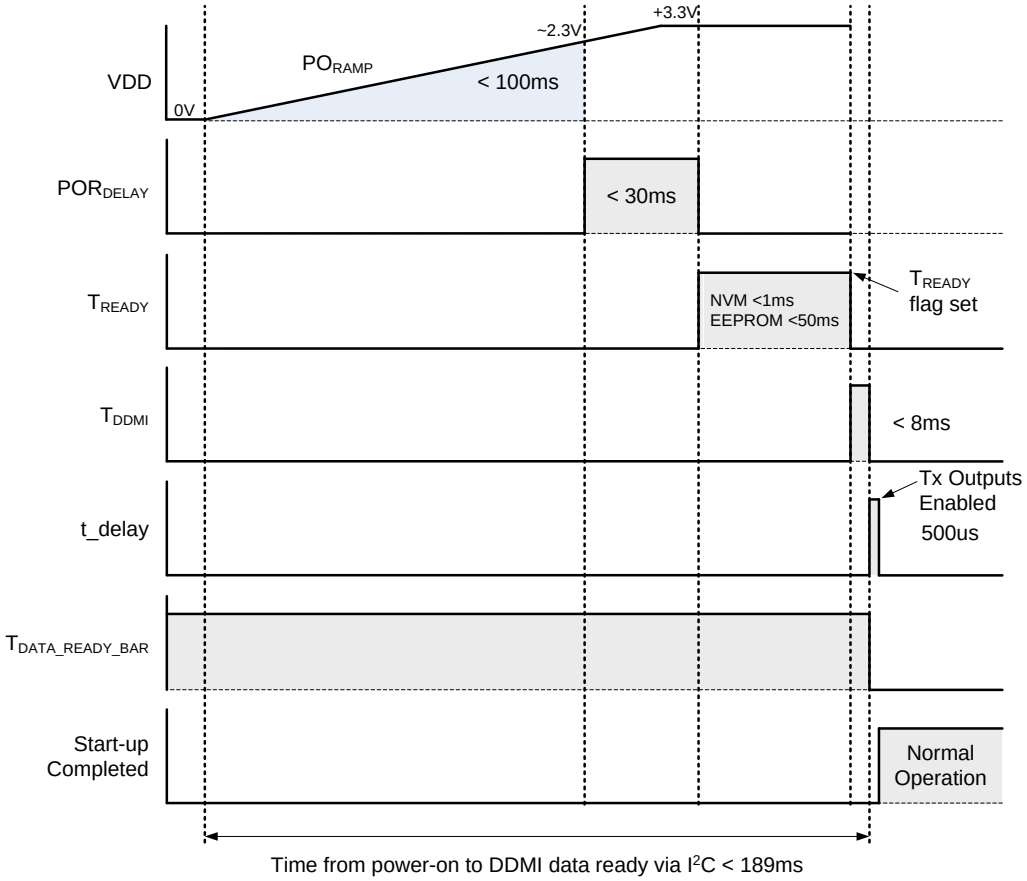

Figure 10 – GN25L95 Power-up timing sequence

The GN25L95 has an on-chip power-on reset circuit to guarantee that the IC powers up correctly. The digital functions, I^2C interface and non-volatile memory within the GN25L95 are controlled by a digital state machine. During the period before T_{READY} is set the transmitter outputs will be disabled and the receiver outputs will be squelched. The LOS output will be asserted high. The POR assert level is typically 2.3 V with a hysteresis of around 100 mV. During power-up to completion of T_{READY}, the GN25L95 will not acknowledge I^2C transfers.

GN25L95 State Machine Controller

The GN25L95 features an internal state machine controller that runs all operating modes and processes data internally to provide a digital diagnostic monitoring solution fully compliant to SFF-8472 (when using external EEPROM). The state machine automatically detects what type of memory is present and configures itself accordingly.

The GN25L95 has two I^2C interfaces: (1) a main I^2C (slave) interface for connection to an external host master or external MCU and (2) an I^2C (master) interface for connection to an external EEPROM memory. The GN25L95 host interface responds to I^2C addresses A0h and A2h by default as detailed in the SFF-8472 multi-source agreement (MSA). The GN25L95 can also be set-up to respond to other I^2C addresses by changing the base address in the GN25L95 control settings – this can be particularly useful for CSFP applications.

The GN25L95 implements a tabled approach to memory addressing to provide additional memory locations for GN25L95 control settings and data that is accessed via the upper A2h addresses 80h to FFh. The function of the upper A2h addresses is determined by the table select byte A2h 7Fh. The user programs this byte to select which memory table to access at address A2h registers 80h to FFh.

The I^2C slave interface physically reads and writes to internal volatile memory registers within the GN25L95. Depending on the mode of operation, the state machine controller will load the internal memory registers with data stored in internal NVM or external EEPROM on power-up.

The diagram below shows the full addressable memory space of the GN25L95.

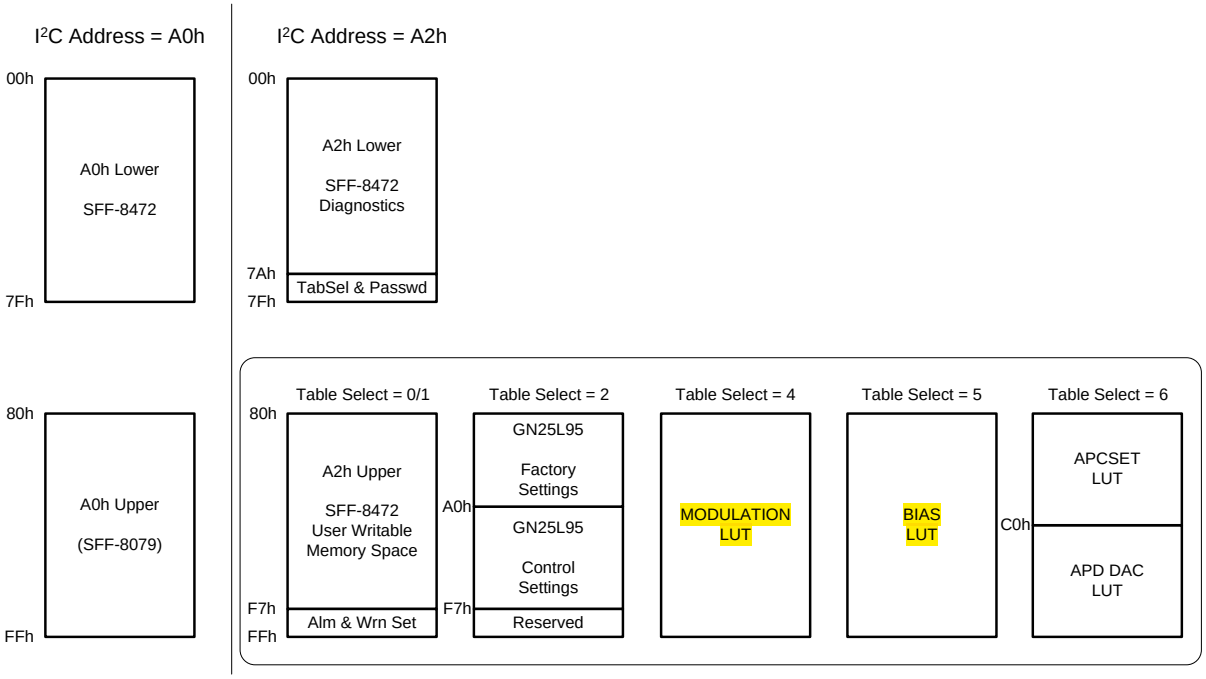

Figure 11 – GN25L95 Register Addressing

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Modes of Operation

The GN25L95 is highly configurable and offers multiple set-up configurations to suit various applications and operating conditions. In particular the modulation and bias currents can be programmed over temperature using several methods of control: Direct programming of Modulation and Bias DACs, Temperature indexed Look-Up Table (LUT) control of Modulation and Bias, Mean Power control using the Automatic Power Control (APC) loop and Automatic Extinction Ratio control – a closed loop control method for controlling modulation current over temperature.

There are three main modes of operation and configuration for memory interfacing on the GN25L95:

1. Internal NVM mode – uses internal NVM to store set-up data.
2. External EEPROM mode – uses external EEPROM to store set-up data.
3. External MCU mode – uses an external MCU to store and process data.

The GN25L95 automatically configures itself into 1 of the 3 operating modes during the power-up process and dependent on the external connections made to the GN25L95. These are described below in detail.

Internal NVM mode

The GN25L95 has enough on-chip non-volatile memory (NVM) to allow the GN25L95 to function without the need for external EEPROM memory or control via an external MCU. The internal NVM mode is particularly suited to low cost applications that do not require SFF-8472 compliance. In this mode the SFF-8472 state machine controller is fully functional, however due to there being no EEPROM memory the A0h and A2h memory areas are entirely volatile register space. The external calibration is not used in this mode. The GN25L95 selects this mode of operation by default if an external EEPROM is not found to be connected to the EE_SDA and EE_SCL I/O pins and those pins are left unconnected. The GN25L95 then loads all setting and control data from the internal NVM.

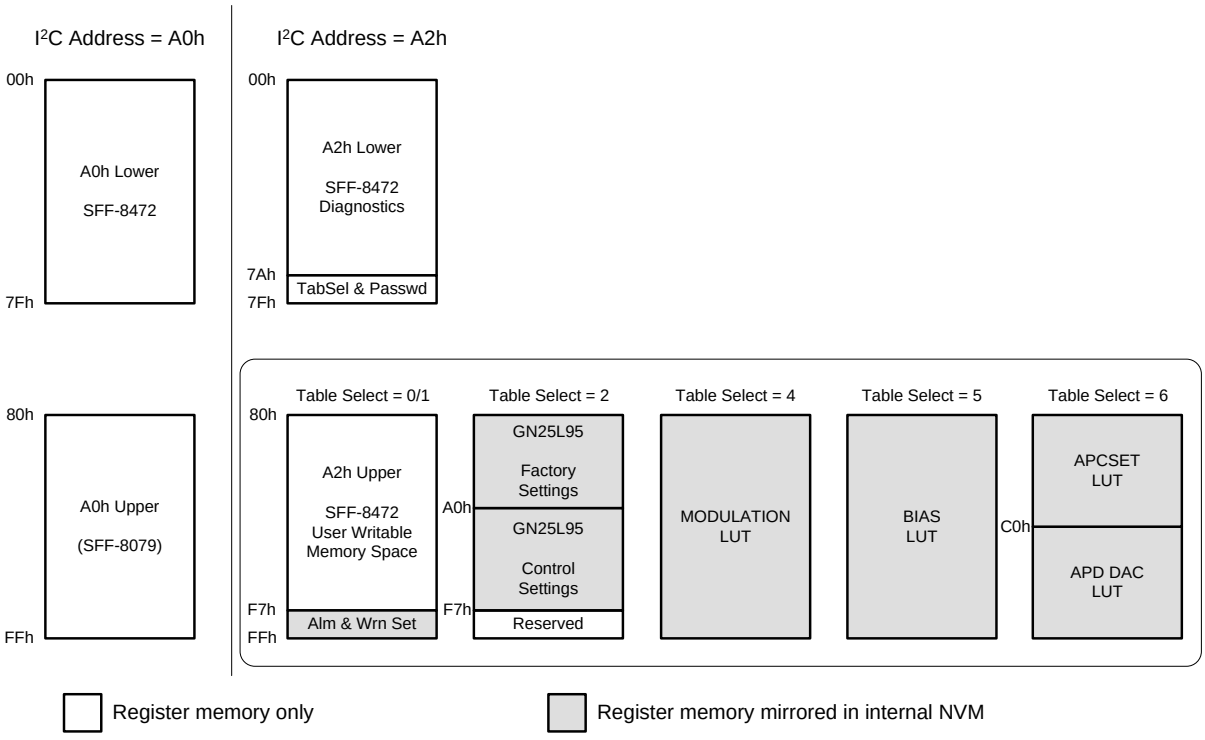


Figure 12 – GN25L95 NVM backed-up addresses

As shown in Figure 12 above, A0h and A2h (Table Select 0/1) are not stored in internal NVM and are therefore completely volatile except for registers F7h to FFh which contain Alarm and Warning control functions.

A2h Tables 2, 4, 5 and 6 are backed-up in NVM. There is enough NVM to allow each table to be written to twice. Note that some registers that contain dynamic data (such as ADC conversions and status monitors) are not backed up in NVM as they are updated on power-up by the state machine.

External EEPROM mode

The GN25L95 can be interfaced with an external 8K bit EEPROM to provide a completely re-writable SFF-8472 compliant digital diagnostic monitoring solution. The EEPROM should be an 8k bit device with 16-byte pages such as the Atmel AT24C08B. The content of the EEPROM are loaded into the GN25L95 volatile registers at power-up. Note that some registers that contain dynamic data (such as ADC conversions and status monitors) are not backed up in EEPROM as they are updated on power-up by the state machine.

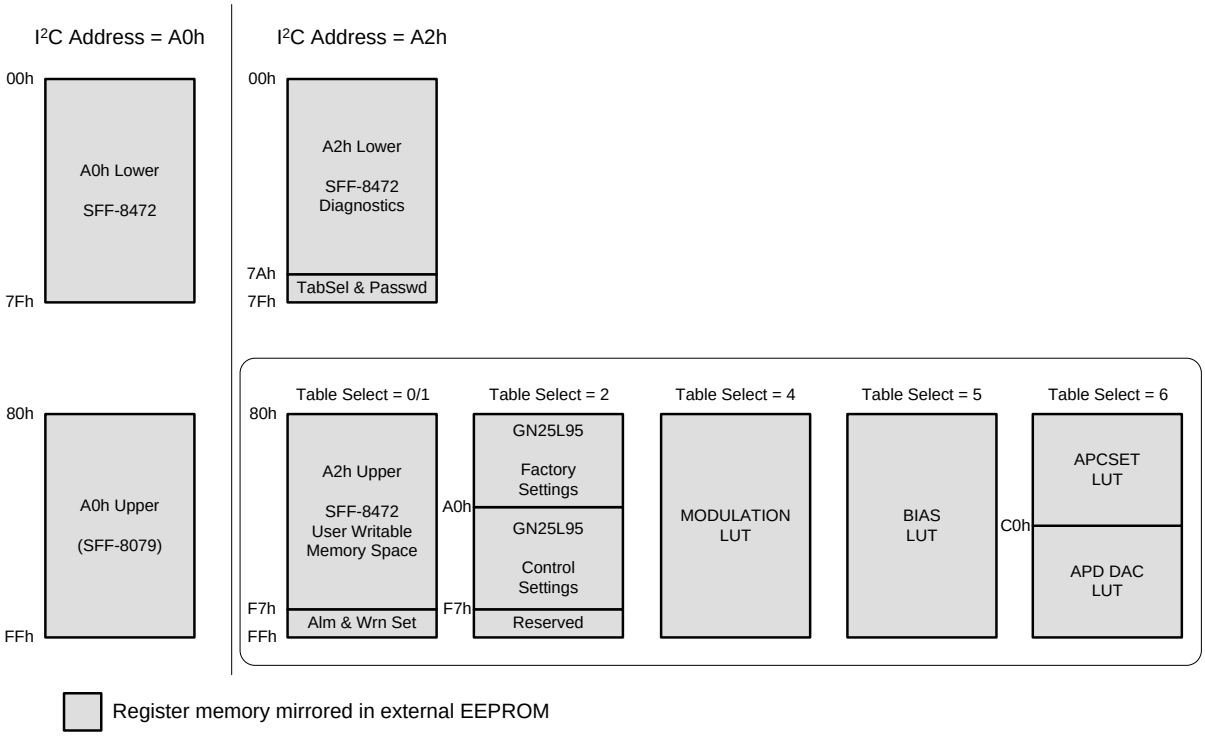


Figure 13 – GN25L95 EEPROM backed-up memory addresses

External MCU mode

The GN25L95 can be interfaced with an external microcontroller (MCU) if the user wishes to provide additional functionality beyond that offered by the GN25L95 state machine controller.

To select this mode of operation the user should connect the EE_SDA and EE_SCL pins to ground.

On power-up the GN25L95 simply waits for the external MCU to load the GN25L95 control settings via the main I^2C host interface. All control and settings data is stored on the external MCU and the SFF-8472 functionality is implemented in the MCU.

The GN25L95 automatically holds the SOFT_TX_DISABLE bit high until the MCU resets this bit to enable normal transmitter operation.

In MCU mode the GN25L95 only responds to I^2C device address A2h.

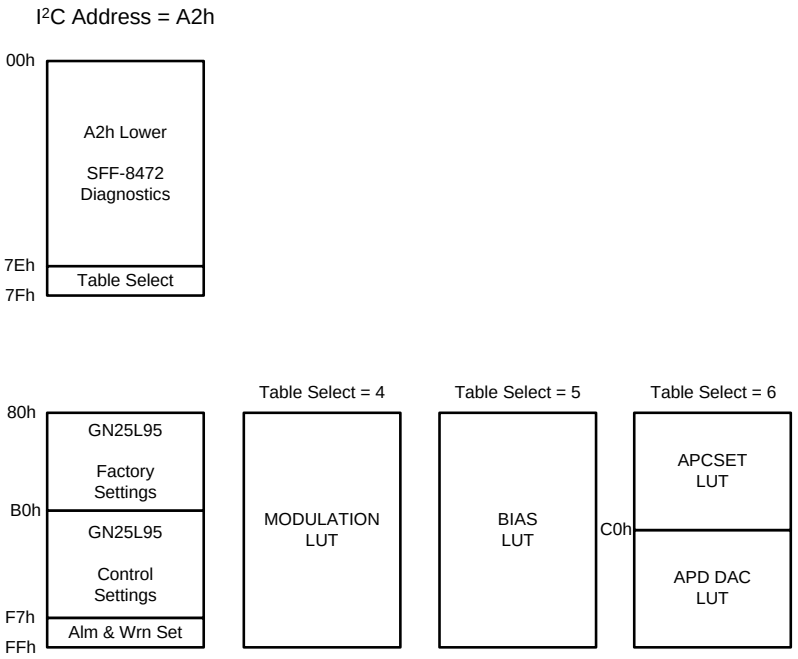


Figure 14 – GN25L95 MCU Mode Register Addresses

Start-up Sequence

The start-up sequence for the GN25L95 is shown in the flow chart diagram below.

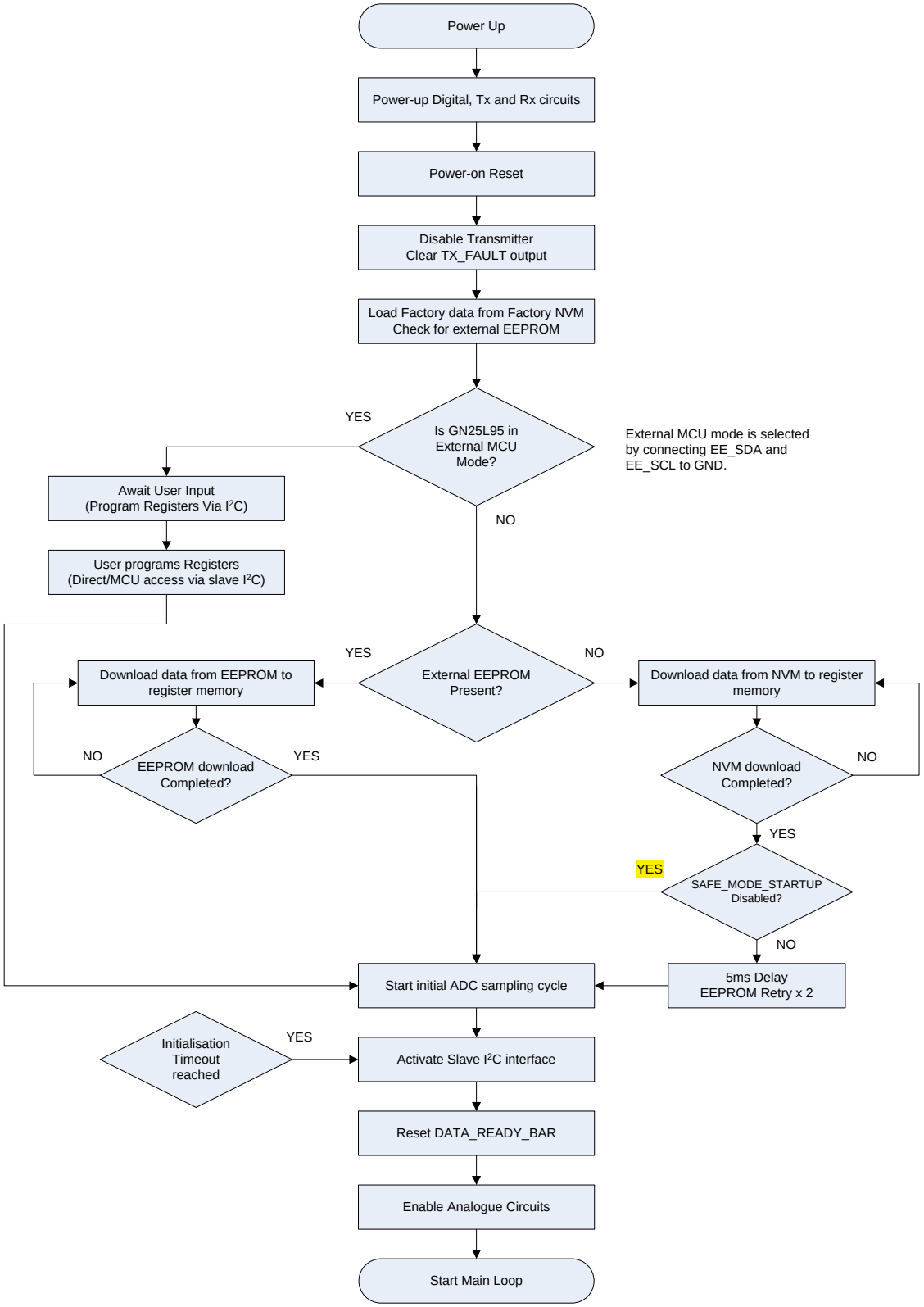


Figure 15 – GN25L95 Power-on Control Loop

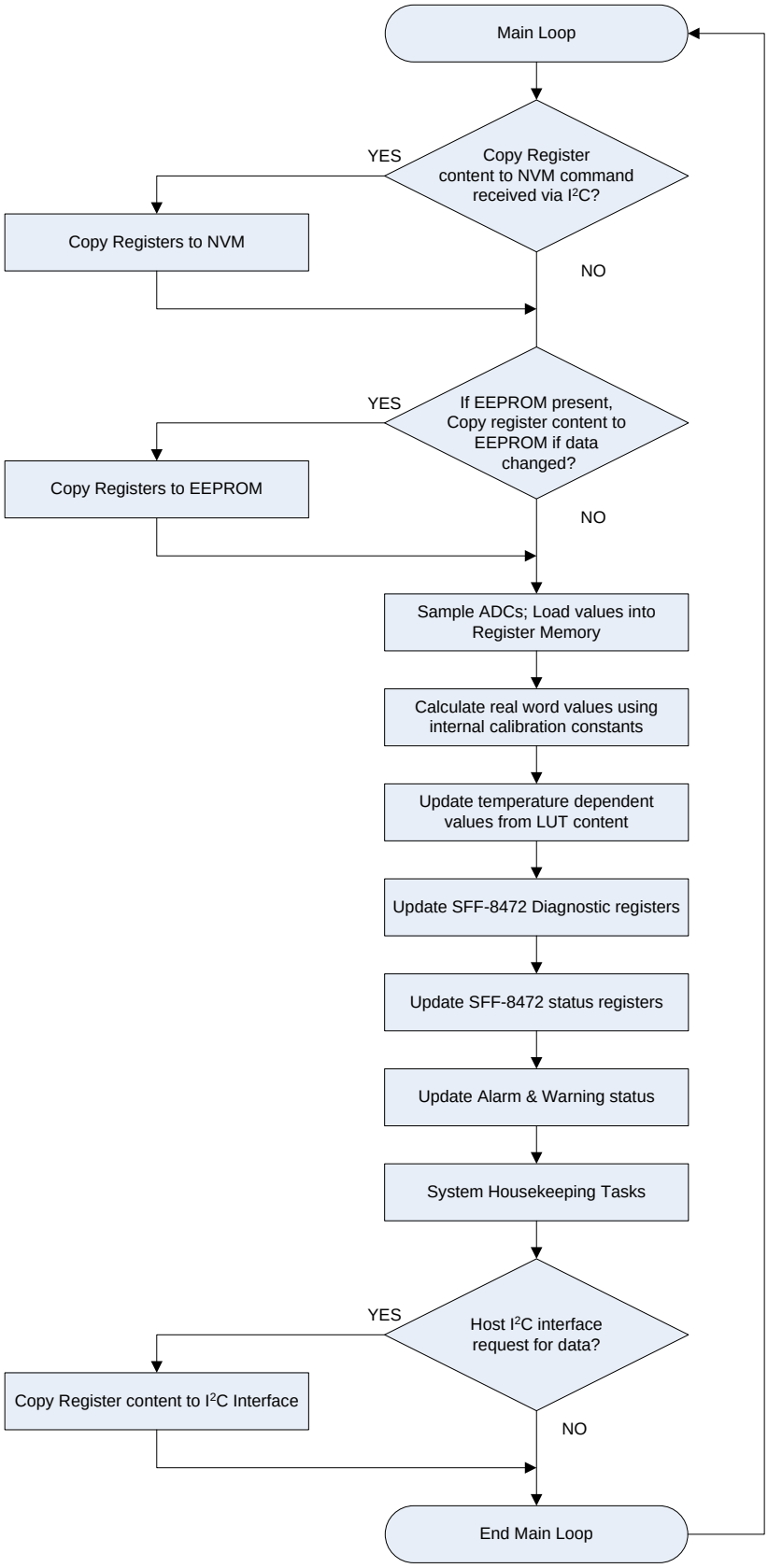


Figure 16 – GN25L95 Main Control Loop

Transmitter Features

The GN25L95 transmitter consists of an internally biased differential input stage that can be DC coupled or AC coupled depending on the mode of operation, a temperature compensated modulation current output driver, a burst mode controlled high current bias driver and a burst control input stage. The transmitter also contains sophisticated eye safety circuitry to comply with single point failure transmitter faults as per IEC-60825 requirements.

Transmitter Input Stage

The transmitter data inputs and the burst enable control inputs are high speed internally biased differential inputs that are typically externally terminated with PECL or CML loads.

The transmitter data input stage can be either DC coupled (burst-mode operation) or AC coupled (standard CW transceivers) and is internally biased. Input termination may be required for CML or LVPECL applications. The input stage consists of a limiting gain block that allows the GN25L95 to work with a range of input signals from 200 mVpp to 2400 mVpp including standard LVPECL inputs.

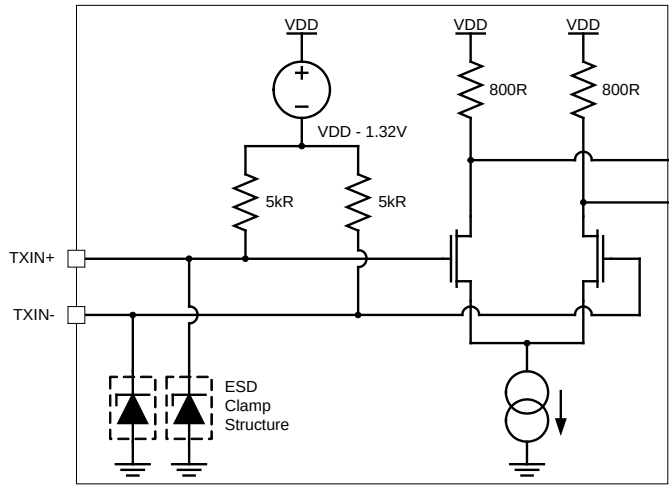


Figure 17 – GN25L95 Transmitter Data Input Internal Biasing

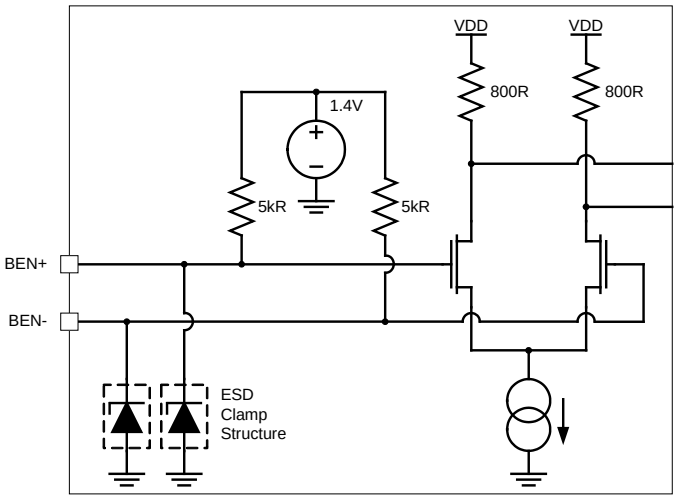


Figure 18 – GN25L95 Transmitter Burst Enable Input Internal Biasing

The burst enable inputs can be used either differentially or single ended depending on the termination scheme being used. The diagrams below indicate the correct termination methods for LVPECL, CML and LVTTL signalling schemes. The burst enable inputs should always be DC coupled for correct operation.

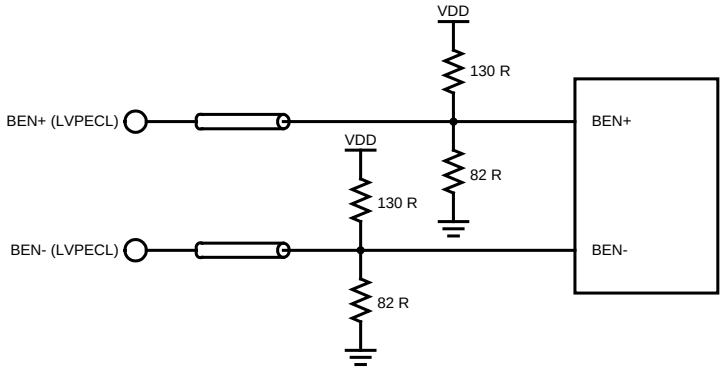


Figure 19 – GN25L95 BEN input termination: Differential LVPECL

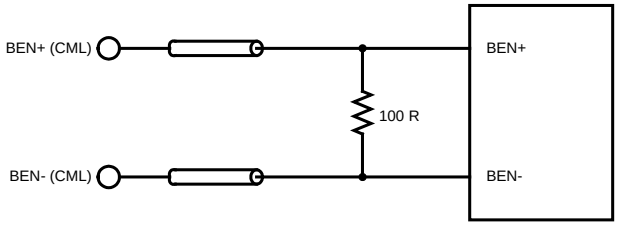


Figure 20 – GN25L95 BEN input termination: Differential CML

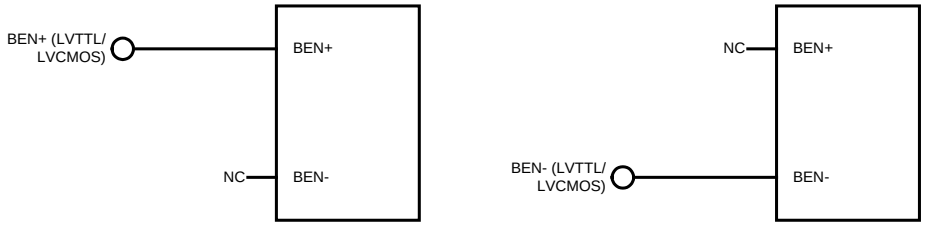


Figure 21 – GN25L95 BEN input termination: Single Ended LVTTL/LVCMOS

The BEN inputs can be configured so that if left floating with no data applied then the default state of the transmitter bias and modulation currents can be on or off.

Semtech recommends adding a 220 Ω series resistor between the BEN input pins and the host interface to protect from electrical overstress events during optical transceiver manufacture.

For electrical evaluation and characterization of the GN25L95 transmitter modulation outputs the test circuit shown in Figure 22 below is used.

The test circuit provides a DC coupled evaluation environment for the LASER+ and LASER- high speed modulation outputs with characteristic load impedance of 10 Ω. When measuring the output rise and fall times the differential output capacitor C_{DIFF} is not fitted. When output overshoot is being measured, the differential output capacitor CDIFF is fitted to represent a typical laser capacitance.

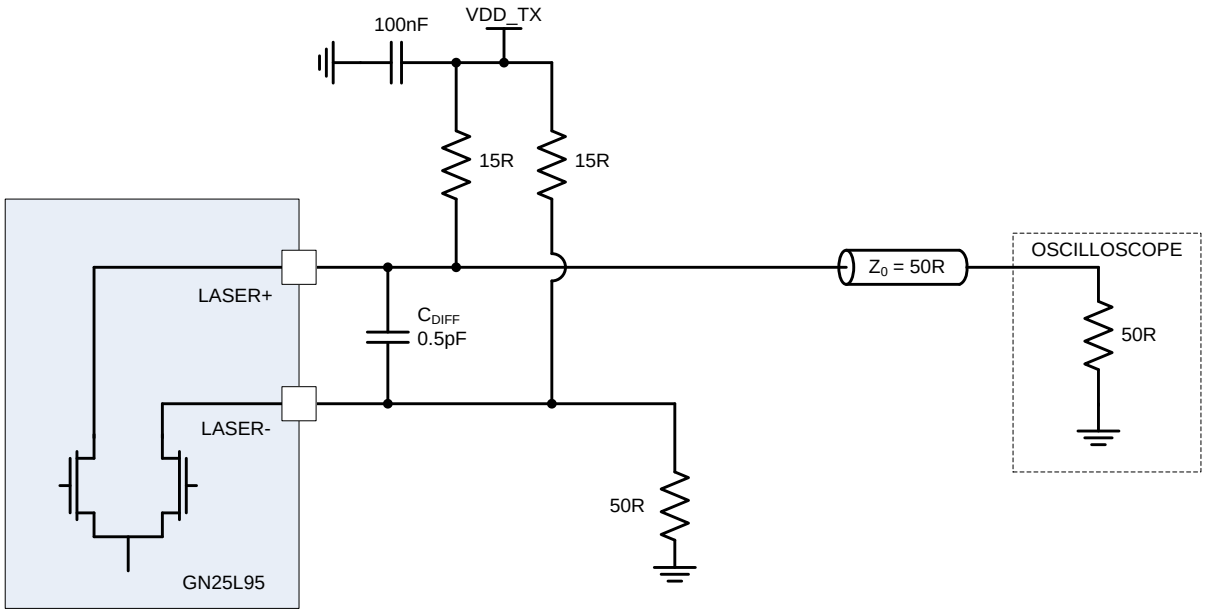


Figure 22 – GN25L95 Transmitter high speed modulation output evaluation circuit

Modulation Stage

The modulator stage comprises of a switched current source capable of switching up to 90 mA of modulation current through either the LASER+ or LASER- outputs. The modulation current is set digitally and is temperature compensated for laser efficiency changes over temperature and lifetime.

For correct burst-mode operation and fast laser turn on times the laser modulation outputs must be DC coupled to a common anode laser. The outputs can be either DC or AC coupled for non-burst applications such as standard SFP modules.

In the absence of input data, or the data inputs floating, if the TX_MOD_SPLIT bit is set then the laser outputs will sink 50% of the modulation current through each pin, LASER+ and LASER- otherwise it will be zero.

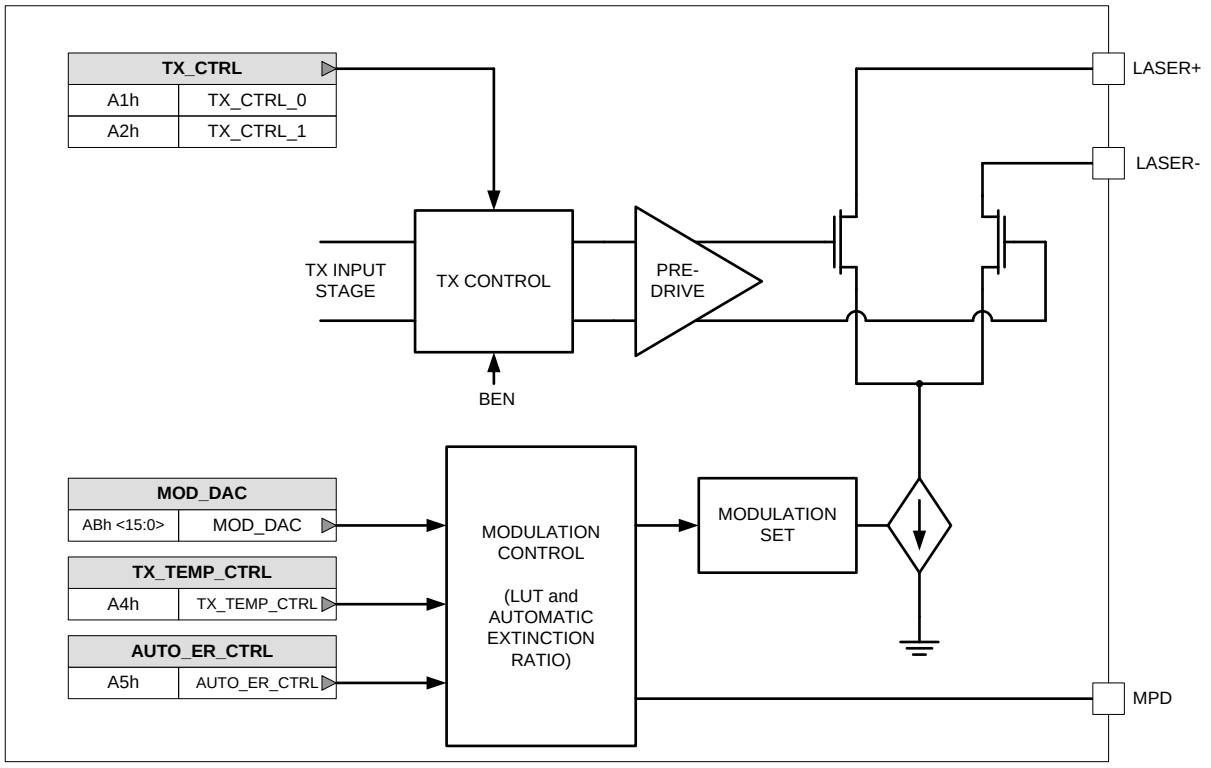


Figure 23 – GN25L95 Transmitter Modulation Stage Diagram

The GN25L95 modulator outputs are driven by the transmitter differential data input signal (TXIN+/TXIN-) and also controlled by the burst control inputs (BEN+/BEN-). The LASER+ output will sink modulation current if a logic one is transmitted through the TXIN data path and the BEN control path is enabled high. Use the TX_MOD_STEER bit to invert the modulation current steering for flexible PCB design. The modulation output crossing point can be adjusted using the TX_CROSSING control.

The GN25L95 modulation current can be programmed directly and simply, using only the MOD_DAC register. This will apply a constant modulation current depending on the register value set and detailed under the MOD_DAC register section.

The modulation current can be controlled by two other on-chip control methods: (1) A temperature indexed Modulation Look-up Table or (2) Automatic Extinction Ratio control that uses closed loop feedback of the monitor photodiode current to generate an error signal to set and maintain a constant transmitter extinction ratio over temperature and lifetime operating conditions of the attached laser. Both of these modulation current control methods are described in detail in this chapter.

MOD_DAC

The MOD_DAC register is a 16-bit register that controls a 10-bit DAC. Therefore only the upper 10 bits of the register are actually used to program the DAC, the remaining lower 6 bits should be set to zero. The MOD_DAC register is actually programmed using two 8-bit registers, MOD_DAC MSB and MOD_DAC LSB, so only the upper 2 bits of MOD_DAC LSB are utilised.

The contents of both MOD_DAC MSB and MOD_DAC LSB are only transferred to the DAC when MOD_DAC LSB is written. This is done to ensure that all bias DAC updates occur in a single step, even when a new value requires both registers to be changed.

Lower Range	Upper Range	MOD_DAC MSB (ABh)								MOD_DAC LSB (ACh)							
0000h	FFC0h	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.8 mA	103.1 mA	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0

Table 9 – MOD_DAC 16-bit register mapping

The MOD_DAC register controls the modulation current via a 10-bit DAC, which has four possible modes of operation selectable via the MOD_DAC_SETUP bits of the AUTO_ER_CTRL register. The available modes are shown in the table below.

MOD_DAC_SETUP[1:0] (A5h bits 3:2)	DAC Mode
00 (default)	100mA Linear
01	25mA Linear
10	75mA Linear
11	100mA Pseudo-Logarithmic

Table 10 – MOD_DAC modes

The modulation current follows the relationship described by one of the four equations below:

100mA Linear Mode: Modulation Current (mA) = (MOD_DAC + 8) * 0.1mA
25mA Linear Mode: Modulation Current (mA) = (MOD_DAC + 8) * 0.025mA
75mA Linear Mode: Modulation Current (mA) = (MOD_DAC + 8) * 0.075mA
100mA Pseudo-Logarithmic Mode:
Modulation Current (mA) =
0.800mA + (MOD_DAC * 0.0267mA) [0 - 255]
7.627mA + ((MOD_DAC – 256) * 0.0533mA) [256 - 511]
21.280mA + ((MOD_DAC – 512) * 0.1067mA) [512 - 767]
48.587mA + ((MOD_DAC – 768) * 0.2133mA) [768 - 1023]

The chart below shows actual modulation current plotted against the MOD_DAC register values.

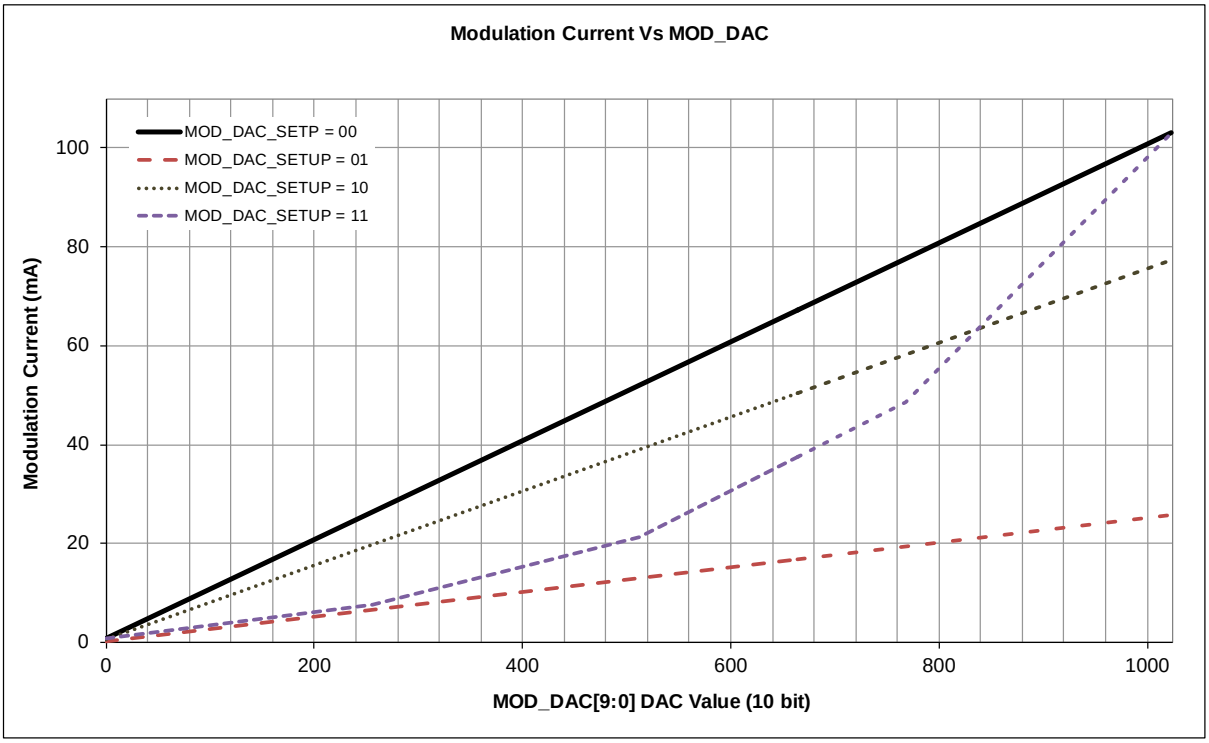


Figure 24 – GN25L95 MOD_DAC Register Value versus Modulation Current Output

The modulation output drive stage is rated to 90mA but the DAC allows modulation currents up to 103.1mA to be programmed but this is not recommended for long-term operation and beyond 90mA will not support laser forward voltages greater than 1.5V.

The modulation current can be directly programmed via the host I^2C interface by setting register MOD_DAC.
When the GN25L95 is used in Automatic ER mode or LUT mode, the current MOD_DAC value being set by the Auto ER loop or LUT can be read back from the MOD_DAC register by reading this register over the slave I^2C interface. Writing to the MOD_DAC register when the GN25L95 is in Auto ER mode or LUT mode will have no effect on the modulation current setting.

Modulation LUT

A temperature indexed modulation current Look-Up Table (LUT) is available for use at address A2h Table 4. The LUT is enabled by setting bit MOD_LUT_EN in register TX_TEMP_CTRL.

The modulation LUT contains 64 locations for MOD_DAC values that are temperature indexed in 2.5°C steps over the internal junction temperature range of -40°C to 120°C. The GN25L95 uses the calibrated temperature value to index the LUT.

The GN25L95 can also be set to interpolate between each of the 64 temperature locations so that the MOD_DAC is actually updated with a new temperature dependent modulation current value every 1.25°C. This effectively turns the 64 location LUT into a 128 location LUT. This feature can be enabled by setting bit MOD_LUT_INTERPOL in register TX_TEMP_CTRL.

If the extremities of the LUT locations are exceeded by the indexing temperature, then the value used will be the first or last value in the LUT depending on which end of the LUT has been exceeded.

Automatic Extinction Ratio Control

The GN25L95 features automatic extinction ratio (AER) control of modulation current that can be programmed to set and maintain a target extinction ratio over temperature. The AER controller uses the monitor photodiode current signal and compares this against a target AER reference current to maintain the extinction ratio.

The AER control is enabled by setting bit AUTO_ER_EN in the AUTO_ER_CTRL register. The target extinction ratio is set by TARGET_ER_SET in the AUTO_ER_CTRL register.

For fast start-up of the transmitter an initial seed value for modulation current is used by the GN25L95 to set the initial modulation current. The AER controller then uses the error signal from the MPD input to obtain and maintain the target ER value. If the MOD_LUT_EN bit is set, the GN25L95 uses the content of the modulation LUT as temperature dependent initial seeds values for the AER controller. Therefore the modulation LUT should be programmed with an approximate estimate of the required modulation current over temperature to enable the fastest settling time of the AER to the desired ER. If the modulation LUT contains no data then the AER is loaded with an initial seed value of zero and the AER will take a longer period of time to search for the desired target ER value. Alternatively, if the MOD_LUT_EN bit is not set, then the AER controller uses the MOD_DAC register as the initial seed value for the modulation current. In both cases, once the AER has found the target ER, the target ER is maintained over the entire operating range until the transmitter is disabled or the GN25L95 is powered off.

If a BEN de-assert occurs whilst the AER controller is operating then the last determined modulation value is applied to the MOD_DAC on the next BEN assert.

If a TX_DISABLE or TX_FAULT event (excluding TX_FAST_SLEEP) occurs during operation of the AER controller, then on reactivation of the transmitter, the AER controller will re-start and load a new modulation current seed value from the modulation LUT (if MOD_LUT_EN is enabled) or directly from the MOD_DAC register itself.

If no data is present at the TXIN data inputs during GN25L95 power-up and initialisation then the AER function will not initiate until data is present at the TXIN inputs.

MOD_MAX

The MOD_MAX function is provided to allow the user to set a maximum modulation current limit beyond which a TX_FAULT condition will be asserted. The MOD_MAX function provides an 8-bit control for setting the upper modulation current. The GN25L95 is designed to produce modulation currents up to 90 mA.

If MOD_MAX is set to FFh then the GN25L95 will apply no upper limit to the modulation current output stage.

In the case where the MOD_MAX limit is exceeded then a latched TX_FAULT will assert and the transmitter bias and modulation currents will be disabled until the TX_FAULT condition is reset by toggling the TX_DISABLE input. If the modulation current persists in exceeding the MOD_MAX limit then the TX_FAULT will repeatedly assert until the modulation current falls below the MOD_MAX limit.

If the NOFAULT_MODMAX bit in the MD_MAX register is set, then the modulation current will be limited to the value set by MOD_MAX, but no fault will be generated.

The MOD_MAX function works by checking and limiting the 8 most-significant bits of the 10-bit MOD_DAC value. The MOD_MAX register value can therefore be multiplied by 4 to find the corresponding current limit on the MOD_DAC response profile, which in turn depends on the MOD_DAC_SETUP register control. For example, in 100mA Linear Mode, the current limit can be calculated using the following formula:

Modulation Current Maximum (mA) = ((MOD_MAX * 4) + 8) * 0.1mA

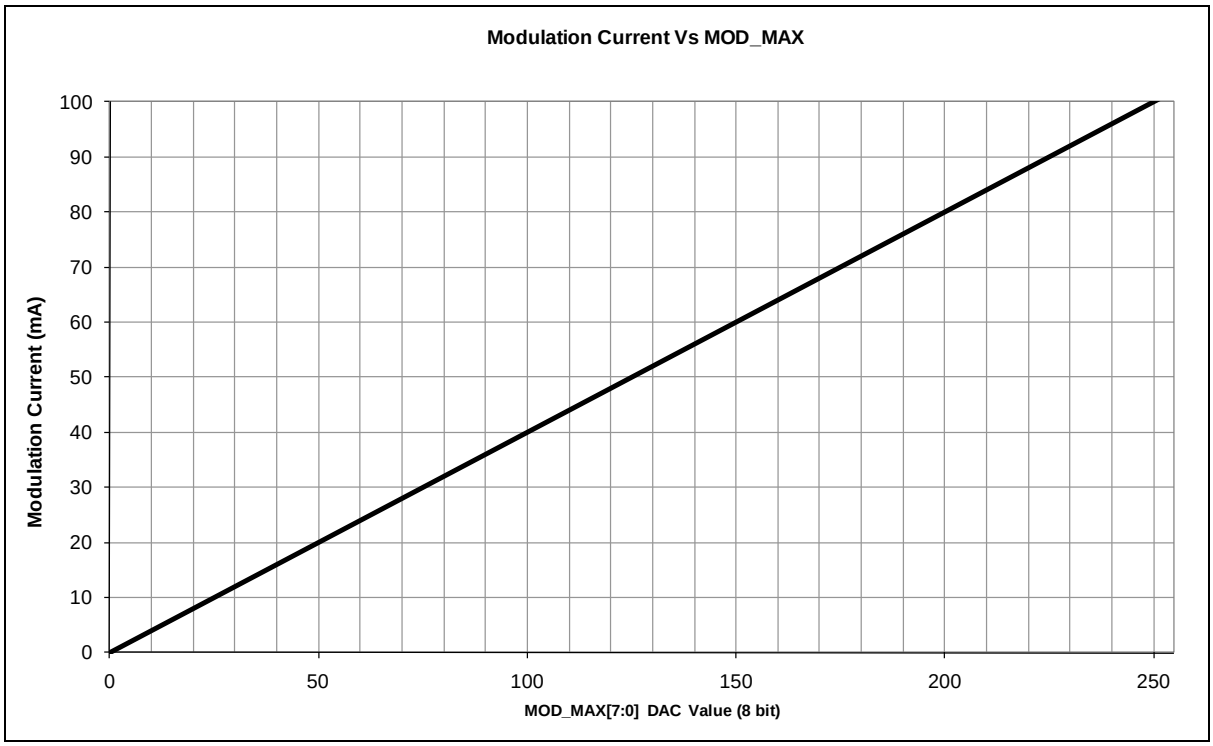


Figure 25 – GN25L95 Modulation Current Maximum Limit Vs BIAS_MAX Code

Active Back Termination

The LASER+ and LASER- modulator outputs have programmable back termination to improve the optical output performance by optimising the matching between the GN25L95 and laser diode component. The back termination helps to manage the overshoot in the modulated current switched through the laser diode by minimizing reflections.

The back termination can be either passive or active and is selected using the BACK_TERM_TYPE control bit. The default setting of '0' applies a passive RC snubbing termination network to the LASER+ and LASER- outputs. Setting BACK_TERM_TYPE to '1' applies active back termination – in this case the RC snubbing network is actively driven rather than terminated to ground. The user can empirically determine which setting is preferable for the laser being driven.

Several levels of back termination can be applied to optimise the modulator output for a particular laser device as shown in the table below. These are controlled using the BACK_TERM setting.

BACK_TERM <2:0> (A2h TX_CTRL_1 Bits 3:1)				
BACK_TERM <2>	**BACK_TERM <1>**	**BACK_TERM <0>**	**R (Ω)**	**C (pF)**
0	0	0	-	-
0	0	1	240	4.9
0	1	0	120	4.9
0	1	1	80	4.9
1	0	0	60	4.9
1	0	1	48	4.9
1	1	0	40	4.9
1	1	1	34	4.9

Table 11 – Modulator Active Back Termination Settings

In active back termination mode, the voltage amplitude of the active drive signal is proportional to the modulation current, the proportional constant being controllable via the VABTSET register according to the following formula:

VABT = I_MOD * 49.2 * (R[0] + 2*R[1] + 4*R[2] + 8*R[3]) / (1 + 3*R[4] + 12*R[5] + 16*R[6] + 32*R[7])

Where VABT is the active drive signal amplitude in Volts, I_MOD is in Amps, and R[0] to R[7] represent bits 0 to 7 of the VABTSET register.

The VABT voltage is subject to a limit of 1.3V. Care should be taken when selecting the VABTSET value that this limit will not be exceeded within the range of I_MOD current expected in the application, since this would cause a loss of proportionality between I_MOD and VABT which could result in variation of the optical eye quality.

Bias Stage

The bias stage features a digital automatic mean power control loop that sets the mean output power and maintains this power over temperature and supply voltage changes. Bias currents of up to 100 mA can be achieved. The bias stage can operate in both burst and non-burst modes as a result of the digital control loop implemented in the GN25L95. The actual bias current can be programmed directly, via the BIAS_DAC register, or indirectly by setting a reference target monitor current for the automatic power control loop to maintain by adjusting the bias current internally. A temperature indexed bias current LUT can also be used to control the bias current over temperature.

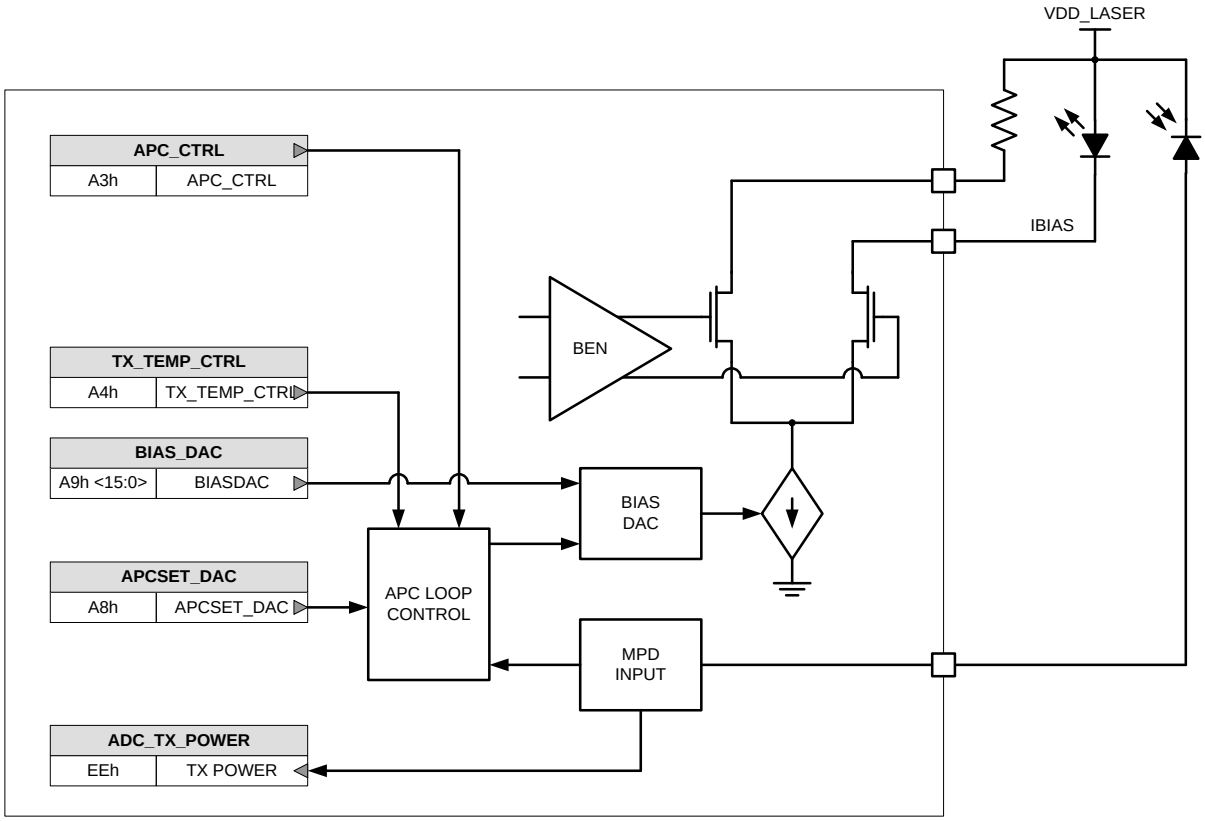


Figure 26 – GN25L95 Bias Stage Diagram

The bias stage comprises of several control registers which are detailed below.

APCSET_DAC

The APCSET_DAC register controls a pseudo logarithmic 8-bit DAC that is a piece-wise linear approximation to the exponential function:

Target Monitor Photodiode Current (µA) = 7.185µA * $2^{(APCSET/32)}$

(only valid for values above the minimum specified current of 25uA)

The APCSET_DAC register allows the user to set a target monitor photodiode current which is used during closed loop mean power feedback control. The GN25L95 internally adjusts the bias current so that the actual monitor photodiode current is equal to the target monitor photodiode current set by APCSET_DAC.

The target monitor photodiode current can be programmed up to 1800 µA as shown in Figure 27 and, as the function is logarithmic, the resolution is the same from the lowest to highest monitor current. This enables precise setting of transmitter output power even for low optical power requirements.

The APC loop is enabled by setting bit APC_EN in the TX_TEMP_CTRL register.

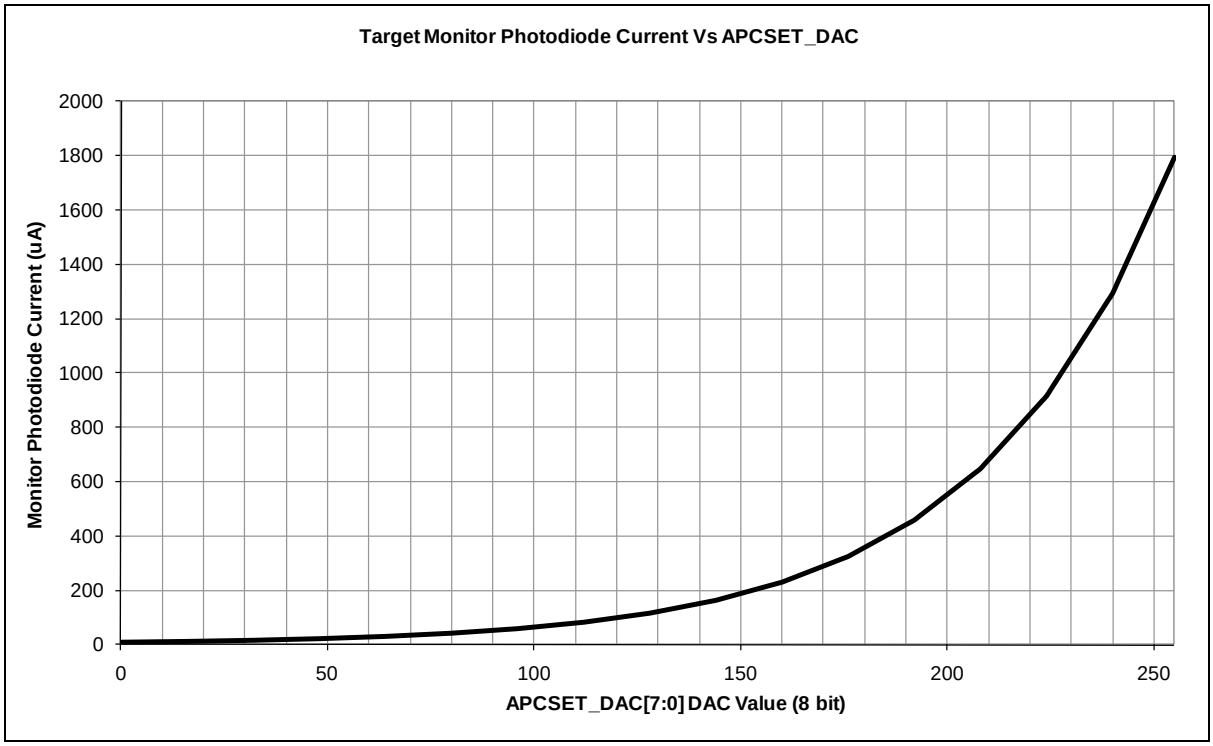


Figure 27 – GN25L95 Target Monitor Photodiode Current Vs APCSET Code

APCSET LUT

A temperature indexed APCSET current Look-Up Table (LUT) is available for use at address A2h Table 6, 80h to BFh. The LUT is enabled by setting bit APC_LUT_EN in register TX_TEMP_CTRL.

The APCSET LUT contains 64 locations for APCSET_DAC values that are temperature indexed in 2.5°C steps over the internal junction temperature range of -40°C to 120°C. The GN25L95 uses the calibrated temperature value to index the LUT.

If the extremities of the LUT locations are exceeded by the indexing temperature, then the value used will be the first or last value in the LUT depending on which end of the LUT has been exceeded.

The APCSET LUT can be used in conjunction with the APC controller to provide a temperature compensated target APCSET value. This can help to compensate for changes in optical output power caused by the effects of systematic mechanical tracking errors in the laser optical package.

BIAS_DAC

The BIAS_DAC register is a 16-bit register that controls a 10-bit DAC. Therefore only the upper 10 bits of the register are actually used to program the DAC, the remaining lower 6 bits should be set to zero. The BIAS_DAC register is actually programmed using two 8-bit registers, BIAS_DAC MSB and BIAS_DAC LSB, so only the upper 2 bits of BIASDAC LSB are utilised.

The contents of both BIAS_DAC MSB and BIAS_DAC LSB are only transferred to the DAC when BIAS_DAC LSB is written. This is done to ensure that all bias DAC updates occur in a single step, even when a new value requires both registers to be changed.

Lower Range	Upper Range	BIAS_DAC MSB (A9h)								BIAS_DAC LSB (AAh)							
0000h	FFC0h	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.8 mA	103.1 mA	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0

Table 12 – BIAS_DAC 16-bit register mapping

The BIAS_DAC register controls the laser bias current via a 10-bit DAC, which has four possible modes of operation selectable via the BIAS_DAC_SETUP bits of the AUTO_ER_3 register. The available modes are shown in the table below.

BIAS_DAC_SETUP[1:0] (B0h AUTO_ER_3 Bits 7:6)	DAC Mode
00 (default)	100mA Linear
01	25mA Linear
10	75mA Linear
11	100mA Pseudo-Logarithmic

Table 13 – BIAS_DAC modes

The bias current follows the relationship described by one of the four equations below:

100mA Linear Mode: Bias Current (mA) = (BIAS_DAC + 8) * 0.1mA
25mA Linear Mode: Bias Current (mA) = (BIAS_DAC + 8) * 0.025mA
75mA Linear Mode: Bias Current (mA) = (BIAS_DAC + 8) * 0.075mA
100mA Pseudo-Logarithmic Mode:

Bias Current (mA) =
0.800mA + (BIAS_DAC * 0.0267mA) [0 - 255]
7.627mA + ((BIAS_DAC – 256) * 0.0533mA) [256 - 511]
21.280mA + ((BIAS_DAC – 512) * 0.1067mA) [512 - 767]
48.587mA + ((BIAS_DAC – 768) * 0.2133mA) [768 - 1023]

Where BIAS_DAC is the actual BIAS_DAC decimal code {0 to 1023}.

When operating in APC or LUT mode, the GN25L95 internally controls the bias current using the APCSET_DAC target value or the LUT, respectively. The BIAS_DAC register is used to set the actual bias current when the APC loop is not enabled.

When the GN25L95 is used in APC mode or LUT mode, the current BIAS_DAC value being set by the APC loop or LUT can be read back from the BIAS_DAC register by reading this register over the slave I^2C interface. Writing to the BIAS_DAC register when the GN25L95 is in APC mode or LUT mode will have no effect on the current bias current setting.

Figure 28 shows actual bias current output plotted against BIAS_DAC values.

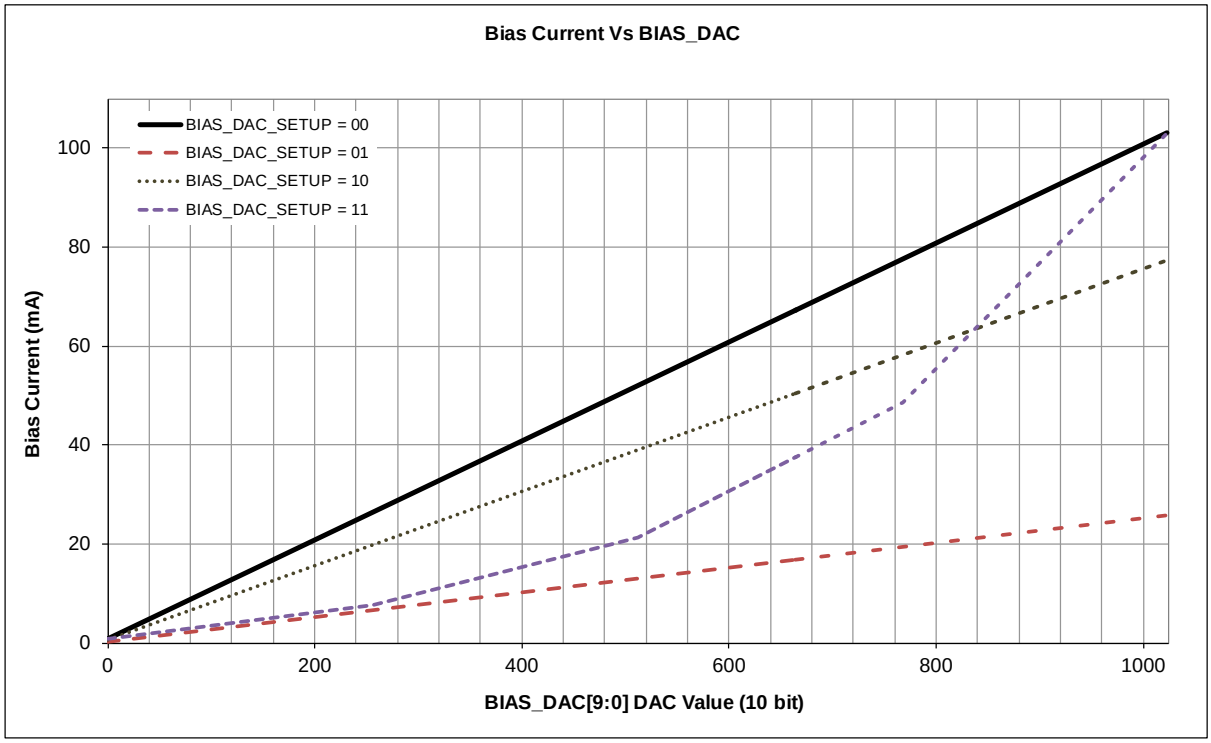


Figure 28 – GN25L95 Bias Current Vs BIAS_DAC Code

Bias LUT

A temperature indexed bias current Look-Up Table (LUT) is available for use at address A2h Table 5. The LUT is enabled by setting bit BIAS_LUT_EN in register TX_TEMP_CTRL.

The bias LUT contains 64 locations for BIAS_DAC values that are temperature indexed in 2.5°C steps over the internal junction temperature range of -40°C to 120°C. The GN25L95 uses the calibrated temperature value to index the LUT.

The GN25L95 can also be set to interpolate between each of the 64 temperature locations so that the BIAS_DAC is actually updated with a new temperature dependent bias current value every 1.25°C. This effectively turns the 64 location LUT into a 128 location LUT. This feature can be enabled by setting bit BIAS_LUT_INTERPOL in register TX_TEMP_CTRL.

If the extremities of the LUT locations are exceeded by the indexing temperature, then the value used will be the first or last value in the LUT depending on which end of the LUT has been exceeded.

Burst Control Stage

The GN25L95 features a sophisticated burst controller that allows the automatic mean power loop to respond quickly to burst enable inputs and turn the bias and modulation currents on in less than 12.8 ns.

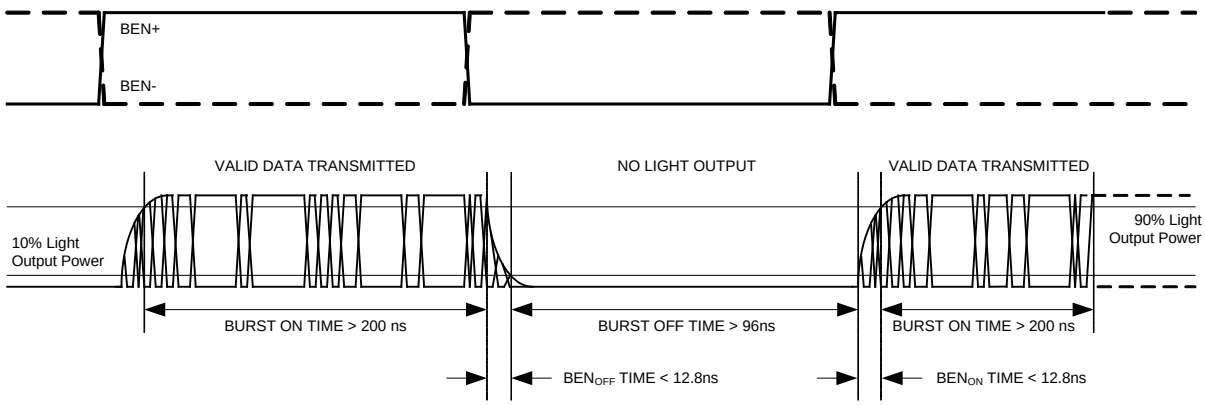


Figure 29 – Burst Control Timing

The burst controller also features a fast start-up algorithm that can set the correct laser mean power within five 200ns burst on cycles as shown in Figure 30.

The digital APC loop that provides fast start-up for burst-mode operation can be optimised for various applications using the control registers shown in Figure 26.

The APC fast start function is enabled by setting the APC_FAST_EN bit in TX_TEMP_CTRL.

If the APC controller is enabled but the fast start function is not enabled, then the APC controller will use an initial bias current value from the bias LUT or BIAS_DAC register, depending on the BIAS_LUT_EN bit, to set an initial seed for the APC loop. If there is no data present in the bias LUT or the BIAS_DAC register, then the initial seed value for bias current will be zero and therefore the APC loop will take a longer time to reach the target APCSET value.

For ‘instant on’ operation of the transmitter bias current the user can use the APC controller in conjunction with the bias LUT. If the APC_EN bit is set and the bias LUT is loaded with data that approximates the required bias current over temperature, then the APC controller will use the LUT data to set an initial bias current. The APC loop will then attain and maintain the desired target APCSET value.

APC_CLOCK_SET

APC_CLOCK_SET is a 2-bit control for the speed of the oscillator used to clock the APC loop. By default the APC_CLOCK_SET is set to the fastest programmable rate of 2.8 MHz. During APC start-up, a fast rate of 11 MHz is applied in order to meet the GPON start-up timing requirements shown in Figure 30 and to enable 200ns minimum burst-on periods.

The APC_CLOCK_SET sets the steady state APC loop sampling rate. Reducing the APC_CLOCK_SET rate effectively reduces the loop sampling rate which can be useful for low data rate applications (below 622Mbps) to reduce base line wander effects. The APC_CLOCK_SET is changed by setting the relevant bits in register APC_CTRL as shown in the table below.

Register APC_CTRL (A3h Bits 2:1)		Nominal Clock Rate
APC_CLOCK_SET <1>	APC_CLOCK_SET <0>	
X	*X*	*11 MHz*[1]
0	0	2.8 MHz
0	1	700 kHz
1	0	175 kHz
1	1	43 kHz

[1] During burst mode fast-start the APC clock is set to 11 MHz.

Table 14 – APC_CLOCK Settings

The fast start-up speed can be changed by setting LOOP START in register APC_CTRL. When LOOP START is set the APC loop will use the current APC_CLOCK rate during start-up as well as during normal steady state operation. It is not recommended to change the fast start-up rate when using the GN25L95 in burst-mode applications.

DIG_AVG_SET

DIG_AVG_SET is a 2-bit control used to set the amount of digital average applied to the APC loop. The function is enabled by setting the DIG_AVG_EN bit. The default for the GN25L95 is digital averaging disabled. When not used (i.e. default) the APC loop makes a decision to increment or decrement the bias current DAC by one bit step on every clock cycle. If the digital averaging function is enabled then the APC loop decision is taken less frequently on multiples of the APC loop clock rate as shown in the table below.

Register APC_CTRL (A3h Bits 3; 5:4))			Clock Cycles Counted	Time Constant for 2.8 MHz Clock
DIG_AVG_EN	DIG_AVG_SET <1>	DIG_AVG_SET <0>		
0	x	x	1	357 ns
1	0	0	4	1.43 µs
1	0	1	16	5.71 µs
1	1	0	64	22.8 µs
1	1	1	256	91.4 µs

Table 15 – APC Loop Digital Averaging Settings

For non-burst mode, low data rate, applications the APC loop performance can be optimised by reducing the APC clock rate using the APC_CLOCK_SET function. For burst-mode applications the APC loop performance can be optimised better by applying the full APC loop clock rate of 2.8 MHz and then using the digital averaging function DIG_AVG_SET to alter the loop response time.

ERC_AVG_SET

ERC_AVG_SET is a 2-bit control used to set the amount of digital averaging applied to the ERC loop. The function is enabled by setting the ERC_AVG_EN bit. The default for the GN25L95 is ERC digital

averaging disabled. When not used (i.e. default) the ERC loop makes a decision to increment or decrement the bias current DAC by one bit step on every clock cycle. If the ERC digital averaging function is enabled then the ERC loop decision is taken less frequently on multiples of the ERC loop clock rate as shown in the table below.

Register AUTO_ER_1 (A6h Bits 5; 7:6)			Clock Cycles Counted	Time Constant for 2.8 MHz Clock
ERC_AVG_EN	ERC_AVG_SET <1>	ERC_AVG_SET <0>		
0	x	x	1	357 ns
1	0	0	4	1.43 µs
1	0	1	16	5.71 µs
1	1	0	64	22.8 µs
1	1	1	256	91.4 µs

Table 16 – ERC Loop Digital Averaging Settings

For non-burst mode, low data rate, applications the ERC loop performance can be optimised by reducing the APC clock rate using the APC_CLOCK_SET function (the ERC loop shares the same sampling clock as the APC loop). For burst-mode applications the ERC loop performance can be optimised better by applying the full APC loop clock rate of 2.8 MHz and then using the digital averaging function ERC_AVG_SET to alter the loop response time.

APC Fast Start-up Algorithm

The APC fast start-up algorithm is intended to be used with either the modulation LUT or automatic ER control. In both cases the modulation LUT should contain valid modulation LUT data for optimum start-up times. In automatic ER mode the modulation LUT can be disabled. In this case the fast start algorithm will use the programmed MOD_DAC value as its seed.

The GN25L95 uses a four stage fast start-up algorithm to enable the transmitter output to reach the desired optical output conditions within GPON timing requirements. The four stages are shown in Figure 30 and described below in detail.

- Step 1: The bias current is set to an initial value. This initial value can either be provided by the Bias LUT, the Modulation LUT or the BIAS_DAC register. The user can choose whether to use the Bias LUT or Modulation LUT by setting APC_FAST_VAL. If the bias LUT is used then the current temperature indexed bias value is used as a seed for the fast start algorithm. If the modulation LUT is used then the current temperature indexed modulation value x0.5 is used as a seed for the fast start algorithm.

- Step 2: The bias current is increased or decreased by incrementing or decrementing the BIAS_DAC in proportion to its current value, as defined in COUNT_INC for each clock period.

- Step 3: Once the ramp phase has incremented or decremented the bias current such that the actual monitor current has crossed the target monitor current, set by APCSET_DAC, then a binary search phase is initiated. The binary search alters the bias current to achieve an actual monitor current that is within one bit value of the target monitor current.

- Step 4: The final stage is APC loop integration mode. The APC loop samples the monitor current at a loop clock rate defined by APC_CLOCK_SET and makes a decision on the sampled monitor current to increment or decrement the BIAS_DAC value in order to maintain the monitor current at the target value defined in the APCSET_DAC register.

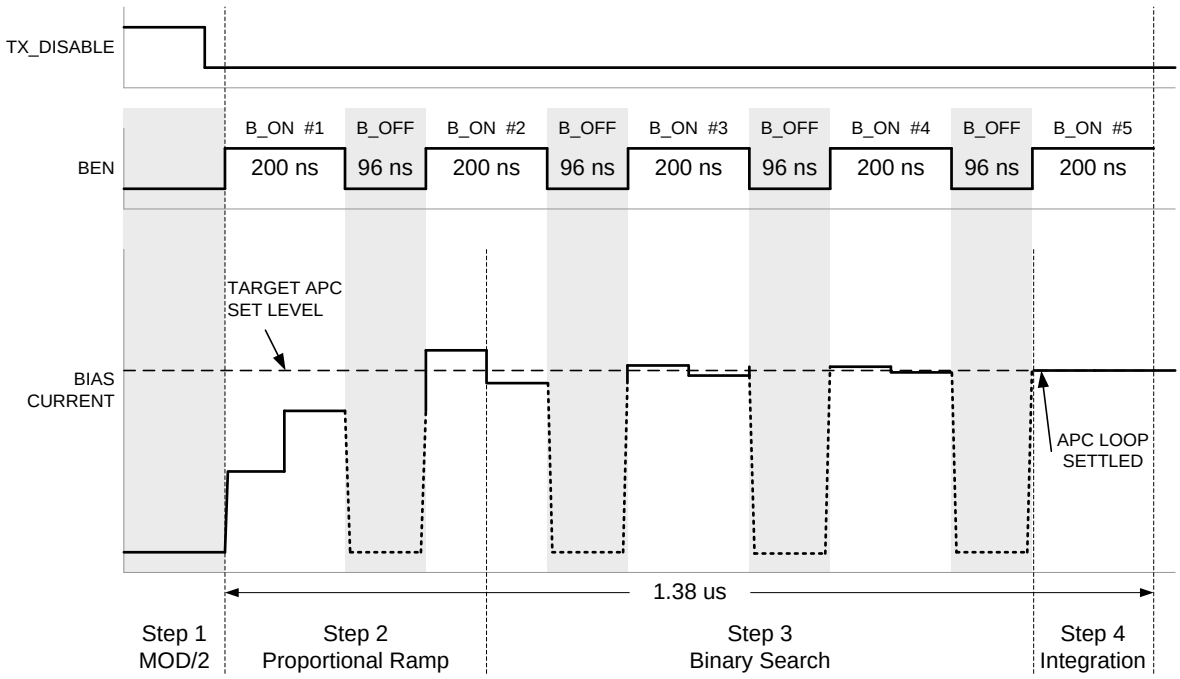


Figure 30 – APC Loop Start-Up Timing in Burst Mode

COUNT_INC

The COUNT_INC function is a 2-bit control for adjusting the step size of the bias current during the linear ramp phase of the fast start-up algorithm as shown in Figure 30. The COUNT_INC control is located in the APC_CTRL register.

The COUNT_INC function is used to change the ramp step size in stage 2 of the fast start-up algorithm. The default value is 1/32 and means that the BIAS_DAC will be incremented or decremented by 1/32 of the current BIAS_DAC value for each ramp step during the ramp stage. Larger step sizes can be programmed as shown in the table below.

Register APC_CTRL (A3h Bits 7:6)		Step Size
COUNT_INC <1>	COUNT_INC <0>	
0	0	1/32 (default)
0	1	1/16
1	0	1/8
1	1	1/4

Table 17 – COUNT_INC Setting Values

BIAS_MAX

The BIAS_MAX function is provided to allow the user to set a maximum bias current limit beyond which a TX_FAULT condition will be asserted. The BIAS_MAX function provides an 8-bit control for setting the upper bias current. The GN25L95 is designed to produce bias currents up to 100 mA.

If BIAS_MAX is set to FFh then the GN25L95 will apply no upper limit to the bias current output stage.

In the case where the BIAS_MAX limit is exceeded then a latched TX_FAULT will assert and the transmitter bias and modulation currents will be disabled until the TX_FAULT condition is reset by toggling the TX_DISABLE input. If the bias current persists in exceeding the BIAS_MAX limit then the TX_FAULT will repeatedly assert until the bias current falls below the BIAS_MAX limit.

If the NOFAULT_BIASMAX bit in the MD_MAX register is set, then the bias current will be limited to the value set by BIAS_MAX, but no fault will be generated.

The BIAS_MAX function works by checking and limiting the 8 most-significant bits of the 10-bit BIAS_DAC value. The BIAS_MAX register value can therefore be multiplied by 4 to find the corresponding current limit on the BIAS_DAC response profile, which in turn depends on the BIAS_DAC_SETUP register control. For example, in 100mA Linear Mode, the current limit can be calculated using the following formula:

Bias Current Maximum (mA) = ((BIAS_MAX * 4) + 8) * 0.1mA

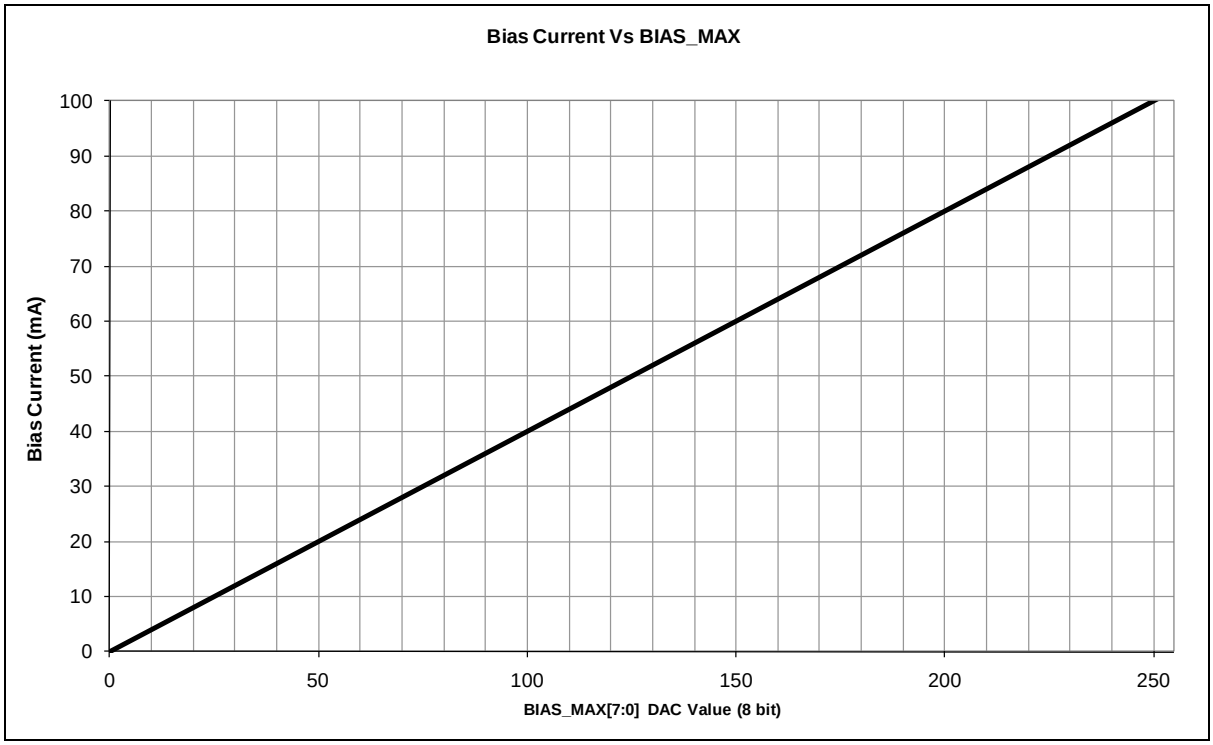


Figure 31 – GN25L95 Bias Current Maximum Limit Vs BIASMAX Code

MD_MAX

The MD_MAX function is provided to allow the user to set a maximum monitor photodiode current limit beyond which a TX_FAULT condition will be asserted. The MD_MAX function provides a 6-bit control for setting the upper monitor photodiode current. The GN25L95 is designed to operate with monitor photodiode currents up to 1800 µA. If the MD_MAX register is set to FFh then no limit is applied and the monitor current could go above 1800 µA, which is outside of the GN25L95 operating specification.

To set the upper limit of MD_MAX to the maximum protected limit of 2016 µA, program register MD_MAX to value F8h.

In the case where the MD_MAX limit is exceeded then a latched TX_FAULT will assert and the transmitter bias and modulation currents will be disabled until the TX_FAULT condition is reset by toggling the TX_DISABLE input. If the monitor current persists in exceeding the MD_MAX limit then the TX_FAULT will repeatedly assert until the monitor current falls below the MD_MAX limit.

The MD_MAX DAC is a 6-bit linear DAC with values as follows:

Maximum Monitor Current (uA) = 32 * (MDMAX+1)

For values of MD_MAX < 63. Where MDMAX = 63, no upper limit will be applied to the MPD current.

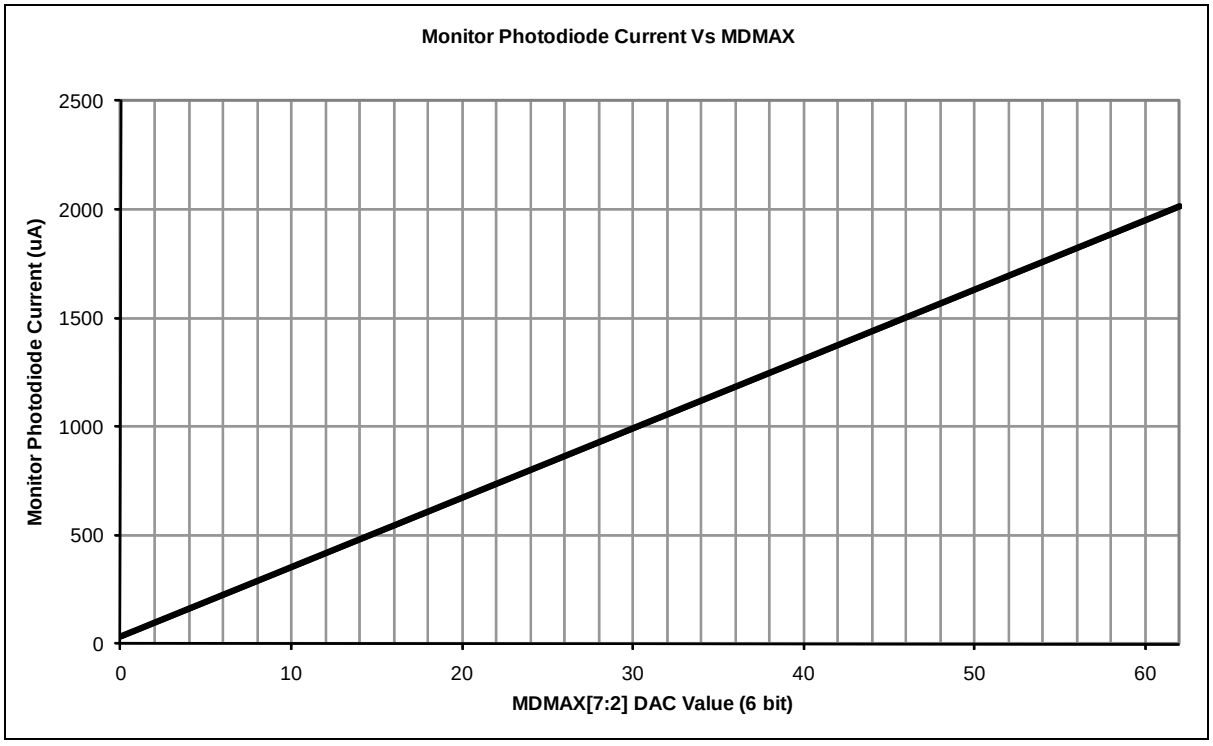


Figure 32 – GN25L95 Monitor Photodiode Current Maximum Limit Vs MDMAX Code

Transmitted Signal Detect Status Output

The GN25L95 features a TX_SD LVTTL status output pin to indicate whether the laser is currently activated or disabled. The GN25L95 uses the monitor photodiode current to ascertain whether the laser is transmitting light. The actual monitor photodiode current (I_{MPD}) is compared with a threshold which is proportional to the mean target monitor current (I_{MPD_APCSET}). The proportion can be selected via the TX_SD_MPD_THRESH register, to values between 2.5% and 20% of I_{MPD_APCSET}. If the actual monitor current is greater than the threshold current then TX_SD will be asserted. The TX_SD circuitry has been designed to cope with long runs of zeroes found in standard SONET and GPON patterns. The diagram below shows the timing associated with the TX_SD function. The polarity of the TX_SD function can be inverted by setting TX_SD_POLARITY.

As the TX_SD function is derived directly from the monitor photodiode current it will assert high as soon as a photocurrent is detected to be greater than the threshold current. Therefore during the initial average power control start-up sequence when the GN25L95 is searching for the correct mean power level, the TX_SD will be asserted as shown in Figure 34.

During power-up and initialisation the TX_SD output will remain de-asserted. The TX_SD output asserts after the transmitter is activated.

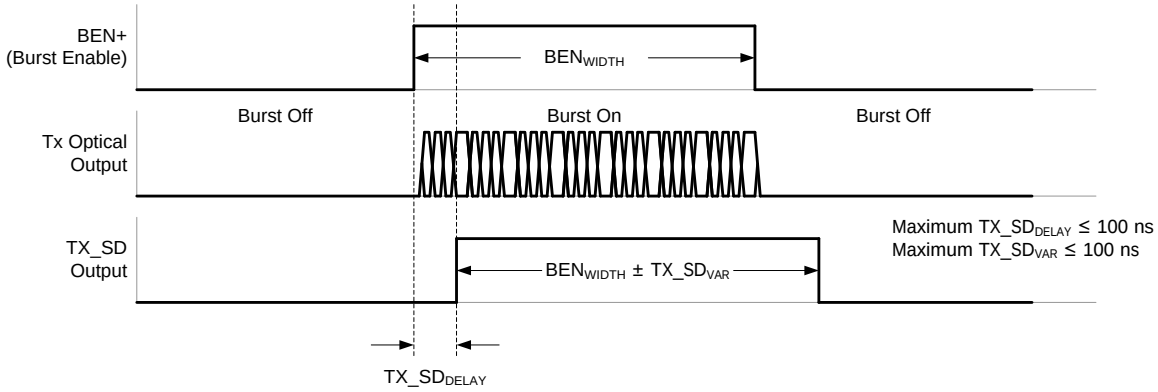


Figure 33 – GN25L95 TX_SD Timing Diagram

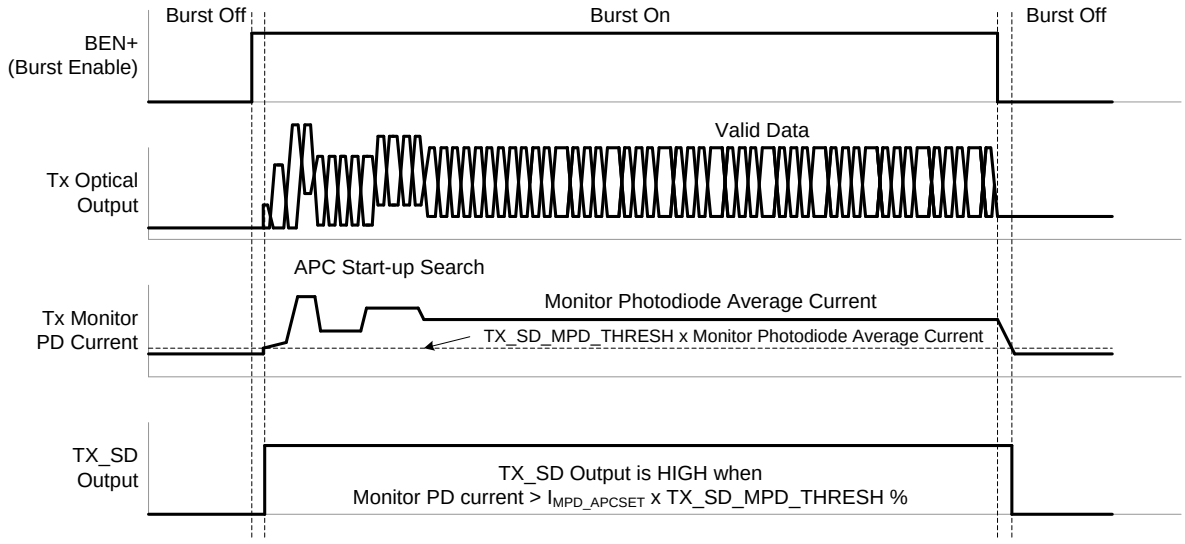


Figure 34 – GN25L95 TX_SD Function during APC Start-up Search Condition

The default stimulus for the TX_SD monitor is an internally generated copy of the monitor photodiode diode current. It is possible to configure the TX_SD to react to changes in the laser forward voltage as an alternative method of generating the TX_SD monitor. To do this, set the TX_SD_MODE bit. When using the TX_SD in this mode, the TX_SD assert threshold can be adjusted by controlling TX_SD_VF_THRESH. The table below shows these controls in detail.

TX_SD_CTRL (B1h Bits 1; 6:5)			
TX_SD_MODE	**TX_SD_VF_THRESH <1>**	**TX_SD_VF_THRESH <0>**	**TX_SD Threshold**
0	X	X	(Uses MPD current)
1	0	0	VCC – 0.6 V
1	0	1	VCC – 0.8 V
1	1	0	VCC – 1.0 V
1	1	1	VCC – 1.2 V

Table 18 – TX_SD Mode and Threshold Adjust

Rogue ONU Monitoring

Both the TX_SD status and BEN inputs are monitored by the GN25L95 and can be used to detect a rogue ONU situation along with the Tx output power. The on-chip state machine can process these conditions and provide a sophisticated Rogue ONU monitoring function.

If the internal TX_SD status monitor is asserted high for longer than the time pre-set in register TX_SD_ROGUE_TIME then the GN25L95 sets the ROGUE_ONU flag bit and the GN25L95 can also be set to indicate a hardware fault (via the TX_SD output or the TX_FAULT output) and/or disable the transmitter. Setting TX_SD_ROGUE_TIME to 0h inhibits this function.

If the BEN inputs are asserted high for a period longer than BEN_ROGUE_TIME then the GN25L95 sets the ROGUE_ONU flag bit and the GN25L95 can also be set to indicate a hardware fault (via the TX_SD output or the TX_FAULT output) and/or disable the transmitter. Setting BEN_ROGUE_TIME to 0h inhibits this function.

If the Tx Power Low Alarm flag event occurs then this can also be used to trigger a ROGUE_ONU flag and the GN25L95 can also be set to indicate a hardware fault (via the TX_SD output or the TX_FAULT output) and/or disable the transmitter. Setting the ROGUE_TXP_LO_EN bit will enable this function otherwise it will be disabled.

The host can interrogate the ROGUE_ONU and ROGUE_TXP_LO_FLAG bits to determine if a rogue ONU condition has occurred. If the ROGUE_ONU or ROGUE_TXP_LO_FLAG bits have been set then the host can reset these flags by setting ROGUE_ONU to ‘0’. Note that the ROGUE_TXP_LO_FLAG will mimic the ROGUE_ONU bit only when a Tx Power Low Alarm triggers the ROGUE_ONU flag to be set otherwise it will be set to ‘0’.

The user can setup the GN25L95 to assert a TX_FAULT upon a ROGUE_ONU condition occurring by setting the ROGUE_FAULT bit. The user can reset the latched ROGUE_ONU condition by ensuring the TX_DIS_ONU_CLR_EN bit is set and then toggling the TX_DISABLE function. The latched ROGUE_ONU condition can also be cleared by setting the ROGUE_ONU flag bit to ‘0’. Power cycling the GN25L95 will also reset the ROGUE_ONU condition.

The user can setup the GN25L95 to disable the transmitter upon a ROGUE_ONU condition occurring by setting the ROGUE_TX_DIS bit. The user can reset the latched ROGUE_ONU condition by ensuring the TX_DIS_CLR_EN bit is set and then toggling the TX_DISABLE function. The latched ROGUE_ONU condition can also be cleared by setting the ROGUE_ONU flag bit to ‘0’. Power cycling the GN25L95 will also reset the ROGUE_ONU condition.

An overview of the Rogue ONU logic is shown in Figure 35 on the following page.

A ROGUE_ONU condition is defined as either the Tx Power falling below a pre-defined level and therefore asserting an Alarm flag (as per SFF-8472 alarm conditions) or either the internal TX_SD function or BEN inputs remaining high for a period longer than that defined by the register settings shown in the table below.

Value (binary)	BEN_ROGUE_TIME (B8h <3:0>)	TX_SD_ROGUE_TIME (B8h <7:4)
0000	Inhibited	Inhibited
0001	1.64 ms	1.64 ms
0010	3.28 ms	3.28 ms
0011	6.55 ms	6.55 ms
0100	13.11 ms	13.11 ms
0101	26.21 ms	26.21 ms
0110	52.43 ms	52.43 ms
0111	104.86 ms	104.86 ms
1000	209.72 ms	209.72 ms
1001	419.43 ms	419.43 ms
1010	838.86 ms	838.86 ms
1011	1.67 sec	1.67 sec
1100	3.35 sec	3.35 sec

Table 19 – ROGUE ONU monitoring times

Once a ROGUE_ONU condition has been detected the GN25L95 can be programmed to respond in a number of ways: The TX_SD output and/or TX_FAULT outputs can be asserted high to indicate the ROGUE_ONU condition. This can be programmed to occur after a pre-determined time set by the timer functions located in A2h Lower memory, registers 72h (TIMER_SETUP) and 78h (ONU_FAULT_DELAY). The GN25L95 can also be programmed to disable the transmitter after a pre-determined time set by the timer functions located in A2h Lower memory, registers 72h (TIMER_SETUP) and 79h (TXOFF_DELAY). If the timers in A2h lower memory are set to zero, then response time will be immediate for both of these functions.

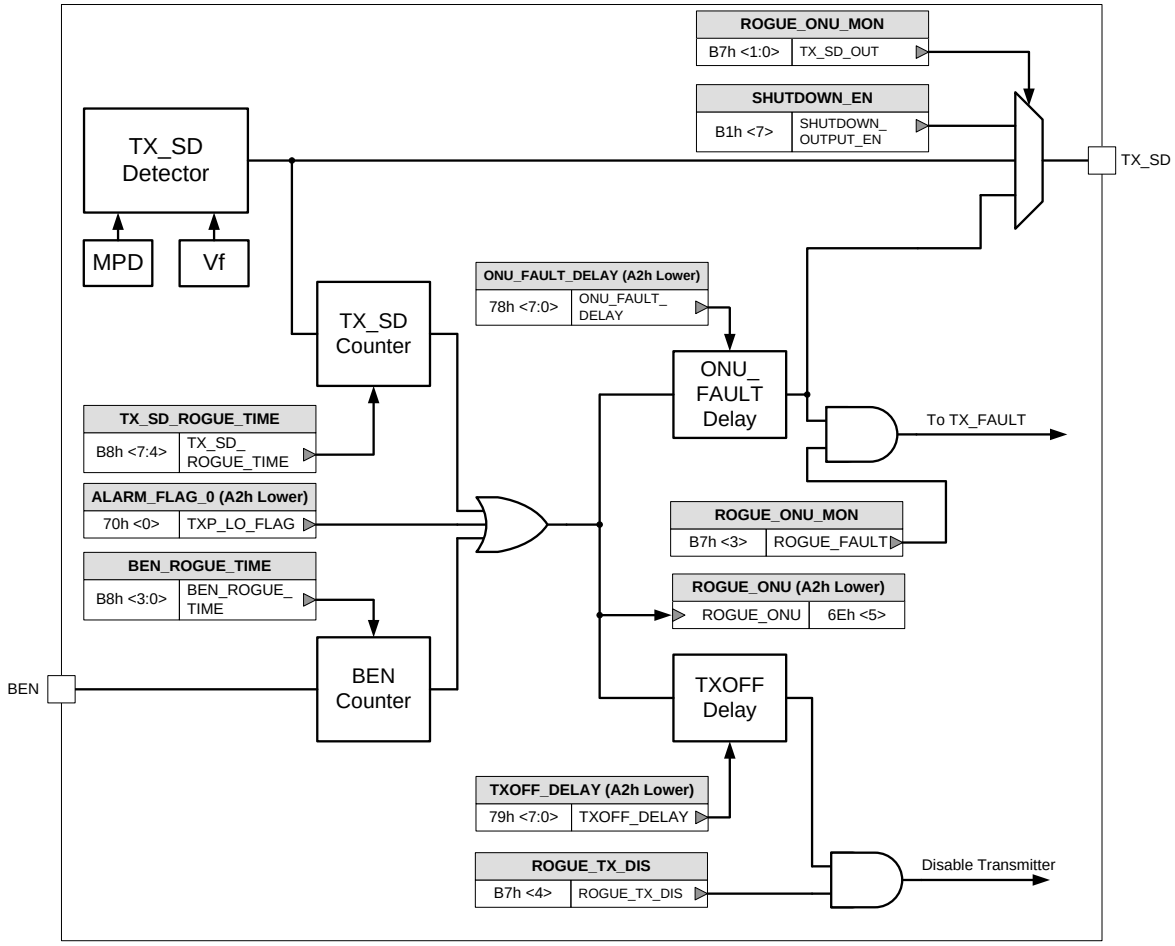


Figure 35 – GN25L95 Rogue ONU Functionality

The Rogue ONU reaction timing is detailed in the figure below.

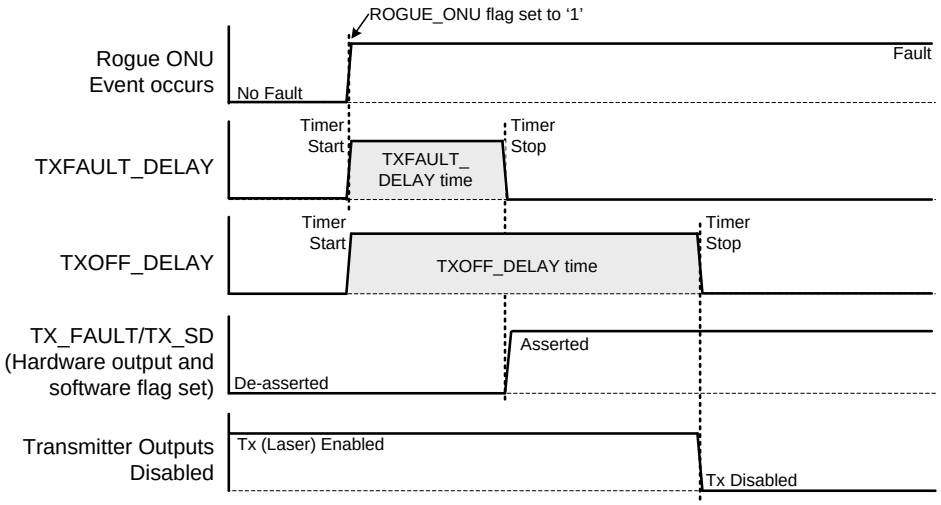


Figure 36 – GN25L95 Rogue ONU Reaction Timing

GPON Power Levelling

The GN25L95 features a GPON Power Levelling mode which can automatically reduce the transmitted output power by -3dB and -6dB as required by the ITU GPON standard. The table below shows how the GPON power levelling function operates.

Register PON_CONTROL (6Fh Bits 1:0)		GPON Power Level	MPD Current (APCSET)	Modulation Current
GPON_P <1>	GPON_P <0>			
0	0	0 dB (default)	x 1.0	x 1.0
0	1	-3 dB	x 0.5	x 0.5
1	1	-6 dB	x 0.25	x 0.25
1	0	Not Used	-	-

Table 20 – GPON Power Levelling Function

If GPON power levels of -3 dB or -6 dB are programmed then the GN25L95 automatically reduces the target APC monitor current and modulation current by 50% or 75% respectively. This results in a reduction in optical transmitted power of -3 dB or -6 dB whilst maintaining the correct extinction ratio and temperature compensated modulation current. It is expected that the GPON power level settings will not be changed during actual data transmission.

The power levelling function only applies to APC closed loop operation with Auto ER control or Modulation LUT control. The power levelling function cannot be used with bias current LUTs.

Tx Crossing Point Adjust

The transmitter crossing level can be adjusted using the TX_CROSSING control in register TX_CTRL_1. This gives a 4-bit control over the transmitter crossing point. The crossing point is adjusted by varying the pulse width of the transmitter eye from approximately -45 ps to + 45 ps. Adjusting the pulse width essentially shortens or lengthens the one-level period as shown in Figure 37. The nominal setting for TX_CROSSING to achieve a 50% crossing point is 0111b. The crossing adjustment control will have greatest effect when the data period is shortest at 2.5 Gbps. For data rates lower than 2.5 Gbps the crossing point adjustment will result in less aggressive variation in the crossing point.

The change in one-level pulse width versus the crossing point adjust control code TX_CROSSING is shown in Figure 38.

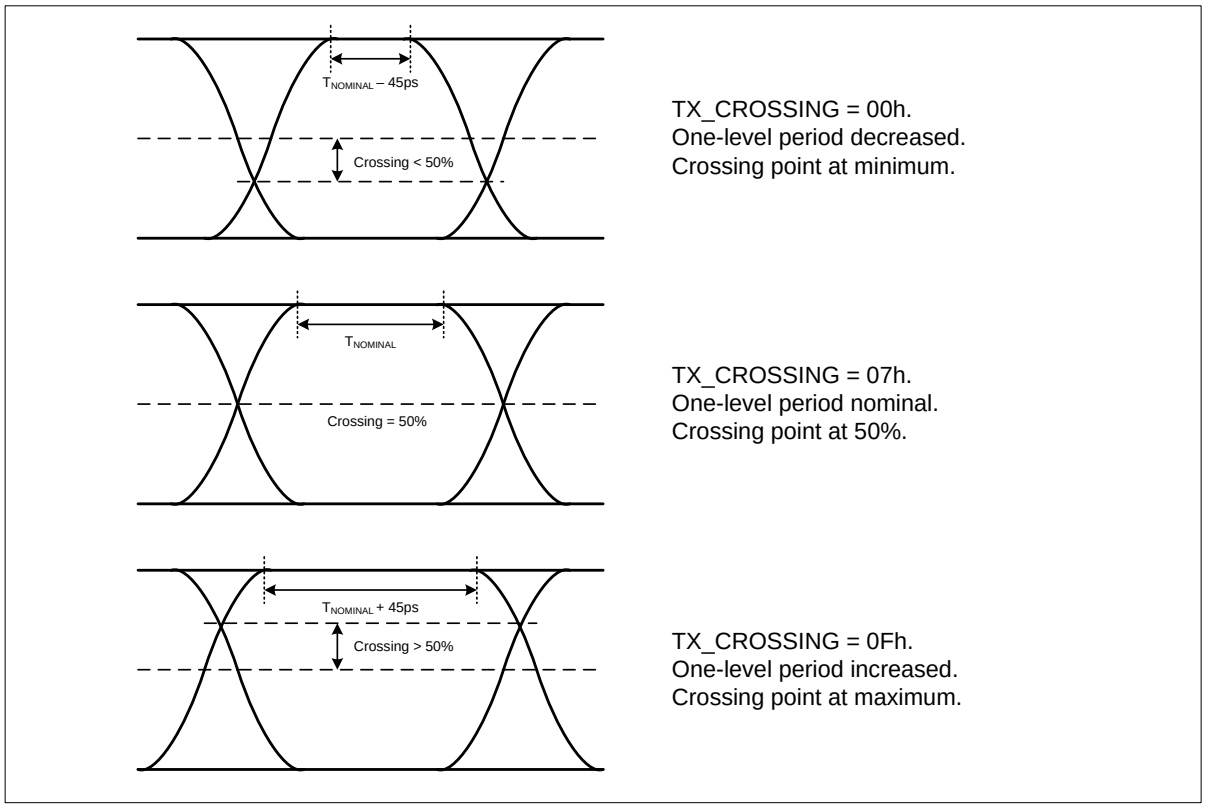


Figure 37 – GN25L95 Tx Crossing Point Adjustment using TX_CROSS

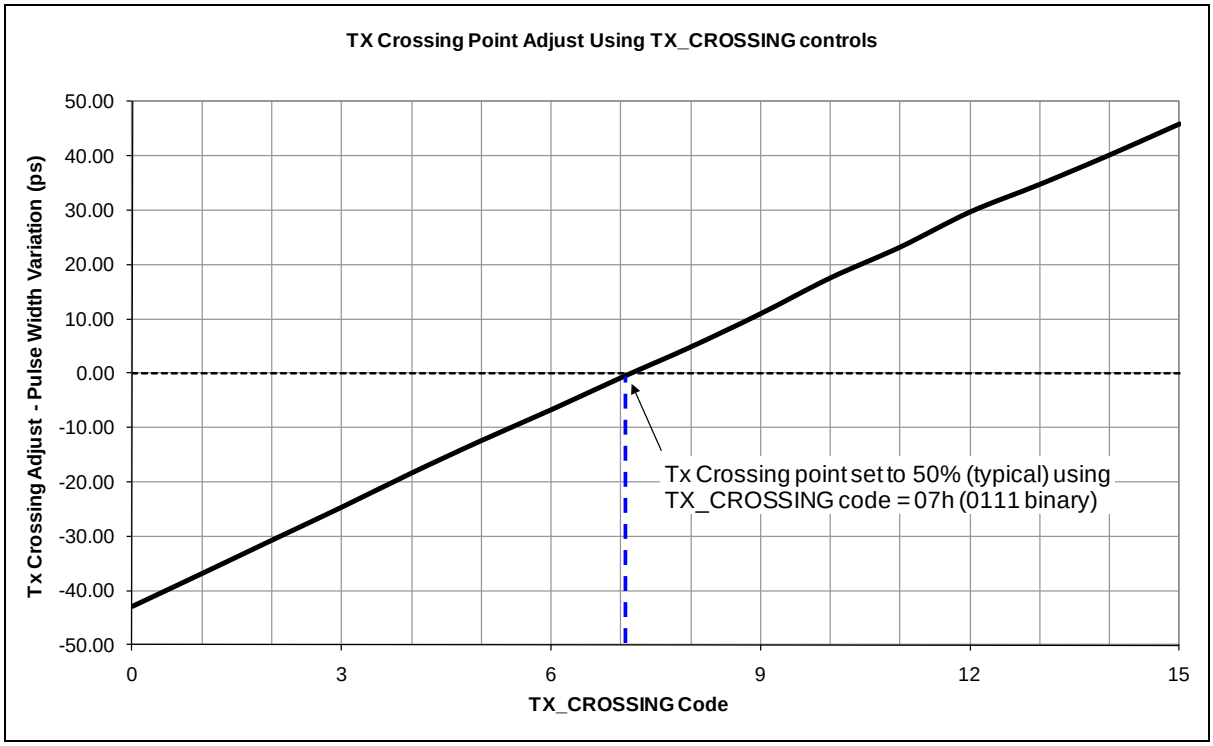


Figure 38 – GN25L95 Tx Crossing Point pulse width variation versus TX_CROSSING

Eye Safety Stage

The GN25L95 features in-built IEC-60825 Eye Safety circuitry that can be programmed as required for the target application.

The GN25L95 includes a TX_DISABLE hardware input and software control via I^2C and a TX_FAULT hardware output with software pin status indicator.

Programmable maximum bias and monitor current limits provide both eye safety and laser end-of-life (EOL) alarms.

A VCC supply monitor can disable the transmitter should VCC_TX go above or below factory limits (see Table 8).

The APC loop and Auto ER loop are protected by a single-point of failure check such that any opens or shorts to these control loops causes a TX_FAULT condition as required by IEC-60825. The GN25L95 circuit response to single point failures is shown in Table 21.

If an APC/Auto ER loop fault occurs, then the TX_FAULT output will be asserted. In the same instance, the bias and modulation currents will be internally disabled to turn off the laser.

In the case of an APC/Auto ER loop fault, the TX_FAULT output can only be reset and the outputs enabled again by either cycling the GN25L95 power supply or by toggling the TX_DISABLE input for a duration greater than 10 µs.

The APC loop and Auto ER loops are protected against single-point failures by using the BIAS_MAX, MD_MAX and MOD_MAX maximum limit functions for bias current, monitor photodiode current and modulation current respectively. These functions are described in more detail in their own sections within this datasheet and in the memory map.

The GN25L95 safety logic circuit diagram is shown in Figure 39. The safety logic can be completely disabled by setting FAULT_INHIBIT. Any latched faults can be changed to non-latching faults by setting LATCH_INHIBIT. The supply voltage monitor can also be disabled such that any over or under voltage events on TX_VCC do not cause a TX_FAULT condition by setting VCC_INHIBIT.

Alarms and Warnings

The GN25L95 can be set to automatically generate alarms and warnings if any of the five DDMI monitor values exceed thresholds defined in A2h lower 00h to 36h.

If a DDMI threshold value is exceeded then the GN25L95 generates an individual high or low alarm and/or warning flag for each of the five individual DDMI monitors giving twenty flags in total. Flags can be latched or non-latched, determined by the controls in ALM_WRN_CTRL register. The flags can also be programmed to disable the transmitter if required and/or generate a TX_FAULT output (for hardware indication of an exceeded alarm/warning threshold). The high and low alarm/warning flags can be individually enabled by setting registers in the vendor reserved area of address A2h at addresses F8h to FFh.

TX_FAULT Output

The TX_FAULT output can be configured as either an open drain output or a LVTTL output. When used in open drain mode, the TX_FAULT output pin should be pulled high to TX VCC using a 4.7kΩ to 10kΩ resistor.

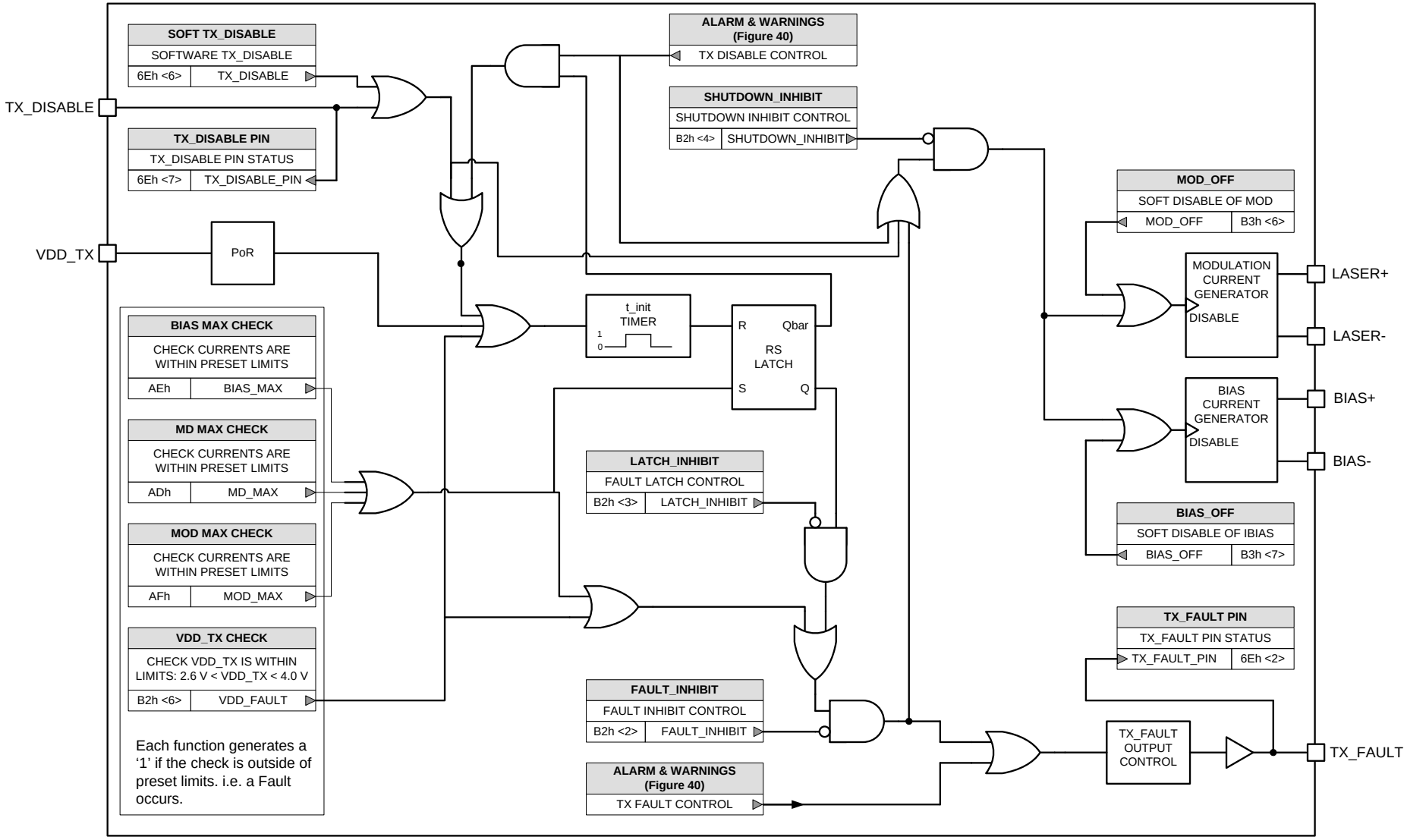


Figure 39 – GN25L95 Eye Safety Logic Control Circuit

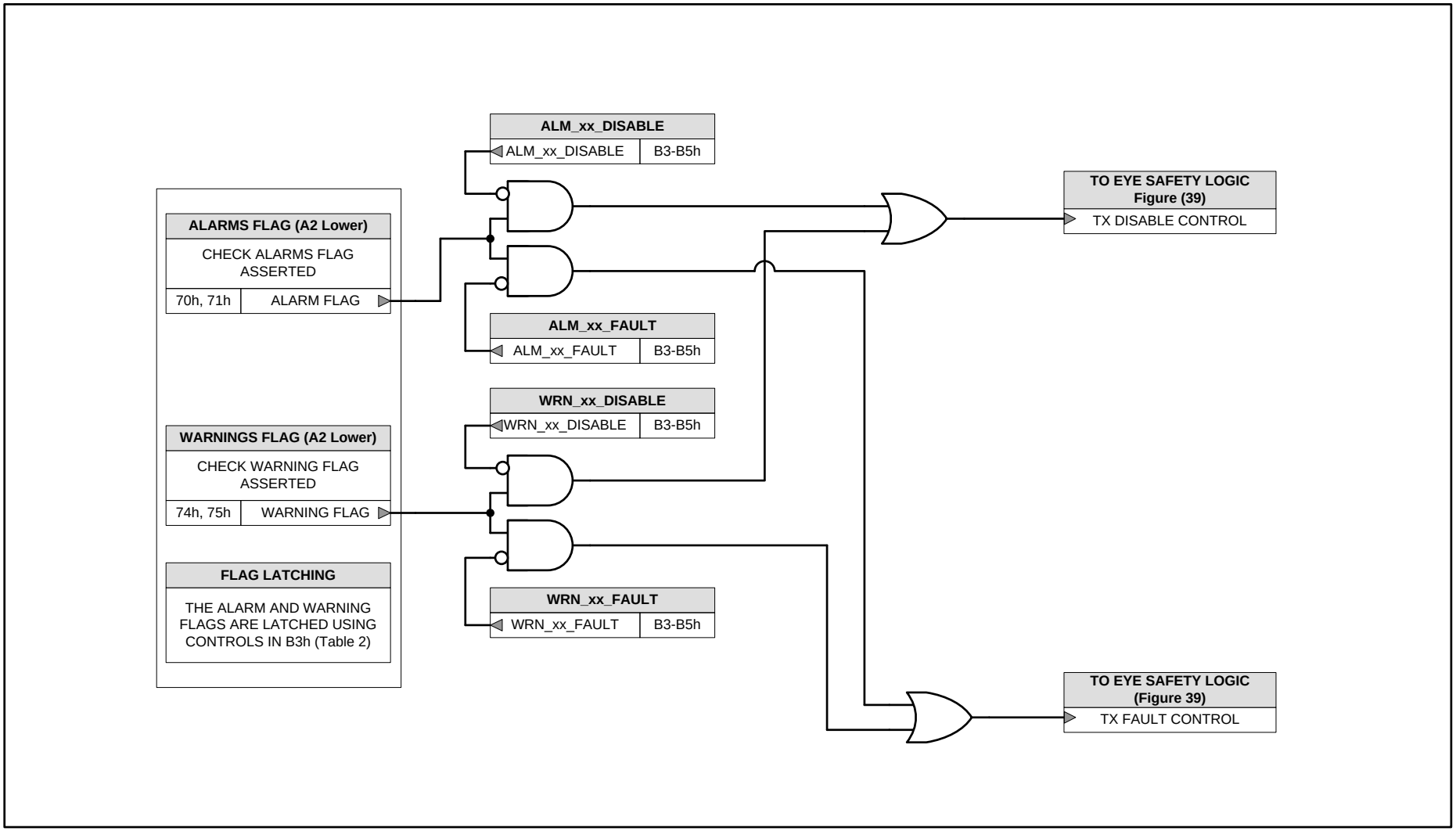


Figure 40 – GN25L95 Alarms & Warnings Safety Logic Control Circuit

Circuit Responses to Single Points Of Failure

The table below shows the GN25L95 responses to single point failures at each pin:

PIN	NAME	SHORT TO VCC_TX	SHORT TO GND	OPEN
1	SD/LOS	None. Excessive SD/LOS current. Could cause internal damage to circuits.	None	None
2	RXOUT-	None. Could cause internal damage to circuits.	None. Could cause internal damage to circuits.	None
3	RXOUT+	None. Could cause internal damage to circuits.	None. Could cause internal damage to circuits.	None
4	VCC_DIG	None.	IC short circuit. Tx disabled. Non-latching TX_FAULT output attempted during IC malfunction.	IC not powered correctly. Tx will not function.
5	SDA	None. Communications will not function.	None. Communications will not function.	None
6	SCL	None. Communications will not function.	None. Communications will not function.	None
7	EE_SDA	None. EEPROM communications will not function.	None. EEPROM communications will not function. MCU mode.	None
8	EE_SCL	None. EEPROM communications will not function.	None. EEPROM communications will not function. MCU mode.	None
9	TX_DISABLE/ TX_SLEEP	Tx disabled/Tx Sleep.	None	Tx disabled/Tx Sleep.
10	TXIN+	None	None	None
11	TXIN-	None	None	None
12	BEN+	None	None	None
13	BEN-	None	None	None
14	MPD	TX_FAULT asserted (latching). Bias and modulation currents disabled.	TX_FAULT asserted (latching). Bias and modulation currents disabled.	TX_FAULT asserted (latching). Bias and modulation currents disabled.
15	BIAS-	None. Increases chip power dissipation.	None.	None.
16	BIAS+	TX_FAULT asserted (latching). Bias and modulation currents disabled.	TX_FAULT asserted (latching). Bias and modulation currents disabled.	TX_FAULT asserted (latching). Bias and modulation currents disabled.
17	VCC_TX	None	IC short circuit. Tx disabled. Non-latching TX_FAULT output attempted during IC malfunction.	IC not powered correctly. Tx will not function.
18	LASER-	TX_FAULT asserted (latching). Bias and modulation currents disabled. Applies only if DC connected to Laser.	TX_FAULT asserted (latching). Bias and modulation currents disabled. Applies only if DC connected to Laser.	None

19	LASER+	TX_FAULT asserted (latching). Bias and modulation currents disabled. Applies only if DC connected to Laser.	TX_FAULT asserted (latching). Bias and modulation currents disabled. Applies only if DC connected to Laser.	None
20	TX_FAULT	None. Excessive TX_FAULT current. Could cause internal damage to circuits.	None	None
21	TX_SD	None. Excessive TX_SD current. Could cause internal damage to circuits.	None	None
22	APD_DAC	None	None	None
23	RSSI_IN	None	None	None
24	ADC_IN	None	None	None
25	RXIN-	None	None	None
26	RXIN+	None	None	None
27	RX_SLEEP	Rx in sleep mode	None	Rx in sleep mode
28	VCC_RX	None	None. IC short circuit. IC malfunction.	None. IC malfunction.
CP	GND	IC short circuit. Tx disabled. Non-latching TX_FAULT output attempted during IC malfunction.	None	IC not grounded correctly. IC may not function correctly.

Table 21 – Circuit Responses to Single Point Failures

Assumes MD_MAX, MOD_MAX and BIAS_MAX are not inhibiting.
Assumes all safety logic circuits are enabled.
BIAS+ output should always be used to drive the laser for correct eye safety operation. BIAS- is only a dummy complementary bias output and does not have internal eye safety protection.

Safety Logic Timing

The following diagrams show the GN25L95 responses to TX_FAULT conditions during start-up and normal operation in the presence of specific faults.

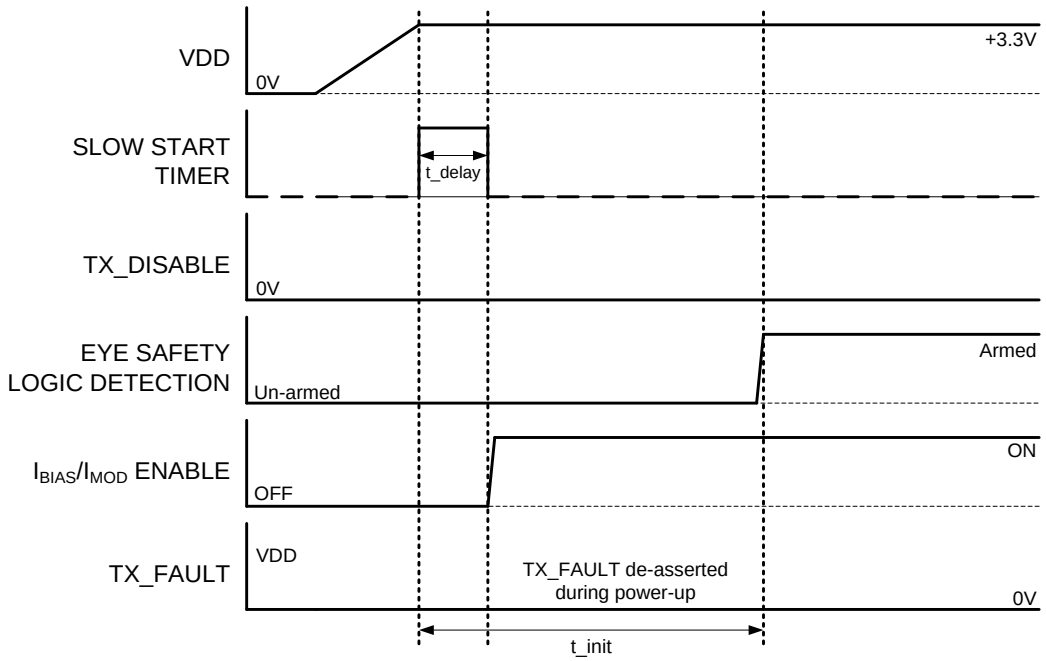


Figure 41 – Power-up Timing Sequence

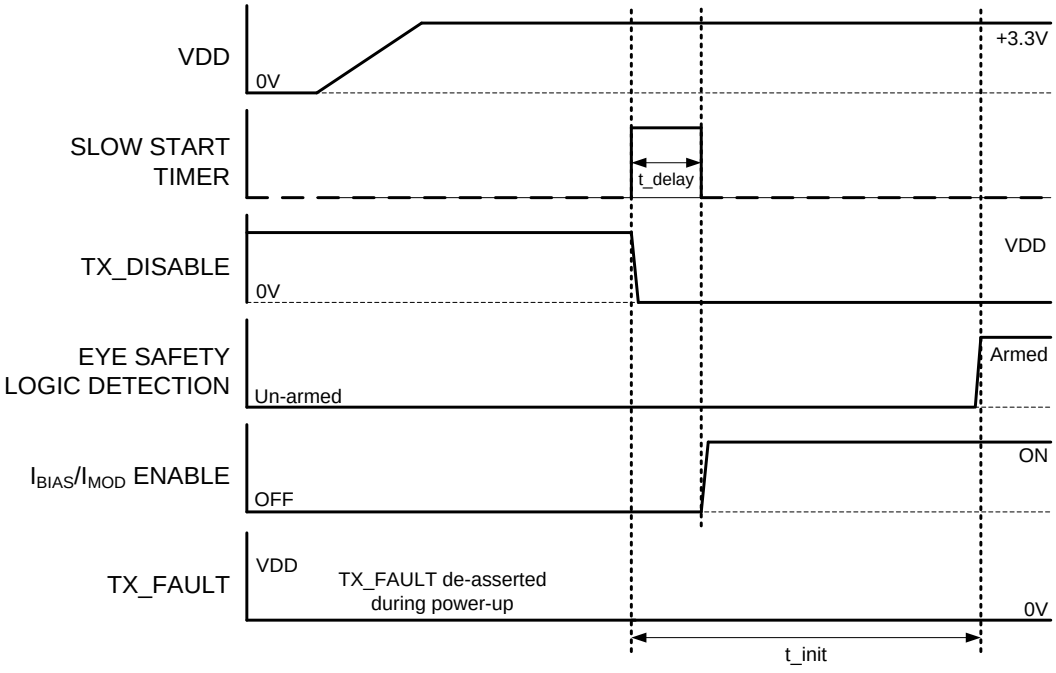


Figure 42 – TX_DISABLE Held High During Power-up Timing Sequence

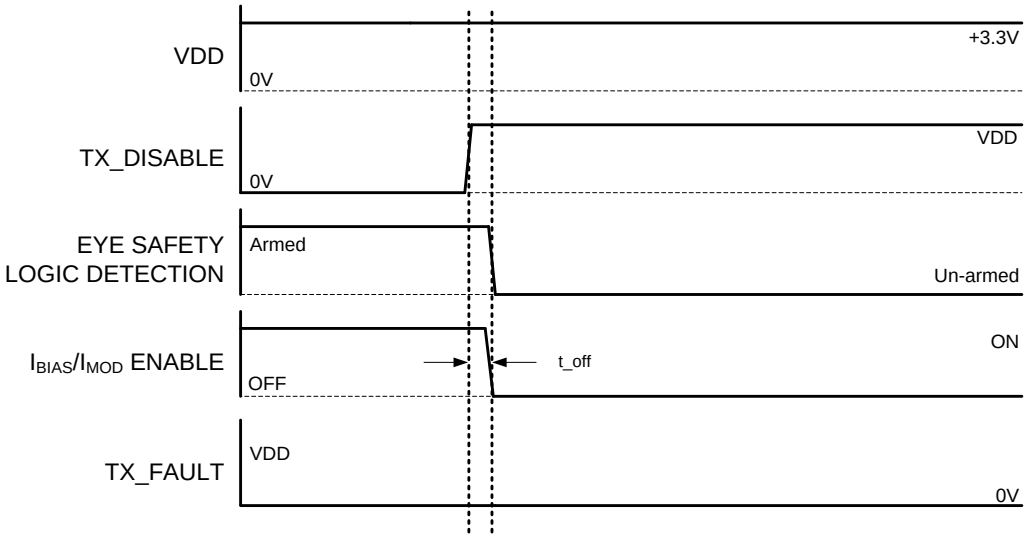


Figure 43 – TX_DISABLE Held High During Normal Operation

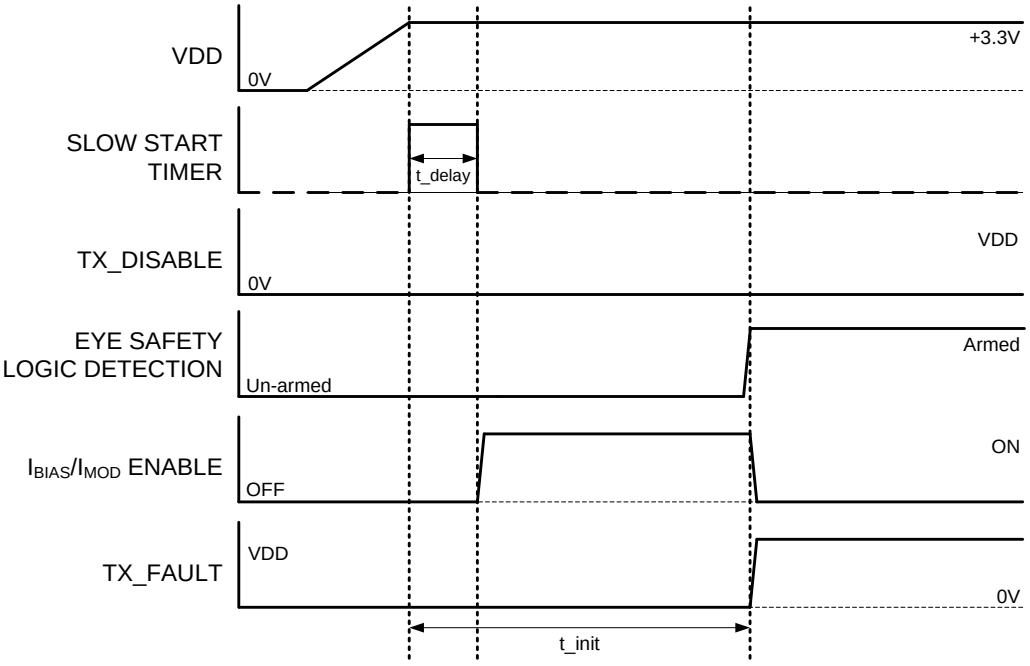


Figure 44 – APC Loop Error during Power-up Causing TX_FAULT

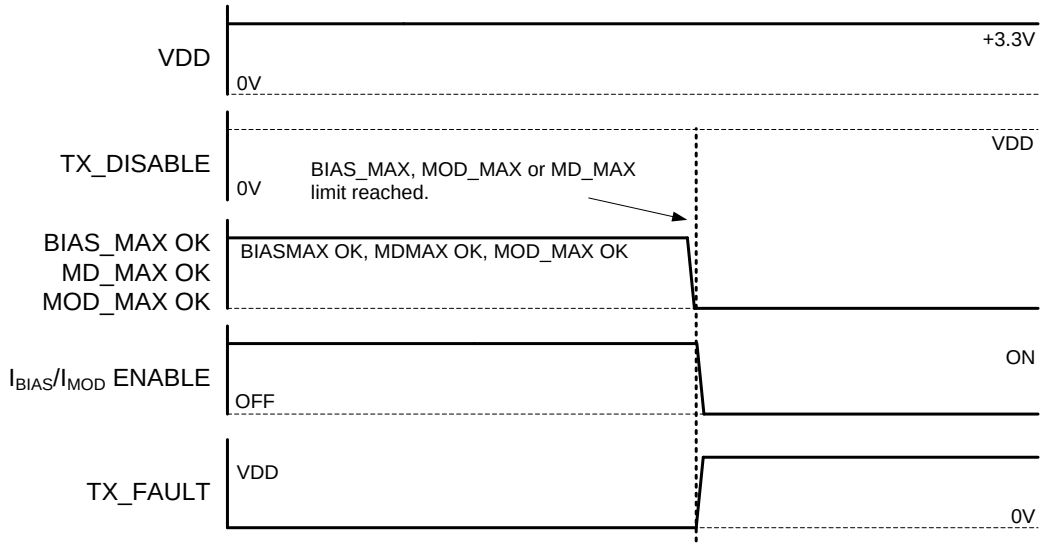


Figure 45 – BIAS_MAX, MD_MAX or MOD_MAX current limit exceeded causing TX_FAULT

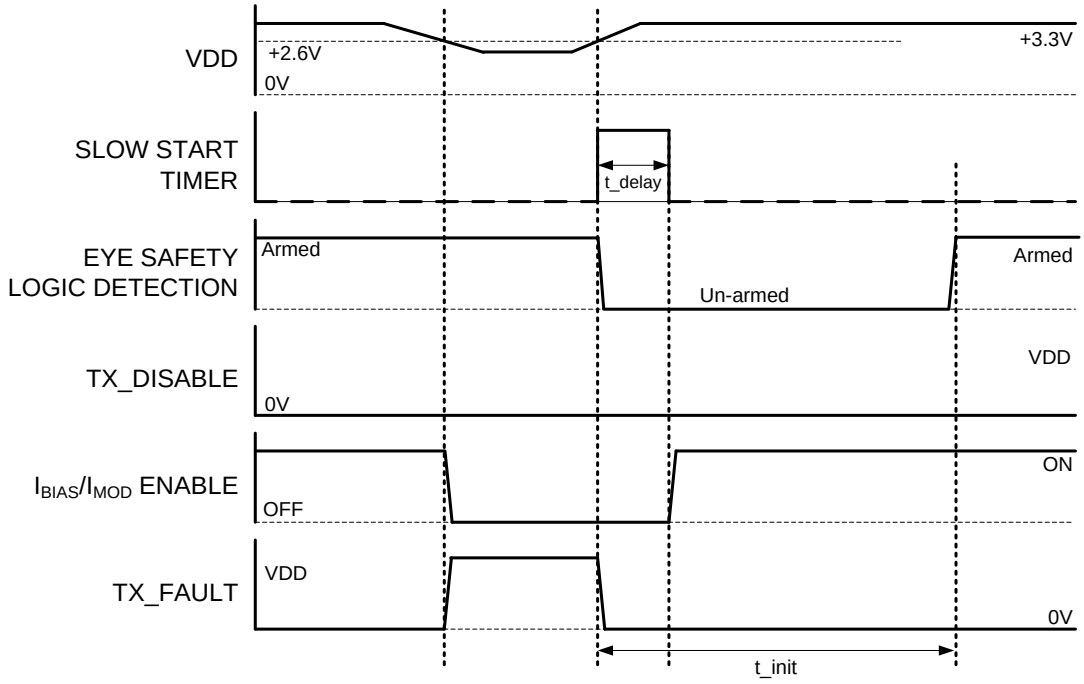


Figure 46 – VCC drops below default limit causing a non-latching TX_FAULT

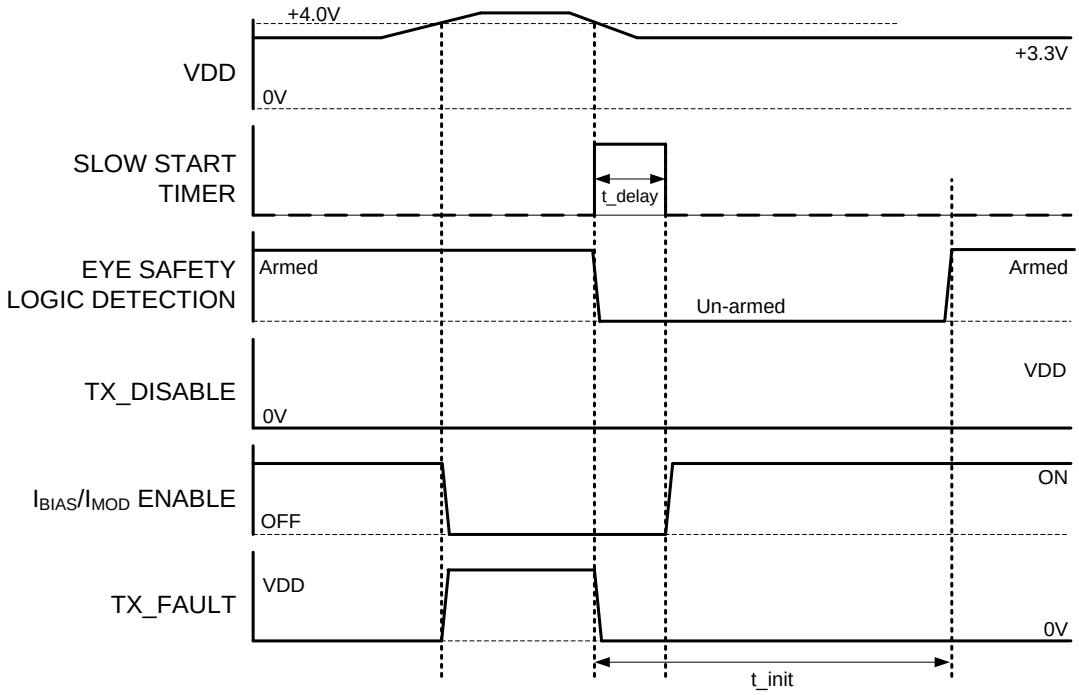


Figure 47 – VCC exceeds default limit causing a non-latching TX_FAULT

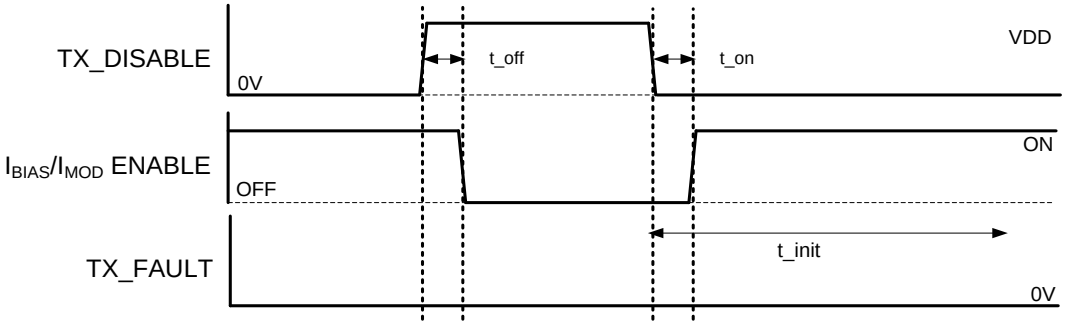


Figure 48 – TX_DISABLE asserted under normal operation

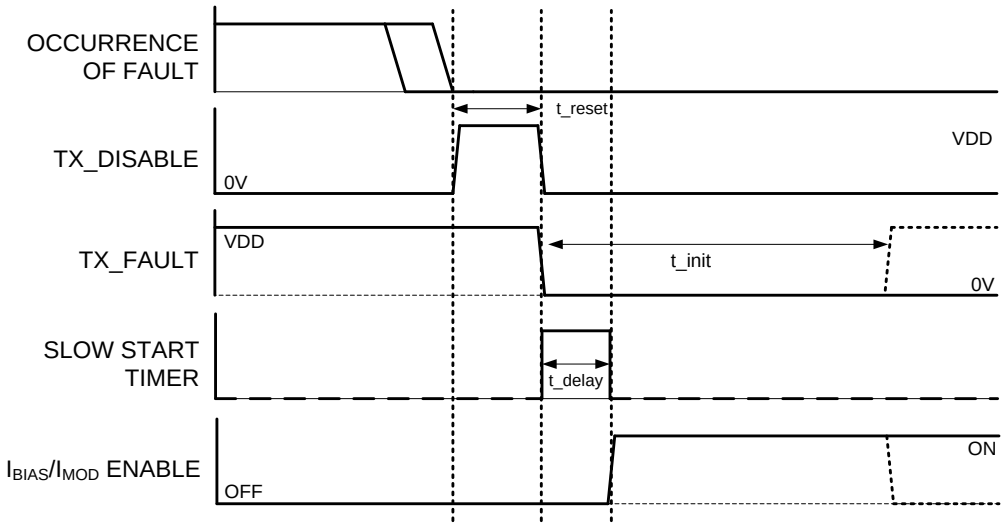


Figure 49 – Clearing of TX_FAULT by toggling of TX_DISABLE

TX_DISABLE on Rx LOS

The GN25L95 can be set-up so that the transmitter outputs can be disabled on detection of a receiver loss of signal (LOS) condition. This function is selected by setting bit 7 (TX_DISABLE_ON_RX_LOS) of TX_CTRL_0 in Table 2, location A1h.

The timing of this function is compliant with SFP MSA timing as the Rx hardware LOS signal is used to control the TX_DISABLE function in this case.

Receiver Features

The GN25L95 features a limiting receiver with CML differential output stage. The signal path operates from 155 Mbps to 2.7 Gbps and has selectable receiver bandwidth settings to improve sensitivity in lower data rate applications. The receiver section also contains a signal detect function with polarity selectable status output indicator.

Receiver Input Stage

The GN25L95 data inputs are internally biased via 6.5k Ω resistors to a common mode voltage of 1.5V. The receiver inputs should be differentially terminated with an external 100 Ω resistor between RXIN+ and RXIN-. Typically the data inputs would be AC coupled to the preceding transimpedance amplifier (TIA) IC. The data input stage is designed to be driven differentially and is sensitive to input voltages as low as 4.0 mV peak-to-peak. The data input stage is shown below.

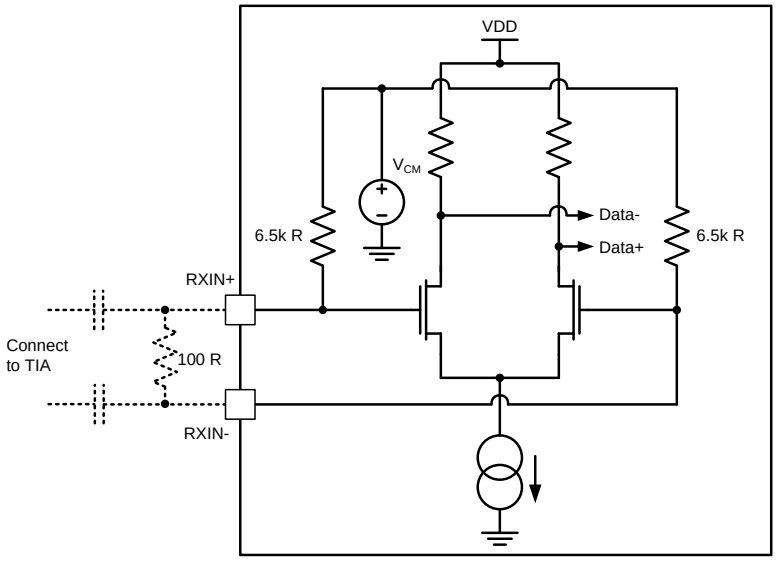


Figure 50 – Receiver Input Stage

Receiver CML Output Stage

The GN25L95 data outputs are CML compliant and may be terminated using an AC-coupled differential termination scheme. A typical AC-coupled 100 Ω termination scheme is shown below.

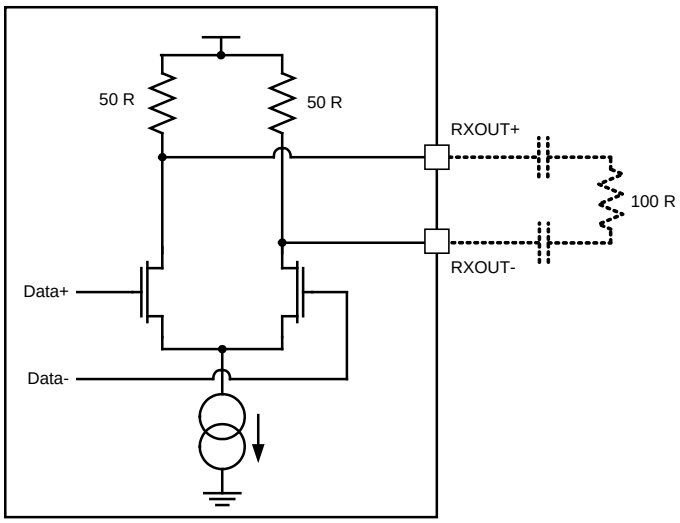


Figure 51 – Receiver Output Stage

Receiver Digital Control Functions Block Diagram

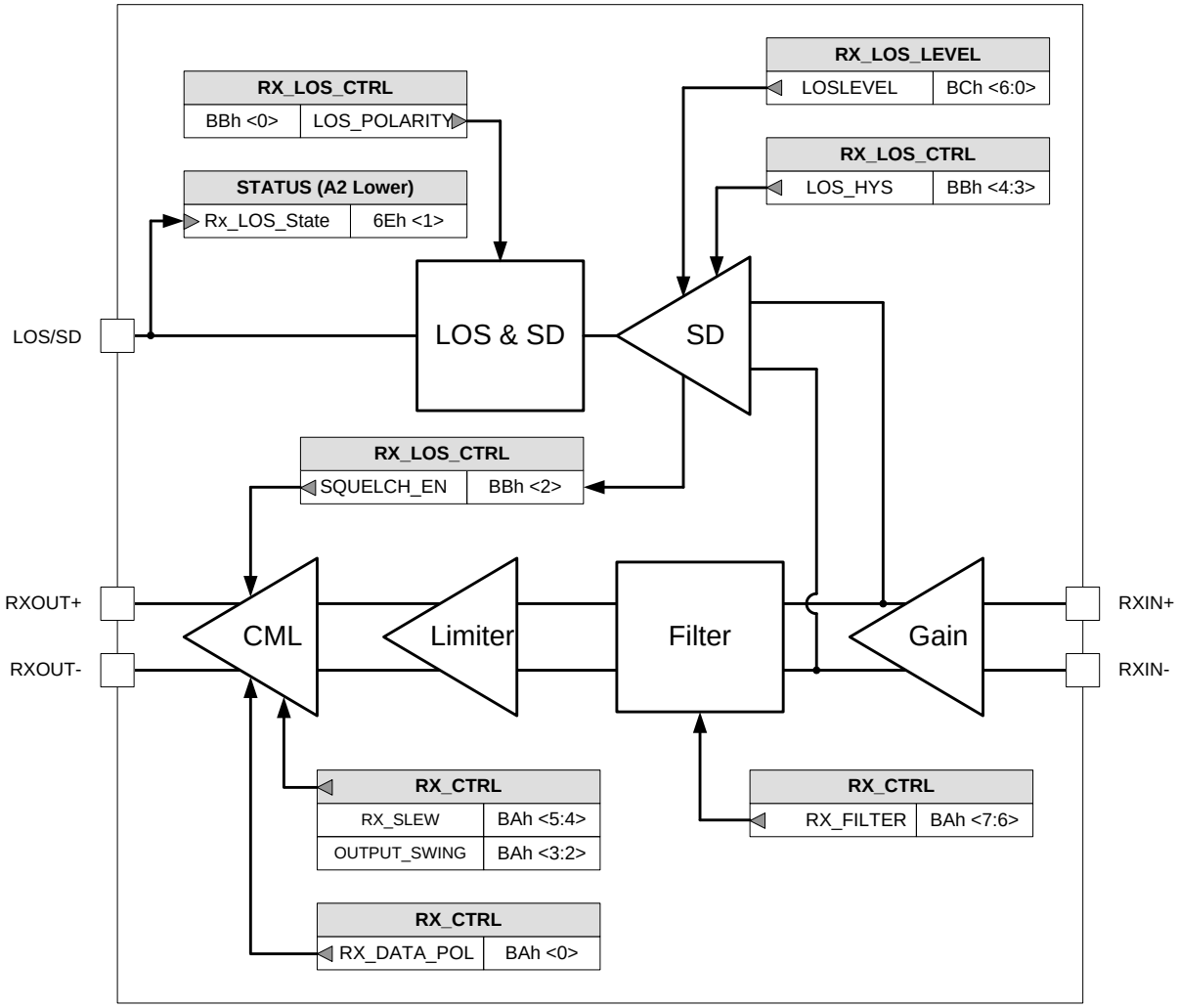


Figure 52 – GN25L95 Receiver Digital Control Functions

Receiver Data Output Polarity Invert Function

The receiver data output polarity can be inverted by setting the RX_DATA_POLARITY bit.

Receiver Data Output Amplitude Control

The GN25L95 has a programmable CML output stage that allows four different amplitudes to be selected using OUTPUT_SWING. The levels available are shown in the table below.

Register RX_CTRL_0 (BAh Bits 3:2)		Output Swing
OUTPUT_SWING <1>	OUTPUT_SWING <0>	
0	0	600 mVpp
0	1	800 mVpp
1	0	900 mVpp
1	1	1000 mVpp

Table 22 – GN25L95 Receiver Output Amplitude Control

Although the GN25L95 default for OUTPUT_SWING is <0:0> resulting in a 600 mVpp swing it is expected that the majority of applications will use the setting of 900 mVpp output swing for EPON, GPON and SFP applications above 622 Mbps.

Receiver Data Output Slew Control

The CML output slew rate can also be adjusted to optimise the receiver data output rise and fall times for the specific application. The possible settings are shown in the table below.

Register RX_CTRL_0 (BAh Bits 5:4)		Slew Selected	Typical 20%-80% Rise/Fall times
RX_SLEW <1>	RX_SLEW <0>		
0	0	OFF (Default)	90 ps
0	1	FAST	160 ps
1	0	MEDIUM	320 ps
1	1	SLOW	1280 ps

Table 23 – GN25L95 Receiver Output Slew Control

Receiver Filter Stage

The receiver signal path contains a digitally programmable bandwidth filter which limits the upper cut-off frequency to one of three settings enabling the signal path sensitivity to be optimised for the data rates shown in the table below.

Register RX_CTRL_0 (BAh Bits 7:6)		Receiver Rate Setting
RX_FILTER <1>	RX_FILTER <0>	
0	0	2.5 Gbps (default)
0	1	1.25 Gbps
1	0	622 / 155 Mbps
1	1	622 / 155 Mbps

Table 24 – GN25L95 Receiver Bandwidth Settings

Setting RX_FILTER to either <1 :0 > or <1 :1> results in the same filter setting which can be used for 622 Mbps or 155 Mbps applications.

Optimising the Receiver Signal Path Settings

The GN25L95 provides control over the receiver signal path for output amplitude, slew rate and filter rate setting. Below is a table with recommended settings for all of these controls for specific data rates and applications.

Data Rate	Application	Rate Setting	Amplitude	Slew Rate
2.5 Gbps	GPON, SFP, SFF	2.5 Gbps	900 mVpp	OFF
1.25 Gbps	EPON, SFP, SFF	1.25 Gbps	900 mVpp	FAST
622 Mbps	SFP, SFF	622 / 155 Mbps	1000 mVpp	MEDIUM
155 Mbps	SFP, SFF	622 / 155 Mbps	1000 mVpp	SLOW
Multi-Rate	155M – 2.5G SFP	2.5 Gbps	900 mVpp	OFF

Table 25 – Optimised Receiver Signal Path Settings

Signal Detect/Loss of Signal Stage

The GN25L95 features a signal status output that is polarity selectable as a LOS or an SD status output. A signal status function is implemented on-chip that uses a peak detector to determine the input modulation amplitude and then compares this with a tuneable reference level, set by the digital interface. If the input amplitude falls below the preset level then the status output is asserted. The assert to de-assert hysteresis can be programmed to be between 1.5 dB to 3.0 dB optically.

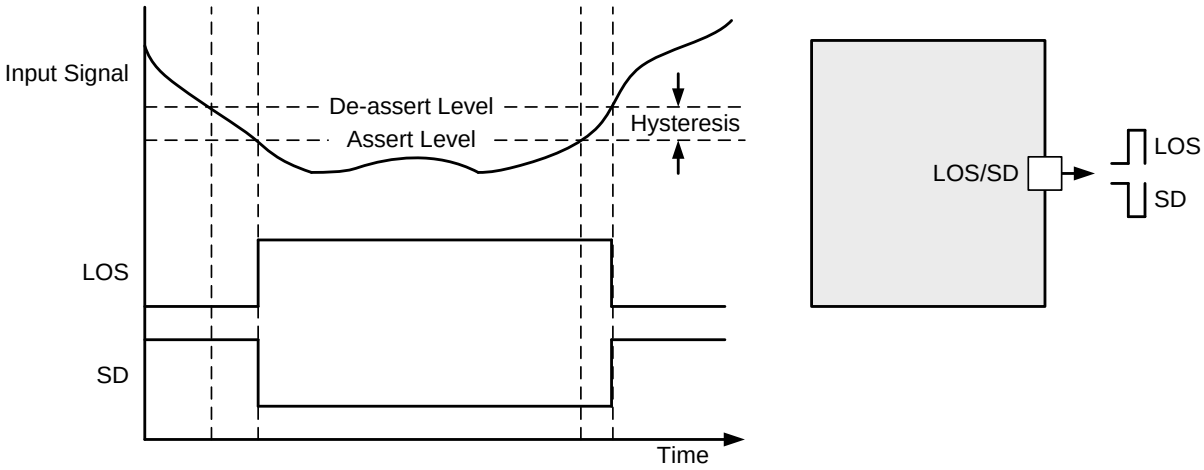


Figure 53 – Receiver Signal Detect Operation

Setting the LOS Assert Level

The LOS signal assert level is set using the control LOS_LEVEL in register RX_LOS_LEVEL. This controls a 7-bit linear DAC to set the LOS assert threshold and covers the range 0 mVpp to 127 mVpp and is described by the formula below:

LOS Assert Level (mVpp) = 1 mV * LOS_LEVEL <6:0>

The LOS is designed to work across the differential signal input range of 10 mVpp to 60 mVpp (see Table 6 for details). The programming range is shown graphically in Figure 54.

Setting the LOS Hysteresis

The LOS hysteresis can be set to one of four levels using register RX_LOS_CTRL. Details are shown in the table below. Figure 55 shows the LOS Assert and De-Assert levels graphically for all Hysteresis settings.

Register RX_LOS_CTRL (BBh Bits 5:3)			Hysteresis (Optical)
LOS_HYS <2>	LOS_HYS <1>	LOS_HYS <0>	
0	0	0	0.5 dB (default)
0	0	1	1.0 dB
0	1	0	1.5 dB
0	1	1	2.0 dB
1	0	0	2.5 dB
1	0	1	3.0 dB

Table 26 – LOS_HYS Settings

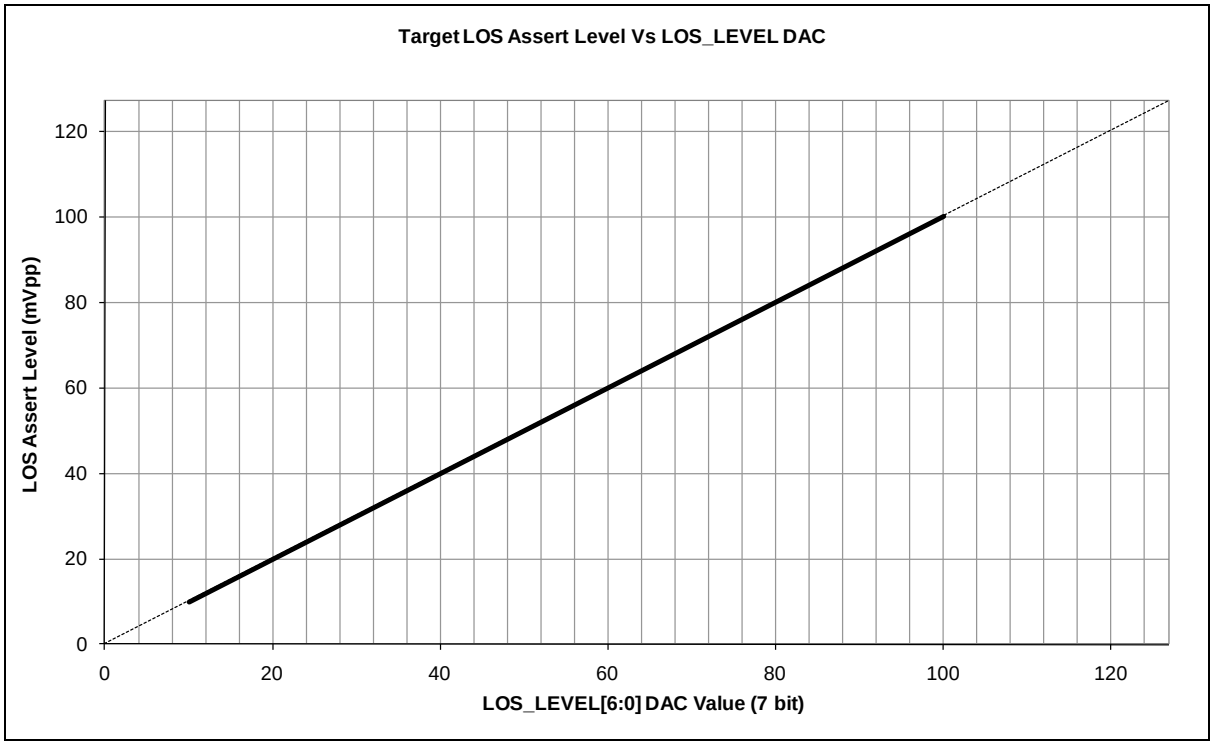


Figure 54 – GN25L95 LOS Assert Setting

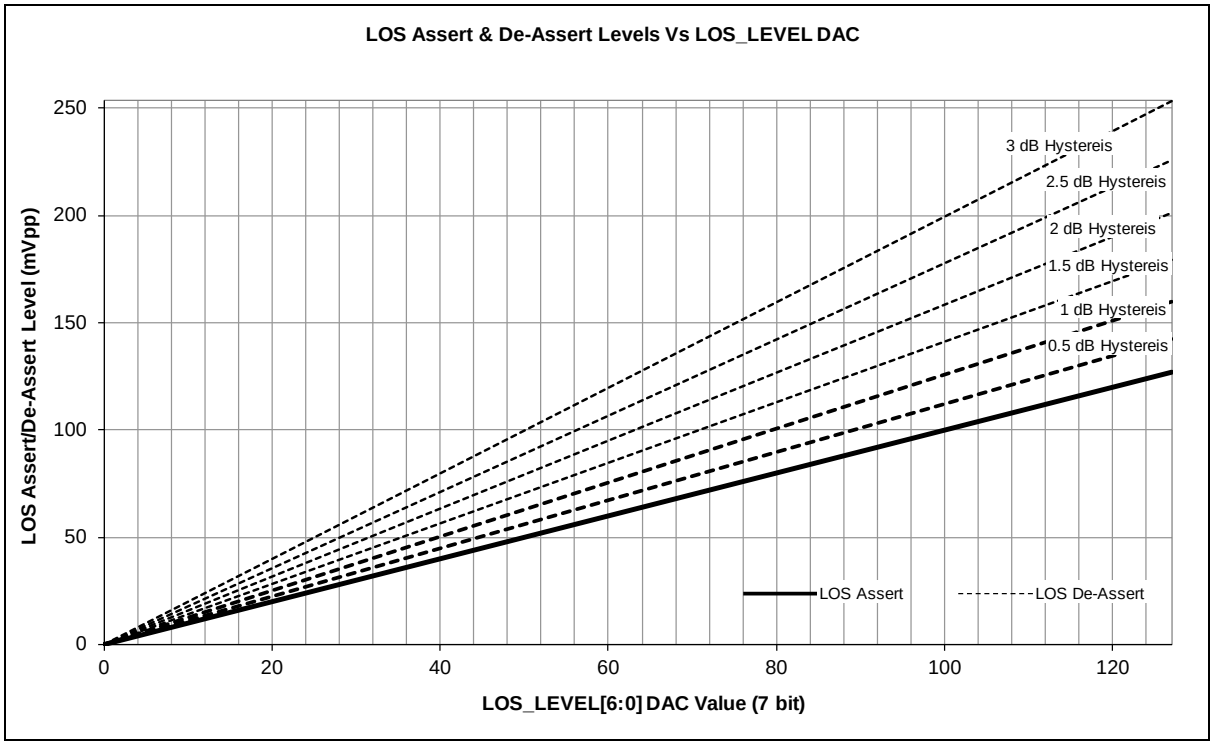


Figure 55 – GN25L95 LOS Assert & De-Assert Levels with Hysteresis

LOS/SD Output Type

The LOS/SD pin can be programmed as either an open drain output or a true LVTTL output. As an open drain output the LOS/SD pin is typically tied to VCC_RX via a 4.7kΩ to 10kΩ pull-up resistor. The output type is set using the register control LOS_OUT_TYPE.

Semtech recommends adding a 220 Ω series resistor between the LOS/SD pin and the host interface to protect from electrical overstress events during optical transceiver manufacture.

LOS/SD Output Polarity

The polarity of the LOS/SD can be changed from Loss of Signal (default) to Signal Detect by programming the register control LOS_POLARITY.

Receiver Output Squelch Function

The receiver outputs can be squelched during a Loss of Signal condition. To enable squelching of the outputs the SQUELCH_ENABLE bit should be set in register RX_LOS_CTRL. The receiver outputs will be set to the mid-point of their nominal levels when squelched.

APD DAC Control

The GN25L95 integrates a digital-to-analogue convertor with current output for controlling an external avalanche photodiode bias circuit. The APD DAC output can be used in conjunction with an external resistor to develop an APD bias control voltage, or the APD DAC output current can be used to directly control an APD bias generator circuit.

The APD DAC is programmed by setting register bytes APD_DAC and APD_DAC_CTRL via the I^2C interface.

The APD_DAC register sets the DAC output current in conjunction with the APD_DAC_CTRL register. The output can be configured in 1 of 4 modes as shown in the table below:

APD_DAC_CTRL (BDh Bits 2:1)		Output Mode	Iref	Output Current Range
APD_MODE <1>	APD_MODE <0>			
0	0	Source	4 µA	0 – 1980 µA
0	1	Source	2 µA	0 – 990 µA
1	0	Sink	1 µA	0 – 495 µA
1	1	Sink	0.5 µA	0 – 247.5 µA

Table 27 – APD DAC Output Mode Control and Range Settings

The output current set can be calculated using the following formula and depending on the mode selected from the table above:

I_APD_DAC = (APD_DAC + (APD_DAC_OFFSET *16))*Iref

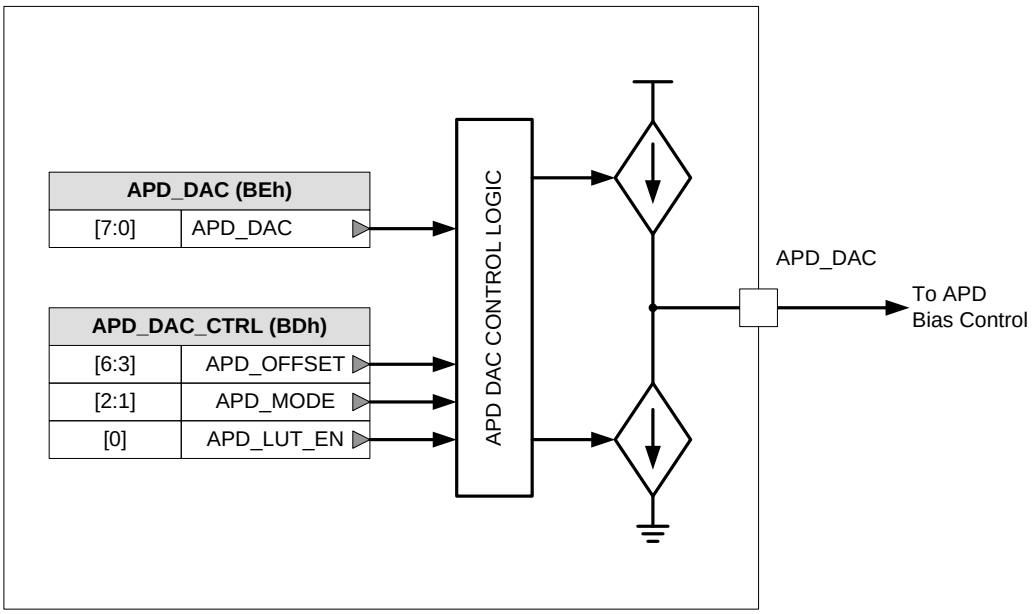


Figure 56 – APD DAC Output

The APD DAC can be controlled via a temperature indexed LUT located at A2h Table 6, C0h to FFh. When enabled, the GN25L95 sets the APD DAC output based on the programmed DAC value indexed to the current temperature.

Sleep Modes

The transmitter and receiver of the GN25L95 can be placed into low power sleep modes using either software or hardware control.

Software control of Sleep Modes

The Tx and Rx can be independently placed into sleep mode using the register bits RX_SLEEP and SOFT_TX_DISABLE (when the TX_SLEEP function is enabled and controlled through TX_DISABLE by setting the TX_SLEEP_MODE bit in Table 2, BFh <0>). The timing will be dependent on the overall I^2C bus speed.

Hardware control of Sleep Modes

The transmitter and receiver sleep modes can be activated independently via hardware input pins on the GN25L95.

Tx Sleep Control

The transmitter can be placed into sleep mode by using the TX_DISABLE input pin (9). The TX_DISABLE pin can be configured as the Tx sleep control pin by setting bit TX_SLEEP_MODE. When this bit is set then the TX_DISABLE will place the transmitter into a low power sleep mode and also disable the transmitter. This applies to both hardware and software TX_DISABLE assertions.

The table below shows all transmitter sleep mode configurations.

TX_DISABLE (TX_SLEEP)	TX_SLEEP_ MODE	Mode	Sleep Assert/ de-assert Time	Tx Supply Current
De-asserted	X	(Tx Enabled)	N/A	Nominal
Asserted	0	TX_DISABLE	N/A	Tx Disabled
Asserted	1	TX SLEEP + TX_DISABLE	< 500 ns	< 3 mA

Table 28 – Hardware control of Tx sleep modes

The hardware control provides a faster activation of sleep modes as detailed in the parametric section. The hardware and software sleep control functions are logic OR'd together.

If the transmitter is being used in closed loop control mode (i.e. using the APC loop to set the mean power) and the TX_FAST_SLEEP register is set to 0, on resuming normal operation after coming out of Tx sleep, the transmitter will immediately perform a fast start-up search to determine the correct mean power setting. If TX_FAST_SLEEP is set to 1, the APC loop (and Auto ER loop, if enabled) will resume operation with the previous closed-loop controlled values for bias (and modulation) current.

The following timings apply to the activation of the transmitter sleep mode:

TX_SLEEP must be de-asserted at least 128 µs before TX_DISABLE is de-asserted.

Rx Sleep Control

The receiver can be placed in a low power sleep mode by asserting the RX_SLEEP pin (27) high using an external hardware control or by setting RX_SLEEP in the user registers. In sleep mode, the receiver consumers less than 1 mA. Assert and de-assert times are less than 1 ms.

By setting bit RX_SLEEP_CONTROL the receiver sleep mode is logical OR'd with the transmitter sleep mode. Therefore asserting TX_DISABLE high will result in both the Tx and Rx entering a sleep state. The RX_SLEEP hardware input will also still function when this mode is selected. This allows

the user to control both the Tx and Rx sleep modes with one hardware input (TX_DISABLE) and software control.

Tx and Rx Hardware Sleep Control Polarity Inversion

The TX_DISABLE (TX_SLEEP) and RX_SLEEP hardware inputs can be polarity inverted so that instead of these pins having to be driven logic high to force the Tx and/or Rx into sleep mode the pins have to be driven low.

The TX_DISABLE polarity inversion function TX_DISABLE_POL (A2h Table 2 BFh <2>) inverts the hardware input signal and applies to both TX_DISABLE and TX_SLEEP functions.

The RX_SLEEP polarity inversion function RX_SLEEP_POL (A2h Table 2 BFh <3>) inverts the hardware input signal for RX_SLEEP.

The soft control functions are NOT polarity inverted.

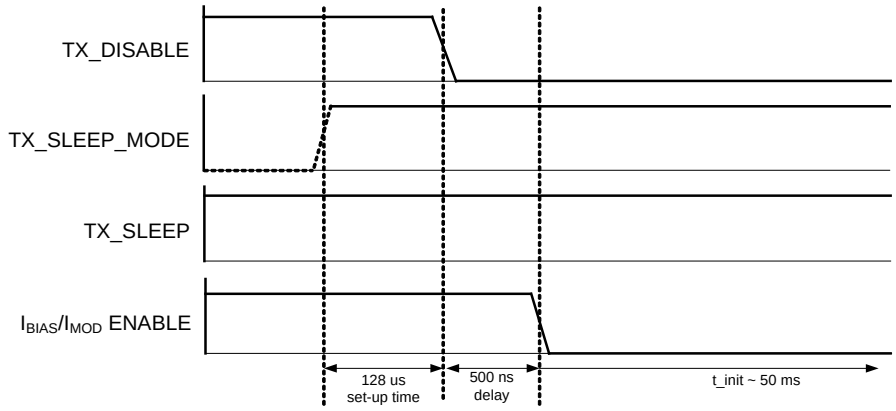


Figure 57 – Exit from standby (LATCH_INHIBIT= 0)

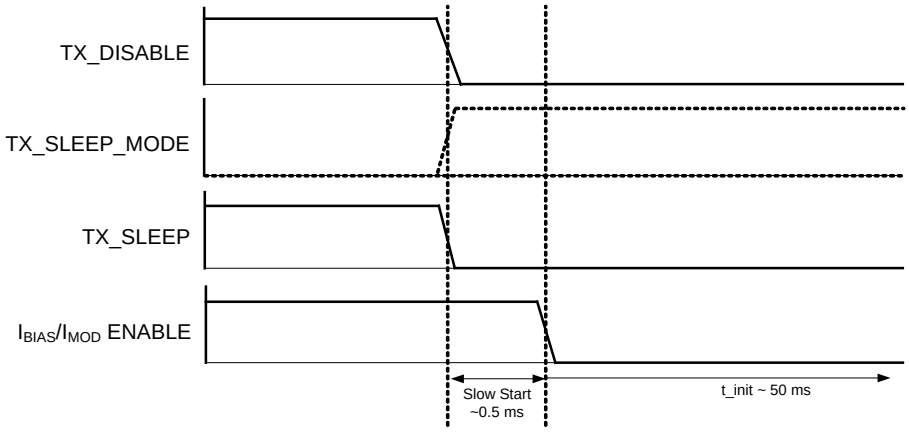


Figure 58 – Exit from disabled mode (LATCH_INHIBIT = 0)

Digital Control & Monitoring Features

The GN25L95 is set-up, programmed and controlled via an I^{2}C digital interface. Registers in the GN25L95 are used to control the various analogue functions within the IC. The contents of the registers related to the IC's configuration are stored in non-volatile memory (on-chip NVM or external EEPROM) to allow the IC to function from power-up without the requirement for an external microcontroller. The GN25L95 registers can be found at I^{2}C address A2h Table 2.

Digital I^{2}C Interface

The I^{2}C interface is a slave interface responding to read and write requests from an external master interface on a host controller. The SDA and SCL interface lines are internally pulled-up to VCC with 10k Ω resistors to reduce off chip components. The interface supports the standard 100 kHz mode and 400 kHz fast mode.

An I^{2}C transaction is contained within a frame that is preceded by a start condition and completed by a stop condition. A start condition is defined by the host master pulling the SDA line low whilst the SCL line is high. A stop condition is defined by the host master releasing the SDA to transition low to high whilst the SCL line remains high.
The master interface has control of the bus during a framed transaction. The GN25L95 allows repeat start conditions in which the master may send multiple frames delimited by a start condition before finally sending a stop condition. This allows the master to send multiple frames without releasing control of the bus.

During a framed data transaction, data is transferred from master to slave or slave to master by clocking data on the bus. A data bit is valid during a clock low to high transition whilst the SDA state may only change when the SCL line is low. Data is arranged as 8 bits followed by an acknowledge (ACK) bit. The acknowledge bit is controlled by the recipient of the data by holding the SDA line low to acknowledge the correct receipt of a data byte. A not-acknowledged (NACK) bit can be signalled by leaving the SDA line floating during the 9th SCL clock cycle. A not-acknowledge can be used to indicate several conditions depending on the nature of the transaction and data content.

Address Decoding

After a start condition from the master indicates the beginning of a frame, the master must then send an address byte to the slave. The address byte is formatted as shown in Figure 59. The first seven bits contain the address of the target slave device with the msb first. The eighth bit indicates the type of transaction required: a '0' indicates a write (master writes to slave) and a '1' indicates a read (master reads from slave). If no slave on the bus matches the address sent, then the SDA line will be left floating and therefore the master receives a NACK back. The master must then send a stop condition. If a slave does appear on the bus with the target address then it must pull down the SDA line thus sending an acknowledge back to the master at which point communication between master and slave can proceed depending on the type of transaction requested – write or read.

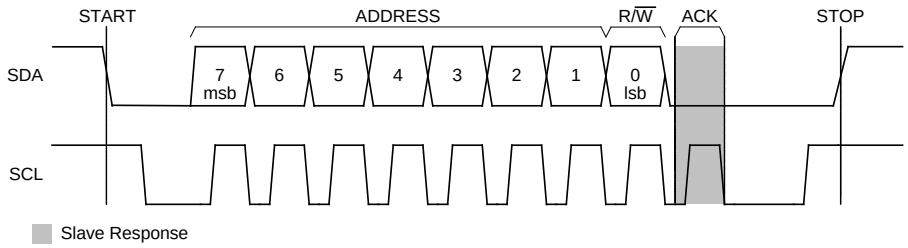


Figure 59 – I^{2}C Address Decoding

Write Transaction

A write transaction is shown below in Figure 60. Communication is initiated by the host master driving the I^2C bus with a start condition. The host master then signals the 7-bit slave (GN25L95) address followed by a write bit, indicating that the host master intends to write data to the slave. The slave then acknowledges the master by holding down the SDA line (shown in grey). The host master then proceeds to write data on to the bus, 8-bits wide with MSB first, and then receives an acknowledge from the slave (again, in grey). The diagram below shows the first byte of data and acknowledge followed by a stop condition.

BYTE WRITE: A single byte write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the GN25L95 will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the GN25L95 will output a zero and the host master device must terminate the write sequence with a stop condition. At this time the GN25L95 enters an internally timed write cycle to the non-volatile memory. All inputs are disabled during this write cycle and the GN25L95 will not respond until the write is complete.

PAGE WRITE: The GN25L95 is capable of an 8-byte page write. A page write is initiated the same as a byte write, but the host master does not send a stop condition after the first data word is clocked in. Instead, after the GN25L95 acknowledges receipt of the first data word, the host master can transmit up to seven data words. The GN25L95 will respond with a zero after each data word received. The host master must terminate the page write sequence with a stop condition to initiate the GN25L95 non-volatile writing process.

The data word address lower three bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight data words are transmitted to the GN25L95, the data word address will “roll over” and previous data will be overwritten.

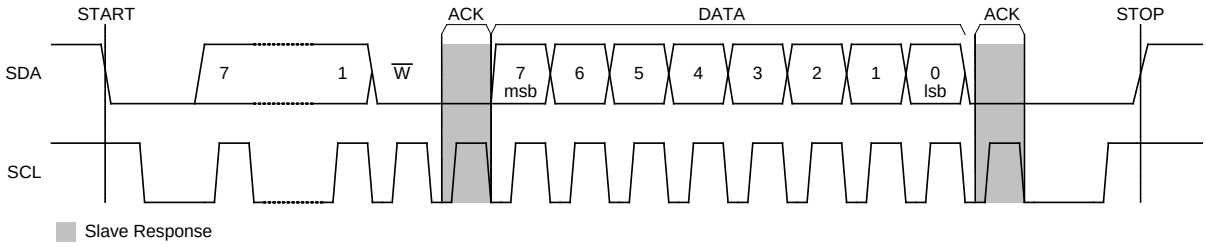


Figure 60 – I^2C Write Transaction

Writing values to 16-bit DACs

The GN25L95 has several DACs that are 16-bits wide and are organised as MSB and LSB bytes (MSB at lower address). These DACs should always be written in one I^2C access in which both the MSB and LSB are written.

Read Transaction

Figure 61 below shows a read transaction. The master sends the slave address followed by a read request bit which is subsequently acknowledged by the slave (the first grey bit). The slave then responds by placing data onto the bus (shown in grey) from the current memory location held in the register address pointer. The master will then hold down the SDA line to acknowledge (shown in white) the successful receipt of the data byte. The process can continue until the master terminates the communication with a stop condition.

To read data from random register addresses the master must first send write to the slave followed by the register address to be read from and a stop condition. The master can then initiate a read frame and the slave will read out consecutive data bytes starting from the register address indicated in the previous write frame.

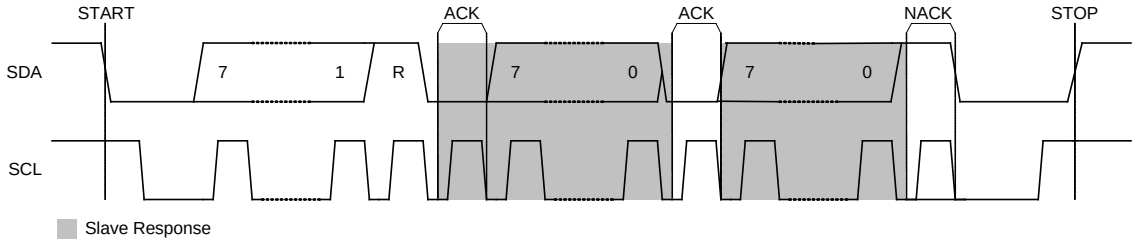


Figure 61 – I^2C Read Transaction

I²C Address Change

The GN25L95 slave I²C interface responds to address A0h and A2h by default. The default addresses can be changed so that the GN25L95 can respond to other address pairs. This feature can be used in CSFP modules where two channels require two separate SFF-8472 DDMI channels.

To change the GN25L95 I²C address the user writes the new base address to register I2C_ADDRESS 195 (C3h) of A2h Table 2. If the GN25L95 is being used with en external EEPROM then the register content will automatically be saved to external EEPROM. If the GN25L95 is being used without external EEPROM then the user needs to initiate an NVM copy of Table 2 to ensure the content of this register are stored in NVM. Since the contents of this register are only read on power-up by the GN25L95 state machine, the GN25L95 will not respond to any new programmed address until the power is cycled.
In order for the new I²C address held in C3h to be used by the GN25L95, then the I2C_PASSWORD byte (C2h) should contain the value C5h. If the I2C_PASSWORD is not set to value C5h then the I2C_ADDRESS value will not be valid and the GN25L95 will continue to use the default I²C addressing.

195	C3h		I2C_ADDRESS	Set the I2C addresses that the GN25L95 responds to.
BIT	R/W	PoR		
7:2	R/W	0	I2C_ADDRESS	Sets I²C address pages for the two memory spaces called A0h and A2h by default. The user can set a new 6 bit address field for the GN25L95 to respond to. Both A0h and A2h locations are changed automatically. This is only read and implemented on power-up. The I²C address does not change dynamically.
1	R/W	0	LOW_PAGE_DIS	Set this bit to disable the GN25L95 lower memory page usually defined at address A0h. This is only read and implemented on power-up. The I²C address does not change dynamically.
0	R/W	0	I2C_TIMEOUT_EN	Set this bit to enable a time out function on the I²C slave interface. If the slave interface clock or data is pulled low for longer than ~20ms then the GN25L95 I²C interface will reset.

The GN25L95 can be used in CSFP applications and supports multiple channel addressing.

The CSFP standard requires that an SFP form factor module contains two separate SFF-8472 DDMI channels which are designated Channel 1 and Channel 2.

An example of CSFP channel 2 I²C addresses are shown below.

CSFP DDMI Channel	Address	"A0 Page"	"A2 Page"	I2C_ADDRESS <7:2>
Channel 1	Default	A0h	A2h	000000b or 101000b
Channel 2	Option 0	B0h	B2h	101100b
	Option 1	10h	12h	000100b
	Option 2	C0h	C2h	110000b
	Option 3	50h	52h	010100b

Table 29 – Example I²C adresses for CSFP applications

In a CSFP application two GN25L95 ICs would be connected to the same host I²C bus. It would be possible to program each GN25L95 individually by powering up each GN25L95 IC one at a time. This enables the user to program each GN25L95 with a different I²C channel address even though both ICs are connected to the same host I²C bus.

Slave I²C Timeout / Recovery

Incorrect operation of the slave I²C interface to the GN25L95 can result in unintended behaviour. This unintended behaviour would be the result of a break in normal communications with the GN25L95 device mid-access. The unintended behaviour could manifest itself by the GN25L95 possibly holding the SDA signal low as it was in the process of clocking out data when the break in communications happened. This could result in the next access to the GN25L95 failing.

The GN25L95 has built in protection that can be enabled to ensure that the slave I²C interface will recover automatically if a break in communications occurs during mid-transaction with the GN25L95. If the user does not want to use the internal protection then a simple recovery sequence can be sent to the GN25L95 device to recover its I²C interface and ensure that any subsequent access will succeed. The two options are detailed below.

1. If the host sets the I2C_TIMEOUT_EN bit then the GN25L95 will monitor the SCL and SDA signals and reset the its slave I²C interface if either of these signals are held low for more than ~20ms. Once this timeout has occurred the GN25L95 will release its control of the SDA signal and go back to the idle state. This will limit the minimum speed that the interface can be operated at to ~25Hz.
2. If the host does not want to use the timeout functionality then a simple recovery sequence can be sent to the GN25L95 device to recover its slave I²C interface. The sequence to be sent by the host is to send a STOP condition followed by 8 clock cycles with the SDA signal not driven. Once sent the host can then resume normal communications with the GN25L95.

Memory Map

The GN25L95 memory can be accessed through register locations addressed via the I²C serial interface. The A0h and A2h memory page organisation is shown in the figure below.

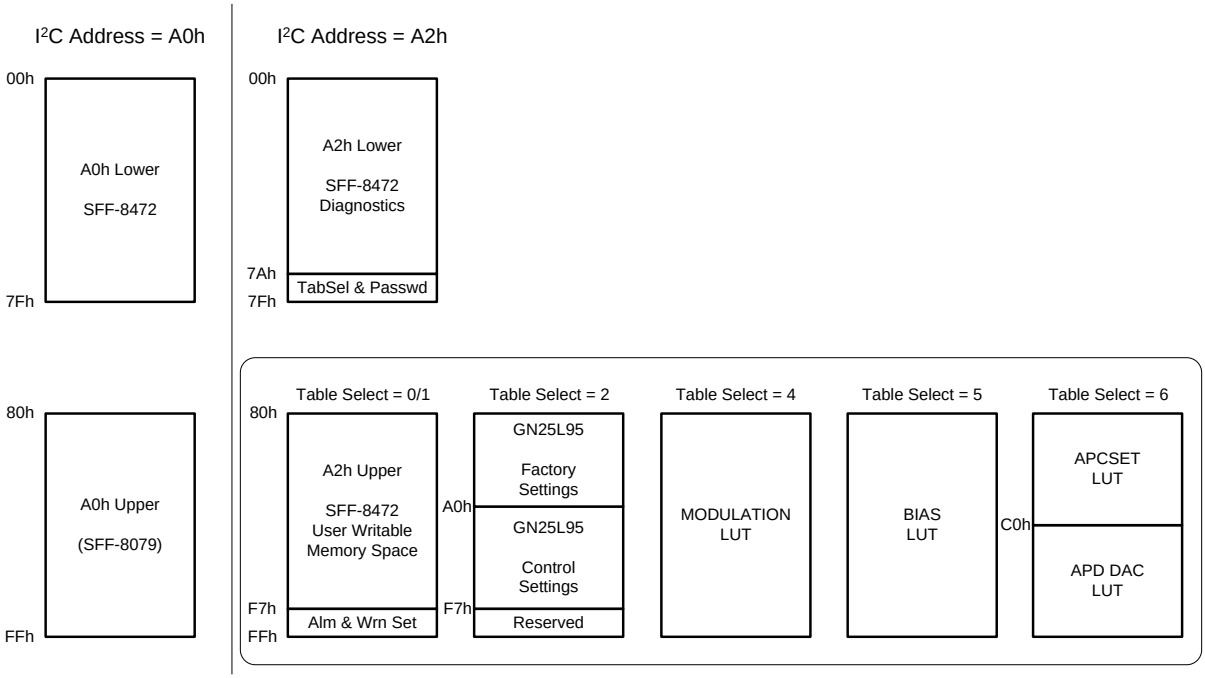


Figure 62 – GN25L95 Register & Memory Structure

Byte 7F of address A2h is used to select further tables that appear at addresses A2h 80h-FFh. The tables that can be addressed along with their functions are described below:

Table 0/1	User Writeable Area
Table 2	GN25L95 Control Settings
Table 4	Modulation LUT
Table 5	Bias LUT
Table 6	APCSET LUT and APD DAC LUT

Password Protection Levels

The GN25L95 supports three levels of password protection so that the GN25L95 user can protect the content of Tables 2, 4, 5 and 6 from the end customer.

The first level of password access only gives the host access to locations at A0h and A2h table 0/1 via the slave I²C interface. The second level of password access gives the host access to all of the memory map excluding the GN25L95 factory settings area at location A2h table 2 (80h to 9Fh). The GN25L95 factory settings area is programmed by Semtech and cannot be accessed by the user.

Table 30 shows the password access codes that need to be written to the Password locations in A2h (Lower) 7Bh to 7Eh to gain access to the GN25L95 memory locations.

PW0 provides the least access to the GN25L95 memory locations and is essentially the default password level set.

Password Level	Access	Byte 7Bh	Byte 7Ch	Byte 7Dh	Byte 7Eh
PW0	A0h, A2h (Lower)	0000h	0000h	0000h	0000h
PW1	A0h, A2h (Lower), A2h (Upper 80h to BFh)	User Set	User Set	User Set	User Set
PW2	A0h, A2h, T2, T4, T5, T6	User Set	User Set	User Set	User Set

Table 30 – Password Levels

The PW1 and PW2 levels can be programmed by the user by setting the 32 bit password level values at locations C9h (PW1) and CDh (PW2) in A2h Table 2.

When the GN25L95 is powered-up the SAFE_MODE_STARTUP byte is read to check that the GN25L95 NVM or EEPROM have been programmed. The user should program this location with the value 6Ah to indicate that the memory content is valid. If the SAFE_MODE_STARTUP byte has not been programmed (i.e. the state after first time initial power-up) then the default password will be FFFFh.

Once the user has determined the GN25L95 user settings and set SAFE_MODE_STARTUP byte to value 6Ah then the GN25L95 passwords will be set to whatever the content of the PW1_VALUE and PW2_VALUE bytes are.

The user can also control write access to various areas of memory by using the WRITE_ACCESS register located at CCh in Table 2 of A2h. This gives the user complete control over what areas of A0h and A2h can be written to by the end customer.

204	CCh		WRITE_ACCESS	Set read only access to A0 and A2 memory locations.
BIT	R/W	PoR		
7	R/W	0	A0h_RD	Set to make the A0h memory page read only.
6	R/W	0	A2h_ALM_WRN_RD	Set to make the Alarm & Warnings section of A2h lower page read only. Registers 00h to 37h
5	R/W	0	A2h_CAL_CON_RD	Set to make the Calibration Constants section of A2h lower page read only. Registers 38h to 5Fh.
4	R/W	0	A2h_RDDMI_RD	Set to make the Real time Diagnostics section of A2h lower page read only. Registers 60h to 6Dh.
3	R/W	0	A2h_80_BF_RD	Set to make registers 80h to BFh of the A2h upper user scratch pad area read only.
2	R/W	0	A2h_C0_F7_RD	Set to make registers C0h to F7h of the A2h upper user scratch pad area read only.
1	R/W	0	A2h_F8_FF_RD	Set to make registers F8h to FFh of the A2h upper user scratch pad area read only.

Copying register memory to NVM

The contents of the register memory can be copied into non-volatile memory by sending I^2C commands to initiate the copy using register NVM_COPY. Once a copy is initiated the register contents are copied into NVM memory. The contents can be copied all in one go, or can be copied one page at a time. The entire copy procedure should take no longer than 1 s. During copying to NVM, the GN25L95 will not acknowledge I^2C transfers. Device polling over I^2C by the host can be used to indicate when the NVM copy has finished. Once the GN25L95 acknowledges an I^2C access it indicates that the NVM copy has completed. The user can then check the NVM_COPY_STATUS register to see whether the copy was successful. The GN25L95 should not be powered-down during the NVM copy procedure.

State Machine Reset Function

The GN25L95 digital state machine can be reset by writing a default code into multiple registers within the memory map. This allows the user to reset the state machine without hardware interaction via the I^2C interface. The soft reset will go through the same reset sequence as on power up.

Register	Location (A2h Lower)	Write Value
PWE (MSB)	7Bh	5Dh
PWE	7Ch	2Ch
PWE	7Dh	6Ah
PWE (LSB)	7Eh	C9h
Table Select	7Fh	0Bh

Table 31 – Soft Reset Write Values & Location for Digital State Machine

As soon as all locations are programmed with the values defined in the table above, the State Machine will reset. Note that the locations can be programmed in any order to invoke a State Machine reset.

Internal Diagnostic Monitoring

The GN25L95 contains a multi-channel 9-bit auto-ranging A/D converter to digitise the following analogue monitors within the IC: supply voltage, transmitter bias current, transmitted output power. The GN25L95 also contains an on-chip temperature sensor which is also digitised using the A/D converter. In conjunction with an external RSSI monitor input, the GN25L95 can digitise the received average power.

In addition to the five monitored functions for SFF-8472, the GN25L95 also provides a digitised monitor of the transmitter modulation current.

Mapping of the ADCs into Register Memory

The GN25L95 digital diagnostic monitors are mapped into 16-bit registers from 232 through to 247 within address A2h Table 2. These are described in the table below.

Register Address	Register Description	Content
232 (E8h)	TEMP MSB	Temperature monitor 16-bit register
233 (E9h)	TEMP LSB	
234 (EAh)	ADC_IN MSB	External ADC input 16-bit register
235 (EBh)	ADC_IN LSB	
236 (ECh)	TX BIAS MSB	Tx bias current monitor 16-bit register
237 (EDh)	TX BIAS LSB	
238 (EEh)	TX POWER MSB	Tx transmitted power monitor 16-bit register
239 (EFh)	TX POWER LSB	
240 (F0h)	RX POWER MSB	Rx RSSI input power 16-bit register
241 (F1h)	RX POWER LSB	
242 (F2h)	TX MOD MSB	Tx modulation current monitor 16-bit register
243 (F3h)	TX MOD LSB	
244 (F4h)	VCC_TX MSB	Tx Supply Voltage monitor 16-bit register
245 (F5h)	VCC_TX LSB	
246 (F6h)	VCC_RX MSB	Rx Supply Voltage monitor 16-bit register
247 F7h)	VCC_RX LSB	

Table 32 – ADC Monitor Register Locations

A description of each of the eight monitors is now provided detailing how to decode each of the 16-bit values.

Temperature Monitor

The temperature monitor can theoretically report temperature from -53.7 °C through to 138.6 °C although this is well beyond the absolute maximum operating range of the GN25L95 IC.

The 9-bit ADC value is mapped to bits 6 to 14 of the ADC_TEMP register with bits 0 to 5 and bit 15 always being set to zero. This gives an equivalent LSB value of (138.6 °C + 53.7 °C) / 32768 = 0.00587 °C/bit with a reporting resolution of ± 0.38 °C.

Lower Range	Upper Range	ADC_TEMP MSB (E8h)								ADC_TEMP LSB (E9h)							
0000h	7FC0h	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-53.7 °C	138.6 °C	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0

Table 33 – Temperature Monitor mapping to TEMP Register

To calculate the temperature from the ADC_ TEMP register value use the formula below:

Temperature (°C) = ADC_TEMP * (192.3 °C / 32768) – 53.7 °C

External ADC input

An external ADC input channel is available for off-chip monitoring of analogue signals – for example an external temperature sensor.

The 9-bit ADC value is mapped to the upper 9 bits of the ADC_IN register with the lower 7 bits always being set to zero. This gives an equivalent LSB value of 2.5V / 65536 = 38 µV/bit with a reporting resolution of ± 4.9 mV.

Lower Range	Upper Range	ADC_IN MSB (EAh)								ADC_IN LSB (EBh)							
0000h	FF80h	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.0 V	2.5 V	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0	0

Table 34 – External ADC input channel mapping to ADC_IN register

To calculate the voltage from the ADC_IN register value use the formula below:

ADC (V) = ADC_IN * (2.5 V / 65536)

Tx Bias Current Monitor

The Tx bias current monitor can report the transmitter bias current from 0.0 mA through to 204.8 mA although the GN25L95 is designed to provide up to 100 mA of bias current.

The 9-bit ADC value is auto-ranged and mapped to five different areas in the 16-bit ADC_TX BIAS register depending on the actual bias current value. Therefore the ADC_TX BIAS register utilises all 16-bits of the register. This gives an equivalent LSB value of 1.6 mA / 512 = 3.125 µA/bit.

Lower Range	Upper Range	ADC_TX_BIAS MSB (ECh)								ADC_TX_BIAS LSB (EDh)							
0000h	FF80h	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.0 mA	1.6 mA	0	0	0	0	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0
1.6 mA	6.4 mA	0	0	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0
6.4 mA	25.6 mA	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0
25.6 mA	102.4 mA	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0
102.4 mA	204.8 mA	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0	0

Table 35 – Tx Bias Current mapping to ADC_TX BIAS Register

The TX BIAS register therefore should be interpreted as follows:

Tx Bias Current (mA) = ADC_TX BIAS * (1.6 mA / 512)

The Tx bias current monitor resolution depends on the actual bias current. For currents less than 1.6 mA the resolution will be ± 3.125 µA. For currents between 1.6 mA and 6.4 mA the resolution will be ± 12.5 µA. For currents between 6.4 mA and 25.6 mA the resolution will be ± 50 µA. For currents between 25.6 mA and 102.4 mA the resolution will be ± 0.2 mA. For currents between 102.4 mA and 204.8 mA the resolution will be ± 0.4 mA. In practice the ADC_TX BIAS value should never result in a value equivalent to 100 mA or greater. Therefore bit 15 of ADC_TX BIAS register will likely always remain zero.

The Tx Bias monitor can be forced to report 0000h when the transmitter is disabled, such as during a TX_DISABLE assert or a fault condition, by setting bit TX_POWER_BIAS_ZERO in register STATUS_0.

The content of the calibrated Tx Bias can be selected to report the following two Tx Bias options during BEN de-assert periods:

1. Continuous monitoring of the Tx Bias value.

2. Maintain the last monitored value of Tx Bias during a BEN assert period for a specified period and then force to 0000h. On the next BEN assert period the Tx Bias value is sampled again.

Set bit TX_BIAS_BEN_LATCH in conjunction with BEN_TIME_SEL to enable latching behaviour of the Tx Bias value after the last BEN assert as described in (2) above.

Tx Power Monitor

The GN25L95 transmitted power monitor reports the mean transmitter output power as follows: (1) In non-burst operation the monitor is directly proportional to the mean transmitted output power derived from the monitor feedback current which is constantly maintained by the automatic power control loop. (2) In burst mode operation the monitor is derived from the averaged monitor photocurrent during successive burst-on periods. During a burst-off period, the transmitted power is assumed to be zero and therefore excluded from the averaging function. A voltage proportional to the monitor current is generated internally within the IC and sampled with a capacitor C_{SAMPLE} only when BEN is high. For non-burst operation, BEN is always tied high.

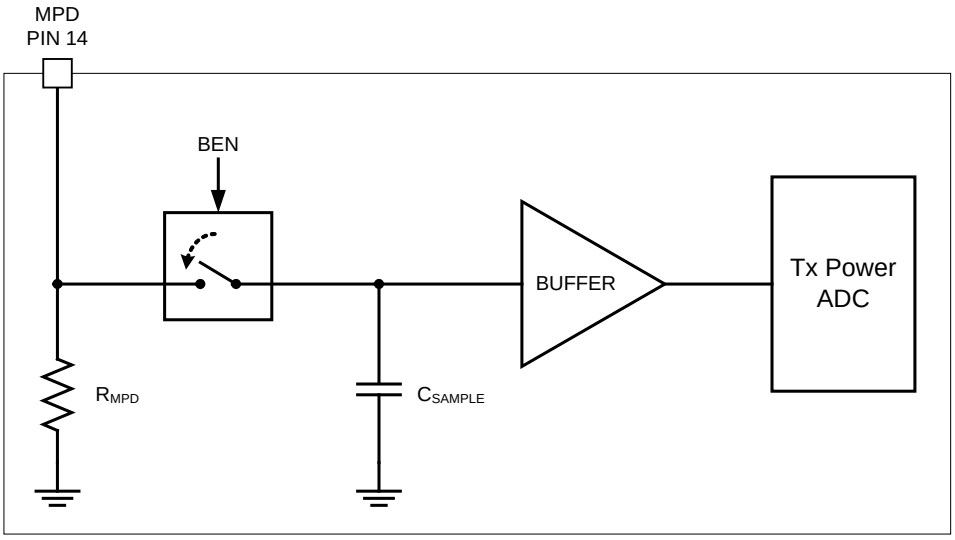


Figure 63 – GN25L95 Burst Tx Power Monitor Functional Diagram

The Tx power monitor can report the monitor photodiode current from 0.0 µA through to 1800.0 µA.

The 9-bit ADC value is auto-ranged and mapped to three different areas in the 16-bit ADC_TX_POWER register depending on the target monitor photodiode current value. The upper three bits of the ADC_TX_POWER register are always zero. This gives an equivalent LSB value of 112.5 µA / 512 = 0.22 µA/bit.

Lower Range	Upper Range	ADC_TX_POWER MSB (EEh)								ADC_TX_POWER LSB (EFh)							
0000h	1FF0h	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.0 µA	112.5 µA	0	0	0	0	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0
112.5 µA	450.0 µA	0	0	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0
450.0 µA	1800.0 µA	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0

Table 36 – Tx Power Monitor mapping to TX POWER Register

The ADC_TX_POWER register therefore should be interpreted as follows:

Monitor Photodiode Diode Current (µA) = ADC_TX_POWER * (112.5 µA / 512)

The Tx power monitor resolution depends on the actual photodiode current. For currents less than 112.5 µA the resolution will be ± 0.22 µA. For currents between 112.5 µA and 450 µA the resolution will be ± 0.88 µA. For currents between 450 µA and 1800 µA the resolution will be ± 3.52 µA.

The Tx Power monitor can be forced to report 0000h when the transmitter is disabled, such as during a TX_DISABLE assert or a fault condition, by setting bit TX_POWER_BIAS_ZERO in register STATUS_0.

The content of the calibrated Tx Power can be selected to report the following two Tx Power options during BEN de-assert periods:

1. Continuous monitoring of the Tx Power value which will fall as the value held on the storage capacitor decays with extended BEN de-assert periods.

2. Maintain the last monitored value of Tx Power during a BEN assert period for a specified period and then force to 0000h. On the next BEN assert period the Tx Power value is sampled again.

Set bit TX_POWER_BEN_LATCH is used in conjunction with BEN_TIME_SEL to enable latching behaviour of the Tx Power value after the last BEN assert as described in (2) above.

Rx Power Monitor

The GN25L95 features a receiver signal strength indicator (RSSI) input for monitoring the current from an external RSSI output from a trans-impedance amplifier (TIA) such as the Semtech NT24L50.
The RSSI input monitor can be configured to accept both Sink (default) or Source output monitors from the preceding TIA. The polarity of the RSSI input is configured to Source mode by setting RSSI_POLARITY. This activates an internal current mirror which changes the input polarity. The maximum current handing capability of the RSSI pin is 8 mA.

The output from the internal RSSI current mirror is fed into an auto-ranging analog-to-digital converter that can digitise TIA monitor currents from 90 nA up to 2 mA – equivalent to an average optical input power range of -40 dBm to +3 dBm (assuming 0.9 A/W responsivity).

The auto-ranger operates continuously and before every ADC sample cycle. This guarantees that the ADC digitised output is monotonic with RSSI input monitor current.

A 10nF capacitor should be connected between the RSSI pin input and ground to reduce noise at the RSSI monitor node as shown in Figure 64.

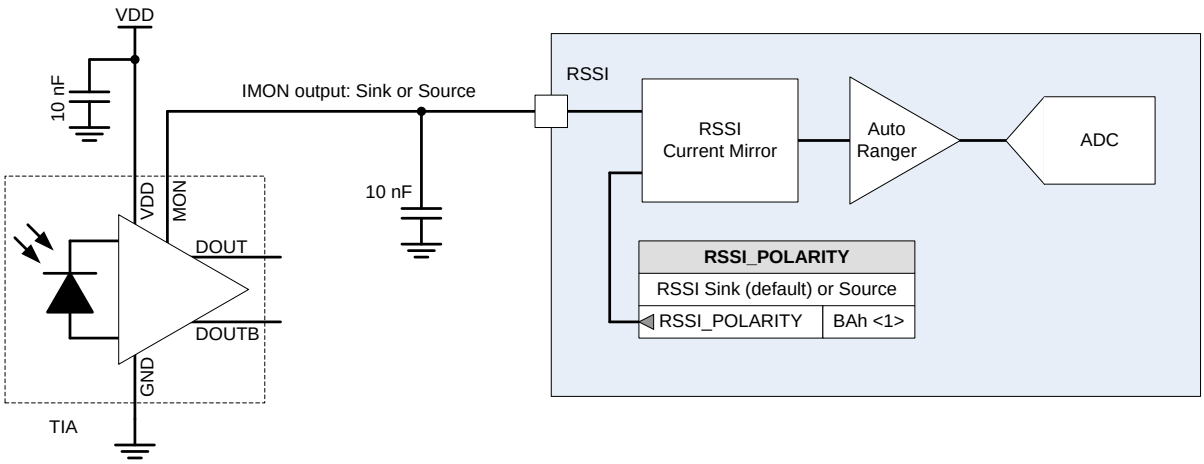


Figure 64 – GN25L95 RSSI Monitor A/D Input

The Rx Power monitor can report the RSSI current up to 2048 µA.

The 9-bit ADC value is auto-ranged and mapped to five different areas in the 16-bit RX POWER register depending on the actual RSSI current value. Therefore the RX POWER register utilises all 16-bits of the register. This gives an equivalent LSB value of 16 µA / 512 = 0.03125 µA/bit.

Lower Range	Upper Range	ADC_RX_POWER MSB (F0h)								ADC_RX_POWER LSB (F1h)							
0000h	FF80h	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0 µA	16 µA	0	0	0	0	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0
16 µA	64 µA	0	0	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0
64 µA	256 µA	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0
256 µA	1024 µA	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0
1024 µA	2048 µA	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0	0

Table 37 – Rx Power mapping to ADC_RX_POWER Register

The ADC_RX_POWER register therefore should be interpreted as follows:

Rx Power [*RSSI*] Current (mA) = ADC_RX_POWER * (16 µA / 512)

The Rx Power current monitor resolution depends on the actual RSSI current. For currents less than 16 µA the resolution will be ± 31.25 nA. For currents between 16 µA and 64 µA the resolution will be ± 125 nA. For currents between 64 µA and 256 µA the resolution will be ± 500 nA. For currents between 256 µA and 1024 µA the resolution will be ± 2 µA. For currents between 1024 µA and 2048 µA the resolution will be ± 4 µA.

Tx Modulation Current Monitor

The Tx modulation current monitor can report the transmitter modulation current from 0.0 mA through to 204.8 mA although the GN25L95 is designed to provide up to 90 mA of modulation current.

The 9-bit ADC value is auto-ranged and mapped to five different areas in the 16-bit ADC_TX_MOD register depending on the actual modulation current value. Therefore the ADC_TX_MOD register utilises all 16-bits of the register. This gives an equivalent LSB value of 1.6 mA / 512 = 3.125 µA/bit.

Lower Range	Upper Range	ADC_TX_MOD MSB (F2h)								ADC_TX_MOD LSB (F3h)							
0000h	FF80h	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.0 mA	1.6 mA	0	0	0	0	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0
1.6 mA	6.4 mA	0	0	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0
6.4 mA	25.6 mA	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0
25.6 mA	102.4 mA	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0
102.4 mA	204.8 mA	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0	0

Table 38 – Tx Modulation Current mapping to ADC_TX_MOD Register

The ADC_TX_MOD register therefore should be interpreted as follows:

Tx Modulation Current (mA) = ADC_TX_MOD * (1.6 mA / 512)

The Tx modulation current monitor resolution depends on the actual modulation current. For currents less than 1.6 mA the resolution will be ± 3.125 µA. For currents between 1.6 mA and 6.4 mA the resolution will be ± 12.5 µA. For currents between 6.4 mA and 25.6 mA the resolution will be ± 50 µA. For currents between 25.6 mA and 102.4 mA the resolution will be ± 0.2 mA. For currents between

102.4 mA and 204.8 mA the resolution will be ± 0.4 mA. In practice the ADC_TX_MOD value should never result in a value equivalent to 90 mA or greater. Therefore bit 15 of ADC_TX_MOD register will likely always remain zero.

Tx Supply Voltage Monitor

The Tx Supply Voltage monitor can report the supply voltage from 2.5 V through to 4 V.

The 9-bit ADC value is mapped to the upper 9 bits of the ADC_VCC_TX register with the lower 7 bits always being set to zero. This gives an equivalent LSB value of 4V / 65536 = 61 µV/bit with a reporting resolution of ± 7.81 mV.

Lower Range	Upper Range	ADC_VCC_TX MSB (F4h)								ADC_VCC_TX LSB (F5h)							
0000h	FF80h	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.0 V	4.0 V	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0	0

Table 39 – Tx Supply Voltage mapping to ADC_VCC_TX Register

To calculate the Tx supply voltage from the ADC_VCC_TX register value use the formula below:

Tx Supply Voltage (V) = VCC_TX * (4 V / 65536)

Rx Supply Voltage Monitor

The Rx Supply Voltage monitor can report the supply voltage from 2.5 V through to 4 V.

The 9-bit ADC value is mapped to the upper 9 bits of the ADC_VCC_RX register with the lower 7 bits always being set to zero. This gives an equivalent LSB value of 4V / 65536 = 61 µV/bit with a reporting resolution of ± 7.81 mV.

Lower Range	Upper Range	ADC_VCC_RX MSB (F6h)								ADC_VCC_RX LSB (F7h)							
0000h	FF80h	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.0 V	4.0 V	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0	0

Table 40 – Rx Supply Voltage mapping to ADC_VCC_RX Register

To calculate the Rx supply voltage from the ADC_ VCC_RX register value use the formula below:

Rx Supply Voltage (V) = VCC_RX * (4 V / 65536)

Register Map

The GN25L95 registers are located at I^2C address A0h and A2h (When using default addresses; see page 68 about changing the default I^2C addressing).

A0h Memory Area

The A0h memory area is completely volatile unless an external EEPROM is used. On power-up the GN25L95 loads the A0h content into the A0h volatile memory area from the external EEPROM. The GN25L95 behaves like a 2K bit EEPROM and requires the user to use byte writes or 8-byte page writes followed by a stop condition to complete a data write into the EEPROM memory.

Programming of the A0h memory area is described elsewhere within this document.

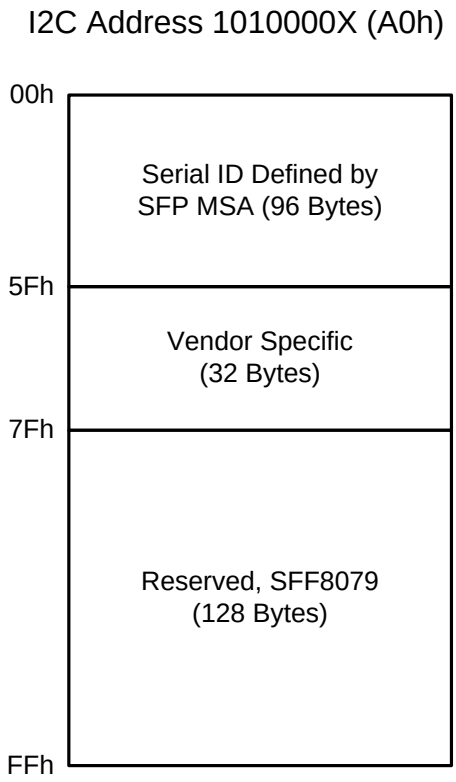


Figure 65 – GN25L95 A0h Memory Map

Refer to the SFF-8472 MSA document for a complete description of the intended content of the A0h memory space.

A2h Memory Area

The A2h memory area is completely volatile unless an external EEPROM is used - apart from the last 8 bytes in A2h that can be backed up in NVM (used to store Alarm & Warning controls). On power-up the GN25L95 loads the A2h content into the A2h volatile memory area from the external EEPROM. The GN25L95 behaves like a 2K bit EEPROM and requires the user to use byte writes or 8-byte page writes followed by a stop condition to complete a data write into the EEPROM memory.

Programming of the A2h memory area is described elsewhere within this document.

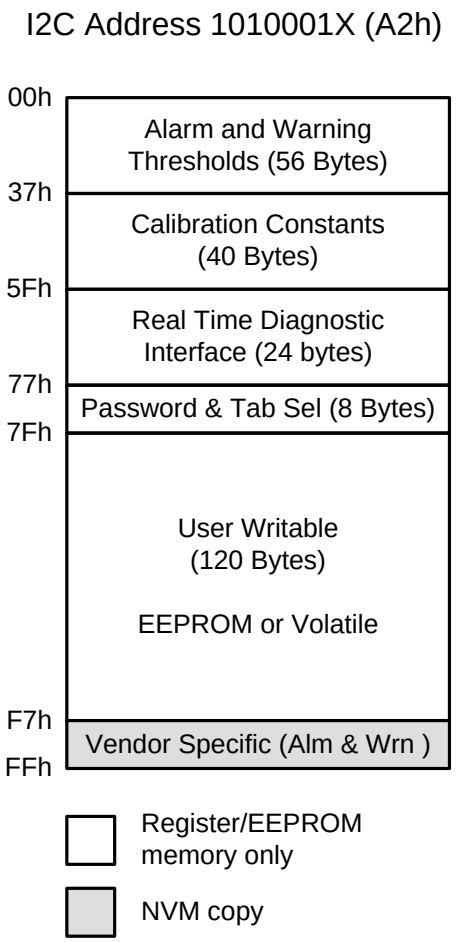


Figure 66 – GN25L95 A2h Memory Map

A2h Lower (00h to 7Fh) Memory Area Register Map

00	00h		Temp High Alarm	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Temperature High Alarm	2 bytes. MSB at low address. Set the temperature high alarm level. This value is compared with the GN25L95 A/D values.

02	02h		Temp Low Alarm	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Temperature Low Alarm	2 bytes. MSB at low address. Set the temperature low alarm level. This value is compared with the GN25L95 A/D values.

04	04h		Temp High Warning	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Temperature High Warning	2 bytes. MSB at low address. Set the temperature high warning level. This value is compared with the GN25L95 A/D values.

06	06h		Temp Low Warning	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Temperature Low Warning	2 bytes. MSB at low address. Set the temperature low warning level. This value is compared with the GN25L95 A/D values.

08	08h		Voltage High Alarm	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Voltage High Alarm	2 bytes. MSB at low address. Set the supply voltage high alarm level. This value is compared with the GN25L95 A/D values.

10	Ah		Voltage Low Alarm	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Voltage Low Alarm	2 bytes. MSB at low address. Set the supply voltage low alarm level. This value is compared with the GN25L95 A/D values.

12	Ch		Voltage High Warning	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Voltage High Warning	2 bytes. MSB at low address. Set the supply voltage high warning level. This value is compared with the GN25L95 A/D values.

14	Eh		Voltage Low Warning	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Voltage Low Warning	2 bytes. MSB at low address. Set the supply voltage low warning level. This value is compared with the GN25L95 A/D values.

16	10h		Bias High Alarm	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Bias High Alarm	2 bytes. MSB at low address. Set the Tx bias high alarm level. This value is compared with the GN25L95 A/D values.

18	12h		Bias Low Alarm	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Bias Low Alarm	2 bytes. MSB at low address. Set the Tx bias low alarm level. This value is compared with the GN25L95 A/D values.

20	14h		Bias High Warning	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Bias High Warning	2 bytes. MSB at low address. Set the Tx bias high warning level. This value is compared with the GN25L95 A/D values.

22	16h		Bias Low Warning	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Bias Low Warning	2 bytes. MSB at low address. Set the Tx bias low warning level. This value is compared with the GN25L95 A/D values.

24	18h		Tx Power High Alarm	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Tx Power High Alarm	2 bytes. MSB at low address. Set the Tx power high alarm level. This value is compared with the GN25L95 A/D values.

26	1Ah		Tx Power Low Alarm	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Tx Power Low Alarm	2 bytes. MSB at low address. Set the Tx power low alarm level. This value is compared with the GN25L95 A/D values.

28	1Ch		Tx Power High Warning	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Tx Power High Warning	2 bytes. MSB at low address. Set the Tx power high warning level. This value is compared with the GN25L95 A/D values.

30	1Eh		Tx Power Low Warning	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Tx Power Low Warning	2 bytes. MSB at low address. Set the Tx power low warning level. This value is compared with the GN25L95 A/D values.

32	20h		Rx Power High Alarm	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Rx Power High Alarm	2 bytes. MSB at low address. Set the Rx power high alarm level. This value is compared with the GN25L95 A/D values.

34	22h		Rx Power Low Alarm	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Rx Power Low Alarm	2 bytes. MSB at low address. Set the Rx power low alarm level. This value is compared with the GN25L95 A/D values.

36	24h		Rx Power High Warning	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Rx Power High Warning	2 bytes. MSB at low address. Set the Rx power high warning level. This value is compared with the GN25L95 A/D values.

38	26h		Rx Power Low Warning	Alarm & Warnings
BIT	R/W	PoR		
15:0	R/W	00h	Rx Power Low Warning	2 bytes. MSB at low address. Set the Rx power low warning level. This value is compared with the GN25L95 A/D values.

56	38h		RX_PWR(4)	External Calibration Constants
BIT	R/W	PoR		
31:0	R/W	00h	Rx Power external calibration constant (4)	4 bytes. Single precision floating point calibration data - Rx optical power. Bit 7 of byte 56 is MSB. Bit 0 of byte 59 is LSB. Rx_PWR(4) should be set to zero for “internally calibrated” devices.

60	3Ch		RX_PWR(3)	External Calibration Constants
BIT	R/W	PoR		
31:0	R/W	00h	Rx Power external calibration constant (3)	4 bytes. Single precision floating point calibration data - Rx optical power. Bit 7 of byte 60 is MSB. Bit 0 of byte 63 is LSB. Rx_PWR(3) should be set to zero for “internally calibrated” devices.

64	40h		RX_PWR(2)	External Calibration Constants
BIT	R/W	PoR		
31:0	R/W	00h	Rx Power external calibration constant (2)	4 bytes. Single precision floating point calibration data, Rx optical power. Bit 7 of byte 64 is MSB, bit 0 of byte 67 is LSB. Rx_PWR(2) should be set to zero for “internally calibrated” devices.

68	44h		RX_PWR(1)	External Calibration Constants
BIT	R/W	PoR		
31:0	R/W	00h	Rx Power external calibration constant (1)	4 bytes. Single precision floating point calibration data, Rx optical power. Bit 7 of byte 68 is MSB, bit 0 of byte 71 is LSB. Rx_PWR(1) should be set to 1 for “internally calibrated” devices.

72	48h		RX_PWR(0)	External Calibration Constants
BIT	R/W	PoR		
31:0	R/W	00h	Rx Power external calibration constant (0)	4 bytes. Single precision floating point calibration data, Rx optical power. Bit 7 of byte 72 is MSB, bit 0 of byte 75 is LSB. Rx_PWR(0) should be set to zero for “internally calibrated” devices.

76	4Ch		Tx_I(Slope)	External Calibration Constants
BIT	R/W	PoR		
15:0	R/W	00h	Tx Bias external calibration constant (Slope)	2 bytes. Fixed decimal (unsigned) calibration data, laser bias current. Bit 7 of byte 76 is MSB, bit 0 of byte 77 is LSB. Tx_I(Slope) should be set to 1 for “internally calibrated” devices.

78	4Eh		Tx_I(Offset)	External Calibration Constants
BIT	R/W	PoR		
15:0	R/W	00h	Tx Bias external calibration constant (Offset)	2 bytes. Fixed decimal (signed two’s complement) calibration data, laser bias current. Bit 7 of byte 78 is MSB, bit 0 of byte 79 is LSB. Tx_I(Offset) should be set to zero for “internally calibrated” devices.

80	50h		Tx_PWR(Slope)	External Calibration Constants
BIT	R/W	PoR		
15:0	R/W	00h	Tx Power external calibration constant (Slope)	2 bytes. Fixed decimal (unsigned) calibration data, transmitter coupled output power. Bit 7 of byte 80 is MSB, bit 0 of byte 81 is LSB. Tx_PWR(Slope) should be set to 1 for “internally calibrated” devices.

82	52h		Tx_PWR(Offset)	External Calibration Constants
BIT	R/W	PoR		
15:0	R/W	00h	Tx Power external calibration constant (Offset)	2 bytes. Fixed decimal (signed two’s complement) calibration data, transmitter coupled output power. Bit 7 of byte 82 is MSB, bit 0 of byte 83 is LSB. Tx_PWR(Offset) should be set to zero for “internally calibrated” devices.

84	54h		T(Slope)	External Calibration Constants
BIT	R/W	PoR		
15:0	R/W	00h	Temperature external calibration constant (Slope)	2 bytes. Fixed decimal (unsigned) calibration data, internal module temperature. Bit 7 of byte 84 is MSB, bit 0 of byte 85 is LSB. T(Slope) should be set to 1 for “internally calibrated” devices.

86	56h		T(Offset)	External Calibration Constants
BIT	R/W	PoR		
15:0	R/W	00h	Temperature external calibration constant (Offset)	2 bytes. Fixed decimal (signed two’s complement) calibration data, internal module temperature. Bit 7 of byte 86 is MSB, bit 0 of byte 87 is LSB. T(Offset) should be set to zero for “internally calibrated” devices.

88	58h		V(Slope)	External Calibration Constants
BIT	R/W	PoR		
15:0	R/W	00h	Supply voltage external calibration constant (Slope)	2 bytes. Fixed decimal (signed two's complement) calibration data, internal module temperature. Bit 7 of byte 86 is MSB, bit 0 of byte 87 is LSB. T(Offset) should be set to zero for "internally calibrated" devices.

90	5Ah		V(Offset)	External Calibration Constants
BIT	R/W	PoR		
15:0	R/W	00h	Supply voltage external calibration constant (Offset)	2 bytes. Fixed decimal (signed two's complement) calibration data, internal module supply voltage. Bit 7 of byte 90 is MSB. Bit 0 of byte 91 is LSB. V(Offset) should be set to zero for "internally calibrated" devices.

95	5Fh		Checksum	Checksum
BIT	R/W	PoR		
7:0	R/W	00h	Checksum	Byte 95 contains the low order 8 bits of the sum of bytes 0-94. Set by the user.

96	60h		Temperature	Converted Analogue Values
BIT	R/W	PoR		
15:0	R	00h	Temperature reading	Internally measured temperature. 2 bytes, MSB at lower byte. Twos complement value.

98	62h		VCC	Converted Analogue Values
BIT	R/W	PoR		
15:0	R	00h	Supply voltage reading	Internally measured supply voltage. 2 bytes, MSB at lower byte. Unsigned value.

100	64h		Tx Bias	Converted Analogue Values
BIT	R/W	PoR		
15:0	R	00h	Tx bias current reading	Internally measured Tx bias current. 2 bytes, MSB at lower byte. Unsigned value.

102	66h		Tx Power	Converted Analogue Values
BIT	R/W	PoR		
15:0	R	00h	Tx power current reading	Internally measured Tx power. 2 bytes, MSB at lower byte. Unsigned value.

104	68h		Rx Power	Converted Analogue Values
BIT	R/W	PoR		
15:0	R	00h	Rx power current reading	Internally measured Rx power. 2 bytes, MSB at lower byte. Unsigned value.

110	6Eh		Status & Control	Status & Control
BIT	R/W	PoR		
7	R	0	TX_DISABLE_STATE	Digital state of the TX_DISABLE input pin. Updated within 100ms of change on pin.
6	R/W	0	SOFT_TX_DISABLE	Enables direct control of the transmitter via I^2C. Set to '1' to disable the transmitter. This bit is "OR"d with the hard TX_DISABLE pin. Soft assert & de-assert within 100ms of I^2C command.
5	R/W	0	ROGUE_ONU	GN25L95 sets this bit to '1' on the occurrence of a rogue ONU condition. Set to'0' to reset.
4	R/W	0	N/A	
3	R/W	0	ROGUE_TXP_LO_FLAG	Set to 1 if the TXP_LO_FLAG has been set by the alarm threshold and the ROGUE_TXP_LO_EN bit is set. Latched.
2	R	0	TX_FAULT_STATE	Digital state of the TX_FAULT output pin. Updated within 100ms of change on pin.
1	R	0	RX_LOS_STATE	Digital state of the RX_LOS output pin. Updated within 100ms of change on pin.
0	R	0	DATA_READY_BAR_ STATE	Indicates GN25L95 has achieved power and data is ready. Bit stays high until data is ready at which time the GN25L95 sets this bit low.

111	6Fh		PON Control	PON Control * HOST_PON_EN bit must be set to enable this register
BIT	R/W	PoR		
7	R/W	0	N/A	
6	R/W	0	TX_FAST_SLEEP	Default '0' means on de-assert of TX_SLEEP, Tx implements a reset start. Set to '1' to enable the Tx to use the last known bias & mod values.
5	R/W	0	RX_SLEEP_ASSERT	Set to '1' to assert RX_SLEEP mode
4	R	0	RX_SLEEP_STATE	Digital state of the RX_SLEEP input pin. Updated within 100ms of change on pin.
3	R/W	0	TX_SLEEP_ASSERT	Set to '1' to assert TX_SLEEP mode
2	R	0	TX_SLEEP_STATE	Digital state of the TX_SLEEP input pin. Updated within 100ms of change on pin (only valid if Tx sleep mode is enabled)
1:0	R/W	0	POW_LEV	Sets the GPON power level control: 00 = 0dB; 01= -3dB; 11 = -6dB.

112	70h		Alarm Flags 1	Alarm & Warning Flags
BIT	R/W	PoR		
7	R/W	0	Temp High Alarm	Set when temperature exceeds high alarm level
6	R/W	0	Temp Low Alarm	Set when temperature exceeds low alarm level
5	R/W	0	VCC High Alarm	Set when supply voltage exceeds high alarm level
4	R/W	0	VCC Low Alarm	Set when supply voltage exceeds low alarm level
3	R/W	0	Tx Bias High Alarm	Set when Tx bias exceeds high alarm level
2	R/W	0	Tx Bias Low Alarm	Set when Tx bias voltage exceeds low alarm level
1	R/W	0	Tx Power High Alarm	Set when Tx power exceeds high alarm level
0	R/W	0	Tx Power Low Alarm	Set when Tx power voltage exceeds low alarm level

113	71h		Alarm Flags 2	Alarm & Warning Flags
BIT	R/W	PoR		
7	R/W	0	Rx Power High Alarm	Set when Rx power exceeds high alarm level
6	R/W	0	Rx Power Low Alarm	Set when Rx power voltage exceeds low alarm level
5:0	R/W	0	Reserved	

114	72h		Timer Setup	Rogue ONU Setup Timer * HOST_PON_EN bit must be set to enable this register
BIT	R/W	PoR		
7:4	R/W	0	Timer Setup	Rogue ONU Timer. Sets the interval time for counters located at 78h and 79h. 4 timer setup values are programmable: 80h = 40ms, 40h = 80ms, 20h = 160ms, 10h = 320ms.
3:0	R/W	0	Reserved	

116	74h		Warning Flags 1	Alarm & Warning Flags
BIT	R/W	PoR		
7	R/W	0	Temp High Warning	Set when temperature exceeds high warning level
6	R/W	0	Temp Low Warning	Set when temperature exceeds low warning level
5	R/W	0	VCC High Warning	Set when supply voltage exceeds high warning level
4	R/W	0	VCC Low Warning	Set when supply voltage exceeds low warning level
3	R/W	0	Tx Bias High Warning	Set when Tx bias exceeds high warning level
2	R/W	0	Tx Bias Low Warning	Set when Tx bias voltage exceeds low warning level
1	R/W	0	Tx Power High Warning	Set when Tx power exceeds high warning level
0	R/W	0	Tx Power Low Warning	Set when Tx power voltage exceeds low warning level

117	75h		Warning Flags 2	Alarm & Warning Flags
BIT	R/W	PoR		
7	R/W	0	Rx Power High Warning	Set when Rx power exceeds high warning level
6	R/W	0	Rx Power Low Warning	Set when Rx power voltage exceeds low warning level
5:0	R/W	0	Reserved	

120	78h		ONU FAULT Delay Timer	Rogue ONU FAULT Delay Timer * HOST_PON_EN bit must be set to enable this register
BIT	R/W	PoR		
7:0	R/W	0	ONU_FAULT_DELAY	This time is used to count the basic unit timer in register 72h (114) and multiplies the time by the value contained within this register. So a value of 08h would result in an ONU_FAULT_DELAY time of 320ms (assuming register 72h is set to 40ms). This timer then provides a hold-off value between a ROGUE_ONU event occurring and an ONU_FAULT being communicated.

121	79h		TXOFF Delay Timer	Rogue ONU TX_DISABLE Delay Timer * HOST_PON_EN bit must be set to enable this register
BIT	R/W	PoR		
7:0	R/W	0	TXOFF Delay Timer	This time is used to count the basic unit timer in register 72h (114) and multiplies the time by the value contained within this register. So a value of 08h would result in a TXOFF Delay time of 320ms (assuming register 72h is set to 40ms). This timer then provides a hold-off value between a ROGUE_ONU event occurring and a TX_DISABLE being asserted.

123	7Bh		PWE	Password Entry
BIT	R/W	PoR		
31:0	W	0	PWE	32 bit password entry double word. Set to all ‘1’s on power-up.

127	7Fh		Table Select	Table Select
BIT	R/W	PoR		
7:0	R/W	0	Table Select Byte	This byte selects the A2 table memory area to be accessed via addresses A2h, 80h to FFh. 00h/01h = User A2 Upper page (as per SFF-8472) 02h = GN25L95 Control & Status page 04h = Modulation Look-Up Table 05h = Bias Look-Up Table 06h = APCSET and APD DAC Look-Up Tables 0Bh = State Machine Reset Function Note: The upper nibble is unused and will be ignored.

A2h Upper (80h to FFh) Memory Area Register Map

This memory area is accessed by setting Table Select byte (7Fh) to 0 or 1.

The A2h upper memory area is divided into 3 separately protected areas:

A2h Upper Memory – User Scratch Area [PW1]				
BYTE	**BIT**	**PoR**	**NAME**	**DESCRIPTION**
80h to BFh	All	0	USER_SCRATCH_PW1	PW1 protected memory scratch pad area. Password protection optional and set using controls in A2h Table 2, register C4h.

A2h Upper Memory – User Scratch Area [PW2]				
BYTE	**BIT**	**PoR**	**NAME**	**DESCRIPTION**
C0h to F7h	All	0	USER_SCRATCH_PW2	PW2 protected memory scratch pad area. Password protection optional and set using controls in A2h Table 2, register C4h.

A2h Upper Memory – Vendor Specific Area [PW2] (Alarm & Warning Flag Enable controls)				
BYTE	**BIT**	**PoR**	**NAME**	**DESCRIPTION**
F8h to FFh	All	0	ALM_WRN_FLAG_EN	PW2 protected vendor specific area. Password protection optional and set using controls in A2h Table 2, register C4h.

The Vendor Specific memory area (F8h to FFh) is password protected to PW2 (when EE_ACCESS <1> is set) and is used to set the alarm and warning flag enables controls. Details of this memory area are shown below.

248	**F8h**		**ALARM_ENABLE_1**	**Alarm & Warning flags enable**
BIT	**R/W**	**PoR**		
7	R/W	0	ALM_EN_TEMP_HIGH	Set to enable temperature high alarm flag
6	R/W	0	ALM_EN_TEMP_LOW	Set to enable temperature low alarm flag
5	R/W	0	ALM_EN_VCC_HIGH	Set to enable supply voltage high alarm flag
4	R/W	0	ALM_EN_VCC_LOW	Set to enable supply voltage low alarm flag
3	R/W	0	ALM_EN_TXB_HIGH	Set to enable Tx bias high alarm flag
2	R/W	0	ALM_EN_TXB_LOW	Set to enable Tx bias low alarm flag
1	R/W	0	ALM_EN_TXP_HIGH	Set to enable Tx power high alarm flag
0	R/W	0	ALM_EN_TXP_LOW	Set to enable Tx power alarm flag

249	**F9h**		**ALARM_ENABLE_2**	**Alarm & Warning flags enable**
BIT	**R/W**	**PoR**		
7	R/W	0	ALM_EN_RXP_HIGH	Set to enable Rx power high alarm flag
6	R/W	0	ALM_EN_RXP_LOW	Set to enable Rx power alarm flag
5:0	R/W	0	Reserved	

250	**FAh**		**Reserved**	
BIT	**R/W**	**PoR**		
7:0	R/W	0	Reserved	

251	FBh		Reserved	
BIT	R/W	PoR		
7:0	R/W	0	Reserved	

252	FCh		WARNING_ENABLE_1	Alarm & Warning flags enable
BIT	R/W	PoR		
7	R/W	0	WRN_EN_TEMP_HIGH	Set to enable temperature high warning flag
6	R/W	0	WRN _EN_TEMP_LOW	Set to enable temperature low warning flag
5	R/W	0	WRN _EN_VCC_HIGH	Set to enable supply voltage high warning flag
4	R/W	0	WRN _EN_VCC_LOW	Set to enable supply voltage low warning flag
3	R/W	0	WRN _EN_TXB_HIGH	Set to enable Tx bias high warning flag
2	R/W	0	WRN _EN_TXB_LOW	Set to enable Tx bias low warning flag
1	R/W	0	WRN _EN_TXP_HIGH	Set to enable Tx power high warning flag
0	R/W	0	WRN _EN_TXP_LOW	Set to enable Tx power warning flag

253	FDh		WARNING_ENABLE_2	Alarm & Warning flags enable
BIT	R/W	PoR		
7	R/W	0	WRN _EN_RXP_HIGH	Set to enable Rx power high warning flag
6	R/W	0	WRN _EN_RXP_LOW	Set to enable Rx power warning flag
5:0	R/W	0	Reserved	

254	FEh		Reserved	
BIT	R/W	PoR		
7:0	R/W	0	Reserved	

255	FFh		Reserved	
BIT	R/W	PoR		
7:0	R/W	0	Reserved	

A2h Table 2 – GN25L95 Control Settings

The GN25L95 control settings are contained at address A2h within Table 2, from A0h to FFh. This is accessed by writing 02h to the table select byte at address A2h, register 7Fh.

The on-chip NVM allows the user to re-write the content in A2h Table 2 up to 2x. If multiple re-writing of this memory area is required then the user should use an external 8k EEPROM connected to the GN25L95.

Note that Table 2 is Password Level 2 protected.

160	**A0h**		SAFE_MODE_ STARTUP	**Safe Mode Startup**
BIT	**R/W**	**PoR**		
7:0	R/W	0	SAFE_MODE_ STARTUP	Set to value 6Ah to enable transmitter and normal user mode. If the correct value is not set then the transmitter will be permanently disabled and the password level set to PW2 on power on. The I2C address is permanently set to the default address of A0h/A2h.

161	**A1h**		**TX_CTRL_0**	**Transmitter controls**
BIT	**R/W**	**PoR**		
7	R/W	0	TX_DISABLE_ON_RX_ LOS	Set to enable the enable the transmitter to be disabled on assertion of the Rx LOS output.
6	R/W	0	LASER_AC	Set if interfacing a laser using AC coupling. The default is DC coupling.
5	R/W	0	FORCE_BEN_ON	Set to force continuous operation of the transmitter (i.e. non burst applications)
4	R/W	0	TX_MOD_STEER	Set to invert the modulation current steering during BEN de-assert
3	R/W	0	TX_MOD_SPLIT	Set to split the modulation current equally between LASER+ and LASER- when the TXIN± is below a preset level.
2	R/W	0	TX_BURST_POLARITY	Set to invert the Tx BEN± input polarity.
1	R/W	0	TX_DATA_POLARITY	Set to invert the TXIN± data input polarity.
0	R/W	0	BURST_POWER_SAVE	Set to turn off the bias and modulation currents fully during a BEN de-assert.

162	**A2h**		**TX_CTRL_1**	**Transmitter controls**
BIT	**R/W**	**PoR**		
7:4	R/W	0	TX_CROSSING	Set to adjust the modulation output crossing point.
3:1	R/W	0	BACK_TERM	Set to adjust the value of the passive or active back termination present at the LASER± outputs. Setting to 0 disables back termination.
0	R/W	0	BACK_TERM_TYPE	Set to change from passive (default) to active back termination on the LASER± outputs.

163	A3h		APC_CTRL	APC loop controls
BIT	R/W	PoR		
7:6	R/W	0	COUNT_INC	Set the step size during an APC fast start.
5:4	R/W	0	DIG_AVG_SET	Set the threshold for the APC digital-averaging counter of the APC control loop.
3	R/W	0	DIG_AVG_EN	Set to enable digital averaging of the APC control loop.
2:1	R/W	0	APC_CLOCK_SET	Set the APC and ERC sampling clock rate after APC fast-start. Default is maximum.
0	R/W	0	LOOP_START	Set to apply slow clock during APC loop fast-start. Values set by APC_CLOCK. Default is to use 11MHz clock.

164	A4h		TX_TEMP_CTRL	Transmitter temperature compensation control
BIT	R/W	PoR		
7	R/W	0	BIAS_LUT_EN	Set to enable bias look-up table.
6	R/W	0	MOD_LUT_EN	Set to enable modulation look-up table.
5	R/W	0	BIAS_LUT_INTERPOL	Set to enable bias LUT interpolation.
4	R/W	0	MOD_LUT_INTERPOL	Set to enable modulation LUT interpolation.
3	R/W	0	APC_LUT_EN	Set to enable APC look-up table
2	R/W	0	APC_EN	Set to enable automatic power control
1	R/W	0	APC_FAST_VAL	Set to use the modulation LUT as the source for the initial seed for the APC Fast start. Default is to use the bias LUT.
0	R/W	0	APC_FAST_EN	Set to enable APC fast start.

165	A5h		AUTO_ER_CTRL	Automatic extinction ratio control
BIT	R/W	PoR		
7:4	R/W	0	TARGET_ER_SET	Sets the target extinction ratio. Values to be set from 0000 to 1111: 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,16, 18, 20, 22, 25, 28. [eqv to 7dB to 14.5dB]
3:2	R/W	0	MOD_DAC_SETUP	Set full-scale range and response shape of Modulation current DAC.
1	R/W	0	ERC_FAST_EN	Set to enable ERC fast start
0	R/W	0	AUTO_ER_EN	Set to enable automatic extinction ratio control

166	A6h		AUTO_ER_1	Automatic extinction ratio control
BIT	R/W	PoR		
7:6	R/W	0	ERC_AVG_SET	Set the threshold for the ERC digital-averaging counter of the ERC control loop.
5	R/W	0	ERC_AVG_EN	Set to enable digital averaging of the ERC loop.
4:3	R/W	0	TX_DATA_RATE	Sets the Tx data rate for the ERC loop. 00=1.25G>2.5G; 01=625M>1.25G; 10=312M>625M; 11=155M>312M
2	R/W	0	ERC_LOOP_START	Set to apply digital averaging during ERC fast-start.
1:0	R/W	0	ERC_COUNT_INC	Set the step size during an ERC fast start.

167	A7h		AUTO_ER_2	Automatic extinction ratio control * Semtech will provide default values for this register
BIT	R/W	PoR		
7:0	R/W	0	Reserved	Reserved

168	A8h		APCSET_DAC	Automatic power control DAC
BIT	R/W	PoR		
7:0	R/W	0	APCSET_DAC	Sets the target APC reference monitor current.

169	A9h		BIAS_DAC	Bias current DAC
BIT	R/W	PoR		
15:6	R/W	0	BIAS_DAC	Sets the bias current DAC value. The BIAS_DAC is a 16 bit register with the MSB at the lower address and the LSB at the upper address. In LUT mode or APC mode the user can read back the value in this DAC set by the GN25L95.

171	ABh		MOD_DAC	Modulation current DAC
BIT	R/W	PoR		
15:6	R/W	0	MOD_DAC	Sets the modulation current DAC value. The MOD_DAC is a 16 bit register with the MSB at the lower address and the LSB at the upper address. In LUT mode or APC mode the user can read back the value in this DAC set by the GN25L95.

173	ADh		MD_MAX	Monitor photodiode current maximum
BIT	R/W	PoR		
7:2	R/W	0	MD_MAX	Sets the maximum allowed monitor photodiode current. Setting all ‘1s’ disables this function.
1	R/W	0	NOFAULT_BIASMAX	Set to inhibit the BIASMAX function generating a TX_FAULT if the value is exceeded.
0	R/W	0	NOFAULT_MDMAX	Set to inhibit the MDMAX function generating a TX_FAULT if the value is exceeded.

174	AEh		BIAS_MAX	Bias current maximum
BIT	R/W	PoR		
7:0	R/W	0	BIAS_MAX	Sets the maximum allowed bias current. Setting FFh disables this function.

175	AFh		MOD_MAX	Modulation current maximum
BIT	R/W	PoR		
7:0	R/W	0	MOD_MAX	Sets the maximum allowed modulation current. Setting FFh disables this function.

176	B0h		AUTO_ER_3	Automatic extinction ratio control * Semtech will provide default values for these register bits
BIT	R/W	PoR		
7:6	R/W	0	BIAS_DAC_SETUP	Set full-scale range and response shape of Bias current DAC.
5:0	R/W	0	Reserved *	Reserved

177	B1h		TX_SD_CTRL	TX_SD Controls
BIT	R/W	PoR		
7	R/W	0	SHUTDOWN_OUTPUT_EN	Set this bit to use the TX_SD output as an eye safety controlled SHUTDOWN output. Use with an external FET
6:5	R/W	0	TX_SD_VF_THRESH	Set the TX_SD threshold level when using laser forward voltage to trigger the TX_SD monitor.
4:2	R/W	0	TX_SD_MPD_THRESH	Set the TX_SD threshold when using the MPD input to trigger the TX_SD monitor. Setting corresponds to a proportion of the APCSET current. 000 = 2.5% 001 = 5% … 111 = 20%
1	R/W	0	TX_SD_MODE	Set to change the TX_SD monitor trigger from MPD (default) to Laser forward voltage.
0	R/W	0	TX_SD_POLARITY	Set to invert the TX_SD output polarity

178	B2h		TX_FAULT_CTRL	Transmitter fault controls
BIT	R/W	PoR		
7	R/W	0	VCC_DIS_INHIBIT	Set to inhibit TX_DISABLE assert on VCC fault.
6	R/W	0	VCC_FAULT_INHIBIT	Set to inhibit GN25L95 VCC fault monitoring.
5	R/W	0	Reserved	Reserved
4	R/W	0	SHUTDOWN_INHIBIT	Set to inhibit shutdown of laser current during fault.
3	R/W	0	LATCH_INHIBIT	Set to inhibit eye safety latching fault functionality.
2	R/W	0	FAULT_INHIBIT	Set to inhibit eye safety logic functionality.
1	R/W	0	TX_FAULT_TYPE	Set to change the TX_FAULT output type from open drain (default) to LVTTL.
0	R/W	0	TX_FAULT_POLARITY	Set to invert the TX_FAULT output pin polarity

179	B3h		ALM_WRN_CTRL_1	Alarm and warning controls
BIT	R/W	PoR		
7	R/W	0	BIAS_OFF	Set to turn off the bias current
6	R/W	0	MOD_OFF	Set to turn off the modulation current
5	R/W	0	WRN_LATCH	Set to enable latching behaviour of the warning flags.
4	R/W	0	ALM_LATCH	Set to enable latching behaviour of the alarm flags.
3	R/W	0	WRN_TEMP_FAULT	Set to generate a TX_FAULT assert on the occurrence of a temperature warning flag being set.
2	R/W	0	WRN_TEMP_DISABLE	Set to disable the transmitter outputs on the occurrence of a temperature warning flag being set.
1	R/W	0	ALM_TEMP_FAULT	Set to generate a TX_FAULT assert on the occurrence of a temperature alarm flag being set.
0	R/W	0	ALM_TEMP_DISABLE	Set to disable the transmitter outputs on the occurrence of a temperature alarm flag being set.

180	B4h		ALM_WRN_CTRL_2	Alarm and warning controls
BIT	R/W	PoR		
7	R/W	0	WRN_VCC_FAULT	Set to generate a TX_FAULT assert on the occurrence of a supply voltage warning flag being set.
6	R/W	0	WRN_VCC_DISABLE	Set to disable the transmitter outputs on the occurrence of a supply voltage warning flag being set.
5	R/W	0	ALM_VCC_FAULT	Set to generate a TX_FAULT assert on the occurrence of a supply voltage alarm flag being set.
4	R/W	0	ALM_VCC_DISABLE	Set to disable the transmitter outputs on the occurrence of a supply voltage alarm flag being set.
3	R/W	0	WRN_BIAS_FAULT	Set to generate a TX_FAULT assert on the occurrence of a Tx bias warning flag being set.
2	R/W	0	WRN_BIAS_DISABLE	Set to disable the transmitter outputs on the occurrence of a Tx bias warning flag being set.
1	R/W	0	ALM_BIAS_FAULT	Set to generate a TX_FAULT assert on the occurrence of a Tx bias alarm flag being set.
0	R/W	0	ALM_BIAS_DISABLE	Set to disable the transmitter outputs on the occurrence of a Tx bias alarm flag being set.

181	B5h		ALM_WRN_CTRL_3	Alarm and warning controls
BIT	R/W	PoR		
7	R/W	0	WRN_TXP_FAULT	Set to generate a TX_FAULT assert on the occurrence of a Tx power warning flag being set.
6	R/W	0	WRN_TXP_DISABLE	Set to disable the transmitter outputs on the occurrence of a Tx power warning flag being set.
5	R/W	0	ALM_TXP_FAULT	Set to generate a TX_FAULT assert on the occurrence of a Tx power alarm flag being set.
4	R/W	0	ALM_TXP_DISABLE	Set to disable the transmitter outputs on the occurrence of a Tx power alarm flag being set.
3	R/W	0	WRN_RXP_FAULT	Set to generate a TX_FAULT assert on the occurrence of an Rx power warning flag being set.
2	R/W	0	WRN_RXP_DISABLE	Set to disable the transmitter outputs on the occurrence of an Rx power warning flag being set.
1	R/W	0	ALM_RXP_FAULT	Set to generate a TX_FAULT assert on the occurrence of an Rx power alarm flag being set.
0	R/W	0	ALM_RXP_DISABLE	Set to disable the transmitter outputs on the occurrence of an Rx power alarm flag being set.

182	B6h		ROGUE_ONU_CTRL	Rogue ONU controls
BIT	R/W	PoR		
7:3	R/W	0	Reserved	Reserved
2	R/W	0	HOST_PON_EN	Set to enable PON control functions in A2 lower registers: 6Fh, 72h, 78h, 79h.
1	R/W	0	ROGUE_TXP_LO_EN	Set to generate a ROGUE_ONU event on Tx Power Low Alarm assertion.
0	R/W	0	TX_DIS_ONU_CLR_EN	Set to enable clearing of ROGUE_ONU flag by toggling of TX_DISABLE function.

183	B7h		ROGUE_ONU_MON	Rogue ONU monitoring control
BIT	R/W	PoR		
7	R	0	BEN_STATUS	Reports the current status of the BEN function.
6	R/W	0	BEN_TOGGLE	Reports activity on the BEN inputs.
5	R	0	TX_SD_PIN	Reports current status of the TX_SD pin.
4	R/W	0	ROGUE_TX_DIS	Set to disable the transmitter if a ROGUE_ONU_FLAG occurs.
3	R/W	0	ROGUE_FAULT	Set to assert a TX_FAULT output if a ROGUE_ONU_FLAG occurs.
2	R/W	0	Reserved	
1:0	R/W	0	TX_SD_OUT	Set to determine what function is enabled at TX_SD output: 00/11 = Internal TX_SD signal, 01 = Rogue ONU TSSI signal, 10 = TX SHUTDOWN (SHUTDOWN_OUTPUT_EN function must be enabled too).

184	B8h		ROGUE_ONU_TIME	Rogue ONU monitoring timing
BIT	R/W	PoR		
7:4	R/W	0	TX_SD_ROGUE_TIME	Set the amount of time the TX_SD has to be asserted high continuously before a ROGUE_ONU flag is set. Default value of 0h inhibits this function. 1.6ms to 3.4sec selectable times. Values of 1100b and above will set a time of 3.4sec.
3:0	R/W	0	BEN_ROGUE_TIME	Set the amount of time the BEN inputs have to be asserted high continuously before a ROGUE_ONU flag is set. Default value of 0h inhibits this function. 1.6ms to 3.4sec selectable times. Values of 1100b and above will set a time of 3.4sec.

185	B9h		VABTSET	Active back termination control
BIT	R/W	PoR		
7:0	R/W	0	VABTSET	Set the active back termination voltage

186	BAh		RX_CTRL	Receiver controls
BIT	R/W	PoR		
7:6	R/W	0	RX_FILTER	Sets the receiver signal path bandwidth
5:4	R/W	0	RX_SLEW	Sets the receiver CML output slew rate
3:2	R/W	0	OUTPUT_SWING	Sets the receiver CML output swing
1	R/W	0	RSSI_POLARITY	Set to change the RSSI input from sink (default) to source.
0	R/W	0	RX_DATA_POLARITY	Set to invert the RXIN± data polarity

187	BBh		RX_LOS_CTRL	Receiver LOS controls
BIT	R/W	PoR		
7:6	R/W	0	LOS_SLOPE_COMP	Sets the LOS slope compensation factor.
5:3	R/W	0	LOS_HYS	Sets the LOS hysteresis. 000=0.5dB; 001=1.0dB; 010=1.5dB; 011=2.0dB; 100=2.5dB; 101=3.0dB
2	R/W	0	SQUELCH_ENABLE	Set to enable squelching of the Rx CML outputs when a LOS event occurs.
1	R/W	0	LOS_OUT_TYPE	Set to change the LOS output type from open drain (default) to LVTTL.
0	R/W	0	LOS_POLARITY	Set to invert the LOS output polarity to SD.

188	BCh		RX_LOS_LEVEL	Receiver LOS assert level setting
BIT	R/W	PoR		
7	R/W	0	LOS_SLEEP_CTRL	Sets the LOS output high (default) or low on RX_SLEEP
6:0	R/W	0	LOS_LEVEL	Sets the LOS assert level.

189	BDh		APD_DAC_CTRL	APD DAC controls
BIT	R/W	PoR		
7	R/W	0	Reserved	Reserved
6:3	R/W	0	APD_DAC_OFFSET	Sets the APD DAC offset
2:1	R/W	0	APD_MODE	Sets the APD control mode
0	R/W	0	APD_DAC_LUT_EN	Enable LUT control of the APD DAC.

190	BEh		APD_DAC	APD DAC setting
BIT	R/W	PoR		
7:0	R/W	0	APD_DAC	Sets the APD DAC value

191	BFh		SLEEP_CTRL	Sleep control
BIT	R/W	PoR		
7:4	R/W	0	Reserved	Reserved
3	R/W	0	RX_SLEEP_POL	Set to invert the polarity of the RX_SLEEP function
2	R/W	0	TX_DISABLE_POL	Set to invert the polarity of the TX_DISABLE function.
1	R/W	0	RX_SLEEP_CONTROL	Set to control RX_SLEEP from the TX_SLEEP function. Applies to both hard & soft controls.
0	R/W	0	TX_SLEEP_MODE	Set to use TX_DISABLE pin as TX_SLEEP control.

192	C0h		STATUS_0	Status information
BIT	R/W	PoR		
7:6	R/W	0	BEN_TIME_SEL	Selects time period that the power and bias values are held for when BEN is de-asserted. 00: 5.5ms to 8.2ms, 01: 21.8ms to 32.8ms, 10: 43.7ms to 65.5ms, 11: 87.4ms to 131.1ms
5	R/W	0	EE_ACC_ISSUE	GN25L95 sets this bit to indicate an error with the last EEPROM update. Latched until reset by user.
4	R/W	0	TX_BIAS_BEN_LATCH	Set to hold the last valid Tx Bias value during a BEN de-assert (timings specified by BEN_TIME_SEL)
3	R/W	0	TX_POWER_BIAS_ ZERO	Set to report zero Tx Power and Tx Bias on TX_DISABLE.
2	R/W	0	TX_POWER_BEN_ LATCH	Set to hold the last valid Tx Power value during a BEN de-assert (timings specified by BEN_TIME_SEL)
1	R	0	DDMI_READY	GN25L95 sets this bit when DDMI data is ready.
0	R	0	EEPROM_PRESENT	GN25L95 sets this bit after successful communication with an external EEPROM.

193	C1h		ADC_CTRL	**ADC control** (Perform a power cycle/soft reset to ensure correct operation after programming)
BIT	**R/W**	**PoR**		
7:5	R/W	0	ADC_ADDR	Select ADC source to continuously sample.
4	R/W	0	ADC_SEL	Enable continuous sampling of ADC.
3	R/W	0	VCC_ADC_SEL	Select which of the VCC monitors is used in the SFF-8472 calibrated values. 0=Tx, 1=Rx.
2	R/W	0	EXT_TEMP_SENSOR	Set this bit to enable an external precision temperature sensor present at the ADC_IN pin to control the DDMI temperature report and LUT indexing.
1	R/W	0	RXP_QUAD_SHIFT_SEL	0= Result of squared ADC value x slope C2 shifted by 29 bits, 1 = Results shifted by 30bits
0	R/W	0	Reserved	

194	C2h		I2C_PASSWORD	I2C Password byte
BIT	**R/W**	**PoR**		
7:0	R/W	0	I2C_PASSWORD	Set this byte to value C5h to enable the I^2C address held in I2C_ADDRESS byte. This new address will be activated after the next power cycle.

195	C3h		I2C_CONTROL	**Set the I2C addresses that the GN25L95 responds to and provides control functions**
BIT	**R/W**	**PoR**		
7:2	R/W	0	I2C_ADDRESS	Sets I^2C address pages for the two memory spaces called A0h and A2h by default. The user can set a new 6 bit address field for the GN25L95 to respond to. Both A0h and A2h locations are changed automatically. This is only read and implemented on power-up. The I^2C address does not change dynamically.
1	R/W	0	LOW_PAGE_DIS	Set this bit to disable the GN25L95 lower memory page usually defined at address A0h. This is only read and implemented on power-up. The I^2C address does not change dynamically.
0	R/W	0	I2C_TIMEOUT_EN	Set this bit to enable a time out function on the I^2C slave interface. If the slave interface clock or data is pulled low for longer than ~20ms then the GN25L95 I^2C interface will reset.

196	C4h		EE_ACCESS	Set memory page access types.
BIT	R/W	PoR		
7	R/W	0	A0h_RD	Set to make the A0h memory page read only.
6	R/W	0	A2h_ALM_WRN_RD	Set to make the Alarm & Warnings section of A2h lower page read only. Registers 00h to 37h
5	R/W	0	A2h_CAL_CON_RD	Set to make the Calibration Constants section of A2h lower page read only. Registers 38h to 5Fh.
4	R/W	0	A2h_RDDMI_RD	Set to make the Real time Diagnostics section of A2h lower page read only. Registers 60h to 6Dh.
3	R/W	0	A2h_80_BF_RD	Set to make registers 80h to BFh of the A2h upper user scratch pad area PW1 read/write only.
2	R/W	0	A2h_C0_F7_RD	Set to make registers C0h to F7h of the A2h upper user scratch pad area PW2 read/write only.
1	R/W	0	A2h_F8_FF_RD	Set to make registers F8h to FFh of the A2h upper user scratch pad area PW2 read/write only.
0	R/W	0	HOST_PON_WRITE	Set to make all PON controls in A2 lower PW1 write only.

197	C5h		NVM_COPY	Copy register content to GN25L95 internal NVM
BIT	R/W	PoR		
7:4	R/W	0	NVM_WRITE_PASS	The correct password must be entered here to enable a register to NVM write. 1010b
3	R	0	Reserved	Factory use
2:0	R/W	0	NVM_PAGE	Select the register page to copy into NVM. 000 = Copy all pages to NVM 010 = Copy A2h Table 2 to NVM (Includes A2h upper F7h – FFh) 011 = Copy A2h Table 4 to NVM 100 = Copy A2h Table 5 to NVM 101 = Copy A2h Table 6 to NVM 001, 110, 111 = Copy A2h Table 2 to NVM (Includes A2h upper F7h – FFh)

198	C6h		NVM_COPY_STATUS	Indicates status of NVM copy process
BIT	R/W	PoR		
7:6	R/W	0	Reserved	Reserved
5	R	0	NVM_COPY_ERROR	Indicates an error occurred during the NVM_PAGE writing process.
4	R	0	NVM_FULL	Indicates an NVM page cannot be written as the NVM write quota has already been exceeded.
3	R	0	NVM_FACTORY_ERR	Indicates an issue writing to the factory calibration page (Factory use only).
2:0	R	0	NVM_PAGE_ERROR	Indicates which NVM page has an issue.

199	C7h		EEPROM_CTRL	External EEPROM controls
BIT	R/W	PoR		
7:2	R/W	0	Reserved	Reserved
1	R/W	0	EE_TAB2_DIS	Inhibits EEPROM updates of A2h Table 2 Control Settings.
0	R/W	0	EE_UPDATE_DIS	Inhibits EEPROM updates of entire memory map

200	C8h		NVM_FLAGS	Holds information about NVM pages * Register is only valid when device operating in NVM mode
BIT	R/W	PoR		
7	R	0	TAB6_NVM_WR_x2	Set if Table 6 has been written in NVM two times.
6	R	0	TAB6_NVM_WR_x1	Set if Table 6 has been written in NVM one time.
5	R	0	TAB5_NVM_WR_x2	Set if Table 5 has been written in NVM two times.
4	R	0	TAB5_NVM_WR_x1	Set if Table 5 has been written in NVM one time.
3	R	0	TAB4_NVM_WR_x2	Set if Table 4 has been written in NVM two times.
2	R	0	TAB4_NVM_WR_x1	Set if Table 4 has been written in NVM one time.
1	R	0	TAB2_NVM_WR_x2	Set if Table 2 has been written in NVM two times.
0	R	0	TAB2_NVM_WR_x1	Set if Table 2 has been written in NVM one time.

201	C9h		PW1	PW1 Password Entry
BIT	R/W	PoR		
31:0	R/W	0	PW1_VALUE	User definable password to provide PW1 access. 32 bit word.

205	CDh		PW2	PW2 Password Entry
BIT	R/W	PoR		
31:0	R/W	0	PW2_VALUE	User definable password to provide PW2 access. 32 bit word.

209	D1h		Reserved	Reserved
BIT	R/W	PoR		
7:0	R	0	Reserved	Reserved

210	D2h		TEMP(Slope)	Temperature Slope Internal calibration constant
BIT	R/W	PoR		
15:0	R/W	0	TEMP(Slope)	Temp Slope calibration constant. This is a 16 bit register with the MSB at the lower address and the LSB at the upper address. Unsigned integer.

212	D4h		TEMP(Offset)	Temperature Offset Internal calibration constant
BIT	R/W	PoR		
15:0	R/W	0	TEMP(Offset)	Temp Offset calibration constant. This is a 16 bit register with the MSB at the lower address and the LSB at the upper address. Signed twos complement.

214	D6h		VCC(Slope)	VCC Slope Internal calibration constant
BIT	R/W	PoR		
15:0	R/W	0	VCC(Slope)	VCC Slope calibration constant. This is a 16 bit register with the MSB at the lower address and the LSB at the upper address. Unsigned integer.

216	D8h		VCC(Offset)	VCC Offset Internal calibration constant
BIT	R/W	PoR		
15:0	R/W	0	VCC(Offset)	VCC Offset calibration constant. This is a 16 bit register with the MSB at the lower address and the LSB at the upper address. Signed twos complement.

218	DAh		Tx_BIAS(Slope)	Tx Bias Slope Internal calibration constant
BIT	R/W	PoR		
15:0	R/W	0	Tx_BIAS(Slope)	Tx Bias Slope calibration constant. This is a 16 bit register with the MSB at the lower address and the LSB at the upper address. Unsigned integer.

220	DCh		Tx_BIAS(Offset)	Tx Bias Offset Internal calibration constant
BIT	R/W	PoR		
15:0	R/W	0	Tx_BIAS(Offset)	Tx Bias Offset calibration constant. This is a 16 bit register with the MSB at the lower address and the LSB at the upper address. Signed twos complement.

222	DEh		Tx_PWR(Slope)	Tx Power Slope Internal calibration constant
BIT	R/W	PoR		
15:0	R/W	0	Tx_PWR(Slope)	Tx Power Slope calibration constant. This is a 16 bit register with the MSB at the lower address and the LSB at the upper address. Unsigned integer.

224	E0h		Tx_PWR(Offset)	Tx Power Offset Internal calibration constant
BIT	R/W	PoR		
15:0	R/W	0	Tx_PWR(Offset)	Tx Power Offset calibration constant. This is a 16 bit register with the MSB at the lower address and the LSB at the upper address. Signed twos complement.

226	E2h		Rx_PWR(Slope C2)	Rx Power Slope Internal calibration constant
BIT	R/W	PoR		
15:0	R/W	0	Rx_PWR(Slope C2)	Rx Power Slope C2 calibration constant. This is a 16 bit register with MSB at the lower address and LSB at the upper address. Unsigned integer.

228	E4h		Rx_PWR(Slope C1)	Rx Power Slope Internal calibration constant
BIT	R/W	PoR		
15:0	R/W	0	Rx_PWR(Slope C1)	Rx Power Slope C2 calibration constant. This is a 16 bit register with MSB at the lower address and LSB at the upper address. Unsigned integer.

230	E6h		Rx_PWR(Offset C0)	Rx Power Offset Internal calibration constant
BIT	R/W	PoR		
15:0	R/W	0	Rx_PWR(Offset C0)	Rx Power Offset C0 calibration constant. This is a 16 bit register with MSB at the lower address and LSB at the upper address. Signed twos complement.

232	E8h		ADC_TEMP	Temperature analogue monitor
BIT	R/W	PoR		
15:0	R	0	ADC_TEMP	Temperature ADC. The ADC is a 16 bit register with the MSB at the lower address and the LSB at the upper address.

234	EAh		ADC_IN	External ADC input analogue monitor
BIT	R/W	PoR		
15:0	R	0	ADC_IN	External ADC input. The ADC is a 16 bit register with the MSB at the lower address and the LSB at the upper address.

236	ECh		ADC_TX_BIAS	Tx bias current analogue monitor
BIT	R/W	PoR		
15:0	R	0	ADC_TX_BIAS	Tx bias current ADC. The ADC is a 16 bit register with the MSB at the lower address and the LSB at the upper address.

238	EEh		ADC_TX_POWER	Transmitter power (MPD) analogue monitor
BIT	R/W	PoR		
15:0	R	0	ADC_TX_POWER	Transmitted power (MPD) ADC. The ADC is a 16 bit register with the MSB at the lower address and the LSB at the upper address.

240	F0h		ADC_RX_POWER	Receiver power (RSSI) analogue monitor
BIT	R/W	PoR		
15:0	R	0	ADC_RX_POWER	Receiver power (RSSI) ADC. The ADC is a 16 bit register with the MSB at the lower address and the LSB at the upper address.

242	F2h		ADC_TX_MOD	Tx modulation current analogue monitor
BIT	R/W	PoR		
15:0	R	0	ADC_TX_MOD	Tx modulation current ADC. The ADC is a 16 bit register with the MSB at the lower address and the LSB at the upper address.

244	F4h		ADC_VCC_TX	Transmitter VCC analogue monitor
BIT	R/W	PoR		
15:0	R	0	ADC_VCC_TX	Transmitter VCC ADC. The ADC is a 16 bit register with the MSB at the lower address and the LSB at the upper address.

246	F6h		ADC_VCC_RX	Receiver VCC analogue monitor
BIT	R/W	PoR		
15:0	R	0	ADC_VCC_RX	Receiver VCC ADC. The ADC is a 16 bit register with the MSB at the lower address and the LSB at the upper address.

248	F8h		Reserved	
BIT	R/W	PoR		
7:0	R/W	0	Reserved	Reserved

249	F9h		Reserved	
BIT	R/W	PoR		
7:0	R/W	0	Reserved	Reserved

250	FAh		Reserved	
BIT	R/W	PoR		
7:0	R/W	0	Reserved	Reserved

251	FBh		Reserved	
BIT	R/W	PoR		
7:0	R/W	0	Reserved	Reserved

252	FCh		Reserved	
BIT	R/W	PoR		
7:0	R/W	0	Reserved	Reserved

253	FDh		Reserved	
BIT	R/W	PoR		
7:0	R/W	0	Reserved	Reserved

254	FEh		Reserved	
BIT	R/W	PoR		
7:0	R/W	0	Reserved	Reserved

255	FFh		Reserved	
BIT	R/W	PoR		
7:0	R/W	0	Reserved	Reserved

A2h Table 4 – GN25L95 Modulation Look-Up Table

The GN25L95 Modulation Look-Up Table is contained within Table 4 at address A2h, registers 80h to FFh. This is accessed by writing 04h to the table select byte at address A2h, register 7F.

Note that Table 4 is Password Level 2 protected.

GN25L95 Modulation LUT				
BYTE	**BIT**	**PoR**	**NAME**	**DESCRIPTION**
80h to FFh	All	0	Modulation LUT bytes	Temperature indexed MOD_DAC values

The LUT consists of 64 word (16-bit) locations from 80h to FFh covering the temperature range -40°C to +120°C. The step size for each location is 2.5°C.

The temperature step size resolution can be halved from 2.5°C to 1.25°C by enabling a linear interpolation of the values between two consecutive look-up table values.

The on-chip NVM allows the user to re-write the content in A2h Table 4 up to 2x. If multiple re-writing of this memory area is required then the user should use an external 8k EEPROM connected to the GN25L95.

A2h Table 5 – GN25L95 Bias Look-Up Table

The GN25L95 Bias Look-Up Table is contained within Table 5 at address A2h, registers 80h to FFh. This is accessed by writing 05h to the table select byte at address A2h, register 7Fh.

Note that Table 5 is Password Level 2 protected.

GN25L95 Bias LUT				
BYTE	**BIT**	**PoR**	**NAME**	**DESCRIPTION**
80h to FFh	All	0	Bias LUT bytes	Temperature indexed BIAS_DAC values

The LUT consists of 64 word (16-bit) locations from 80h to FFh covering the temperature range -40°C to +120°C. The step size for each location is 2.5°C.

The temperature step size resolution can be halved from 2.5°C to 1.25°C by enabling a linear interpolation of the values between two consecutive look-up table values.

The on-chip NVM allows the user to re-write the content in A2h Table 5 up to 2x. If multiple re-writing of this memory area is required then the user should use an external 8k EEPROM connected to the GN25L95.

A2h Table 6 – GN25L95 APCSET DAC and APD DAC Look-Up Tables

The GN25L95 APCSET DAC and APD DAC Look-Up Tables are contained within Table 6 at address A2h registers 80h to FFh. This is accessed by writing 06h to the table select byte at address A2h, register 7Fh.

Note that Table 6 is Password Level 2 protected.

GN25L95 APCSET LUT				
BYTE	**BIT**	**PoR**	**NAME**	**DESCRIPTION**
80h to BFh	All	0	APC SET LUT bytes	Temperature indexed APCSET_DAC values

The APCSET_DAC LUT consists of 64 byte locations from 80h to BFh covering the temperature range -40°C to +120°C. The step size for each location is 2.5°C.

GN25L95 APD DAC LUT				
BYTE	**BIT**	**PoR**	**NAME**	**DESCRIPTION**
C0h to FFh	All	0	APD DAC LUT bytes	Temperature indexed APD_DAC values

The APD_DAC LUT consists of 64 byte locations from C0 to FFh covering the temperature range -40°C to +120°C. The step size for each location is 2.5°C.

The on-chip NVM allows the user to re-write the content in A2h Table 6 up to 2x. If multiple re-writing of this memory area is required then the user should use an external 8k EEPROM connected to the GN25L95.

Applications Information

Applications

The following applications circuit diagrams show how the GN25L95 can be used in several different fiber optic transceiver applications.

EPON FTTh ONU Transceiver Module

The application schematic below shows how the GN25L95 can be configured for use in a EPON transceiver module. The GN25L95 can be used without any additional external memory or microcontrollers as EPON applications generally do not require digital diagnostic monitoring functionality and the GN25L95 can be digitally programmed during module assembly via the I^2C interface and set-up values stored in the on-chip NVM.

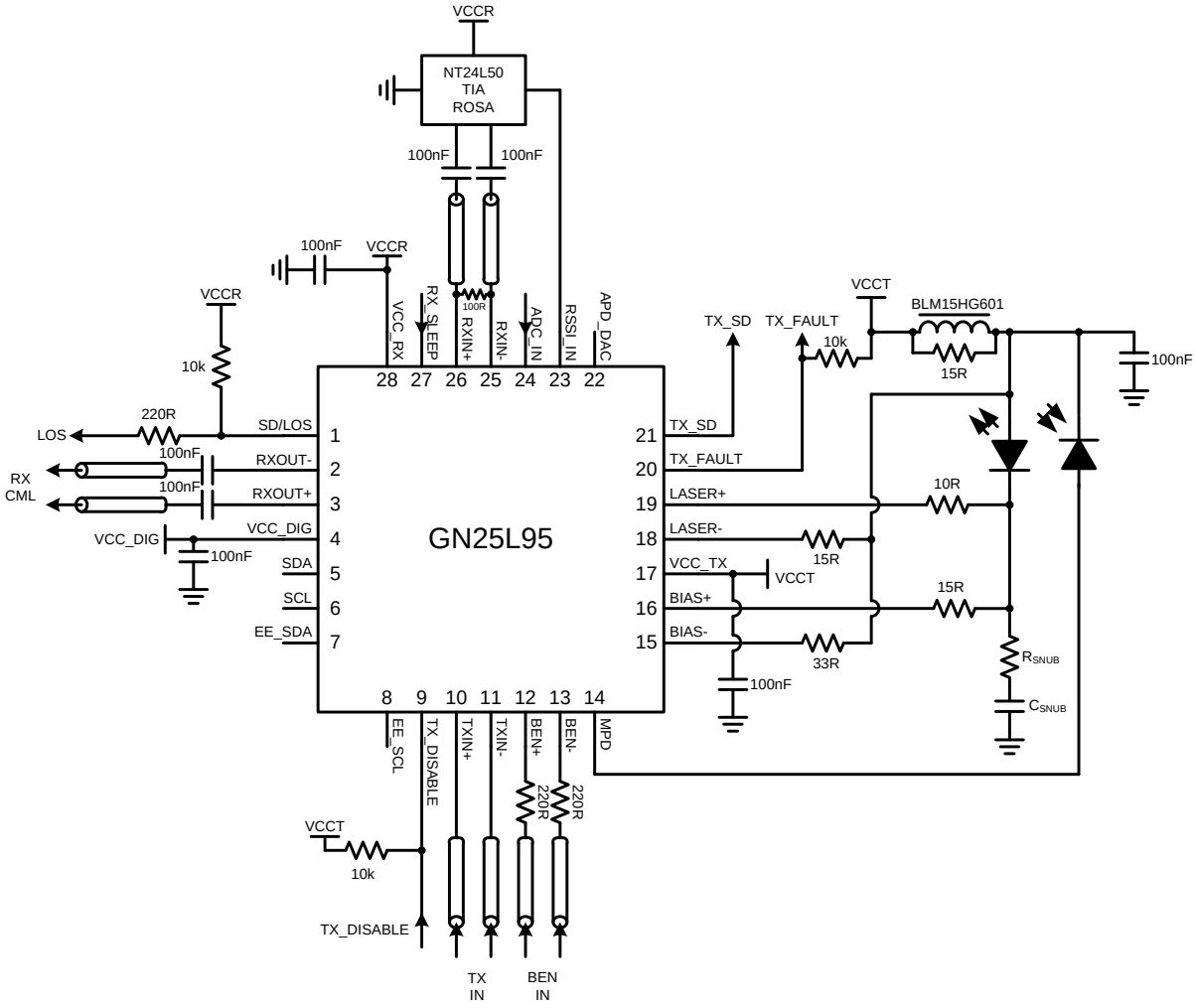


Figure 67 – Typical EPON Module Application Using GN25L95

GPON FTTh ONU Transceiver Module

The application schematic below shows how the GN25L95 can be configured for use in a GPON transceiver module. In this application for a GPON Di-Plexer module the GN25L95 is used in conjunction with an 8K EEPROM to provide a complete SFF-8472 compliant DDMI solution.

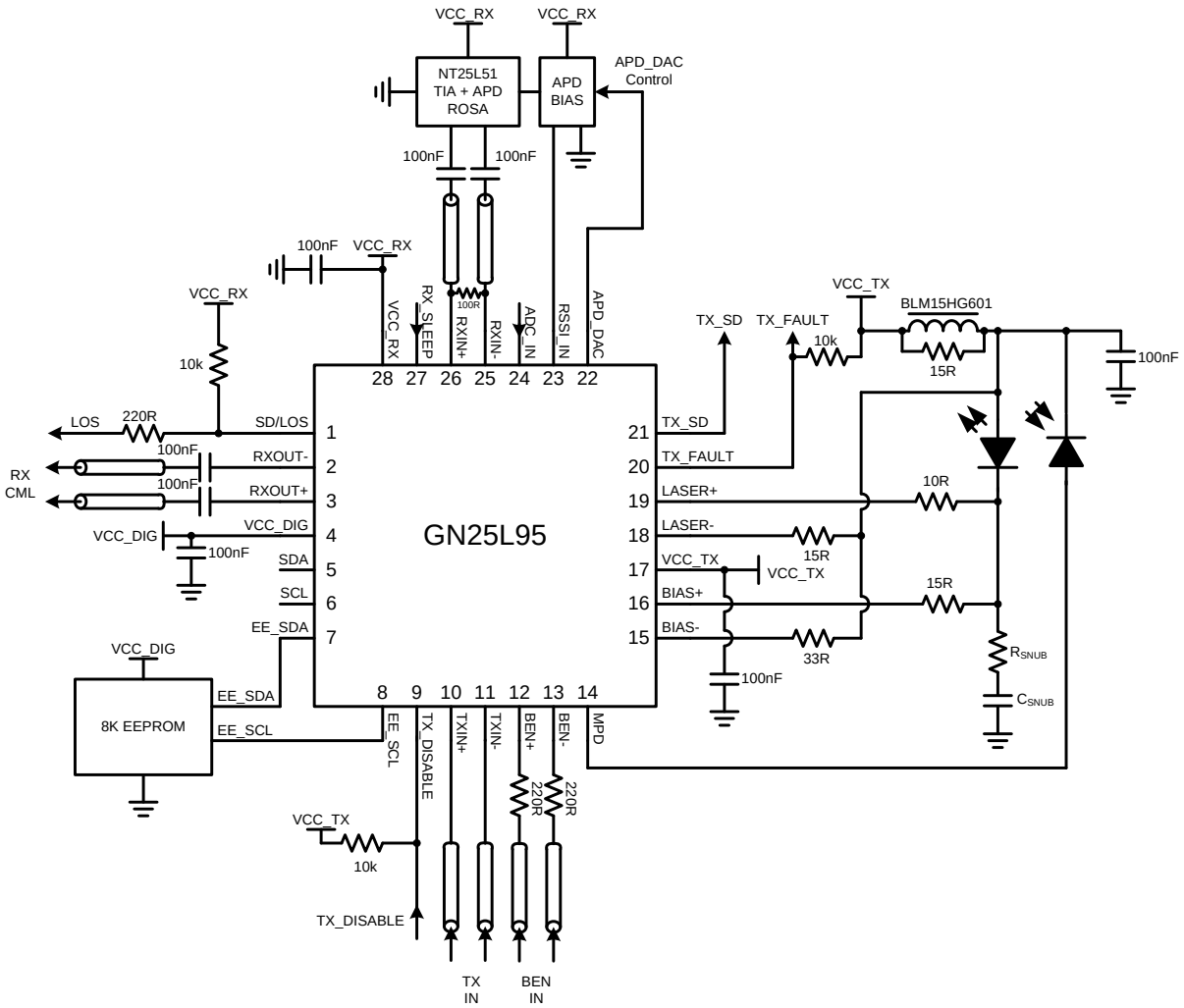


Figure 68 – Typical GPON Module Application Using GN25L95

GPON APD BOSA-on-Board Application

The application schematic below shows how the GN25L95 can be configured for use in a GPON ONU BOSA-on-Board application. The GN25L95 is controlled via the I_2C interface from the ONU GPON MAC SoC or microcontroller. The example below shows an APD based receiver, using Semtech's NT25L51 TIA + APD in a BOSA, where the APD control voltage is provided by an external switching boost regulator that is controlled via the GN25L95's on-chip APD_DAC output.

An alternative, non APD, solution could use Semtech's NT25L59 high sensitivity 2.5 Gbps TIA. In this case the APD_DAC output is not used.

The GN25L95 mean power control loop is used to set and maintain the transmitter output power whilst the extinction ratio control can be provided either by the GN25L95's on-chip temperature compensated modulation current control or by using modulation current Look-Up Tables stored on the GPON SoC set via the I^2C interface.

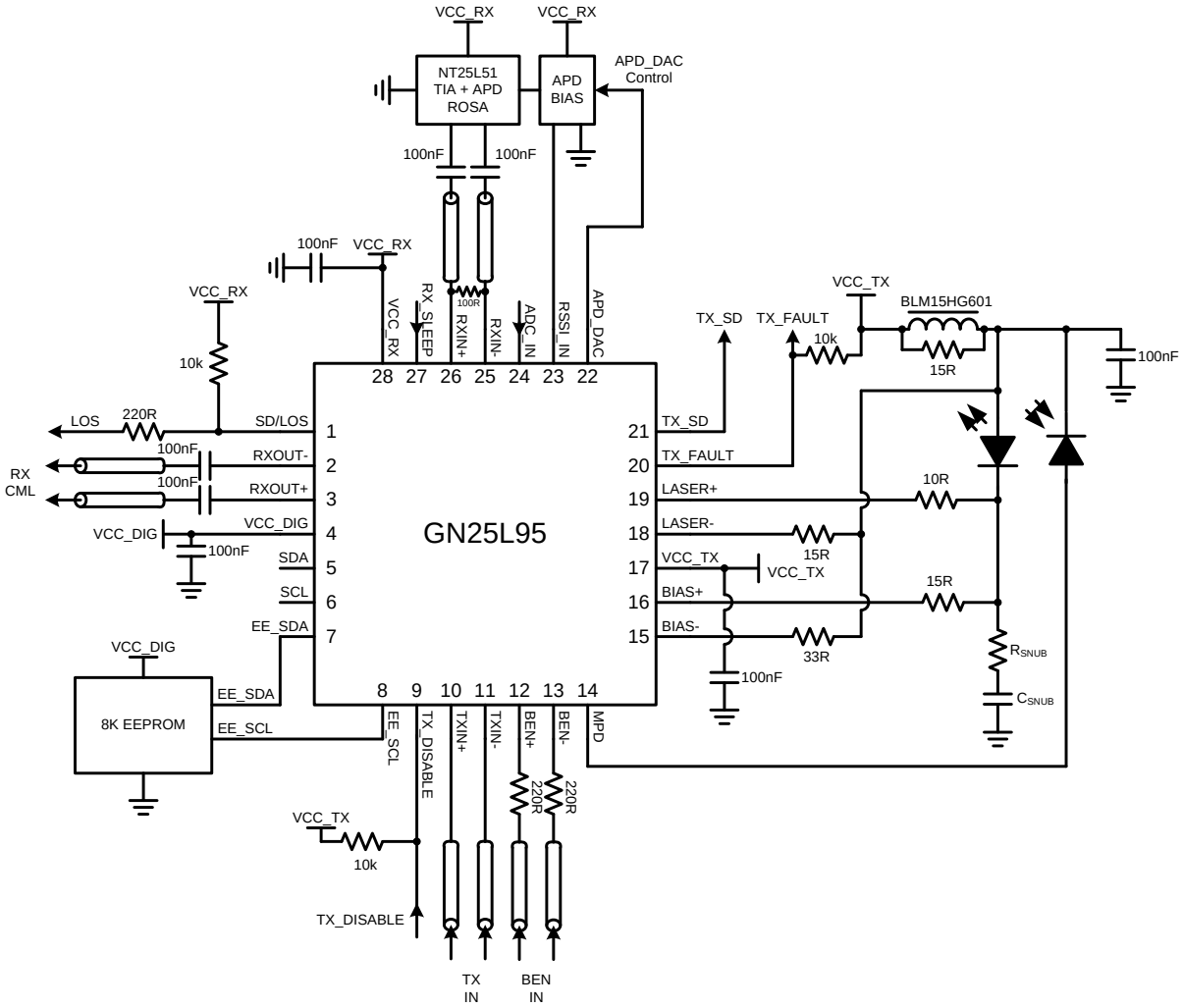


Figure 69 – Typical GPON ONU BOSA-on-Board Application Using GN25L95

SFP DDMI Transceiver Module

The application schematic below shows how the GN25L95 can be configured for use in an SFP DMMI transceiver module. The GN25L95 is used in conjunction with an external microcontroller that features some digital I/O only. The microcontroller provides the external I^2C data interface to the module host interface and processes digital diagnostic data obtained by reading the digital memory of the GN25L95.

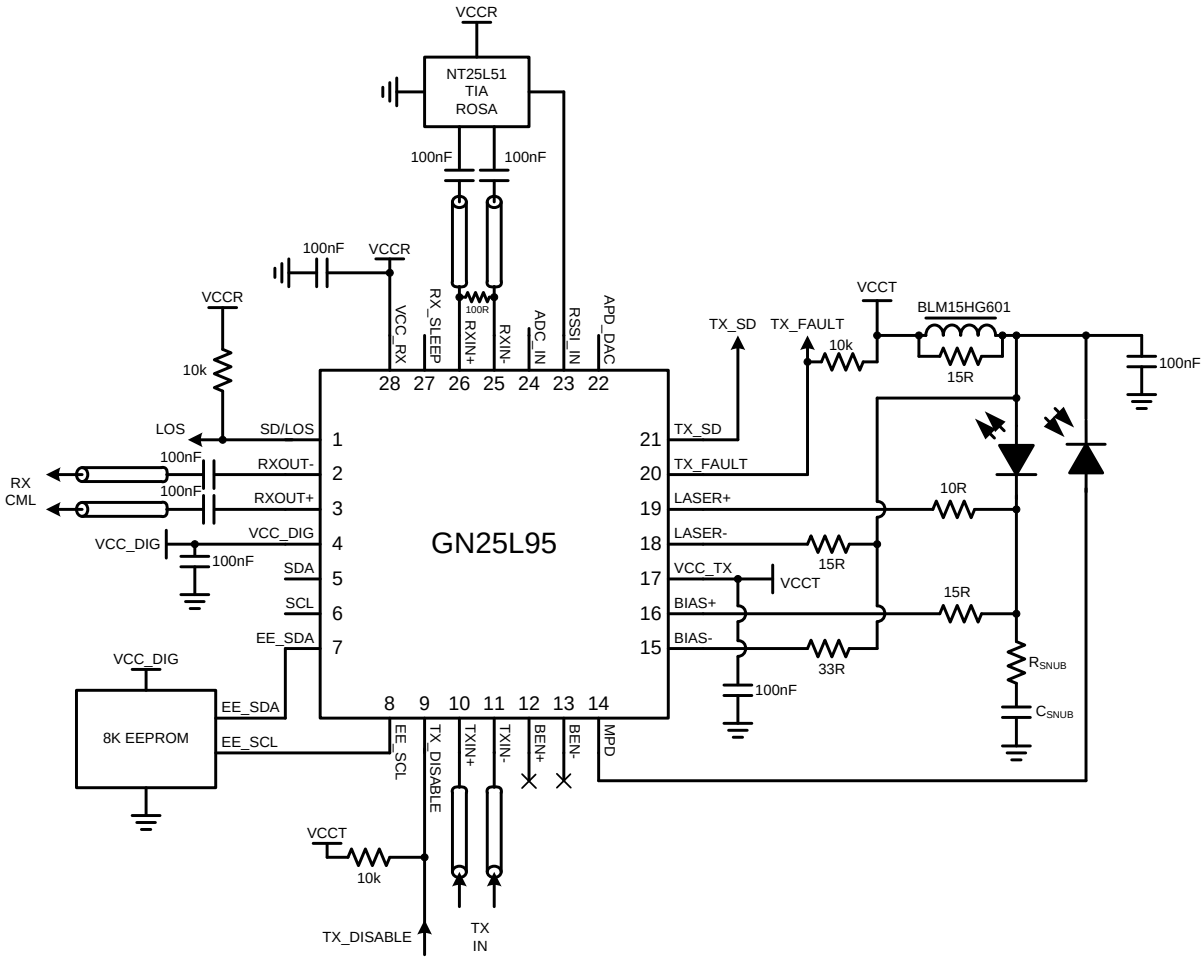
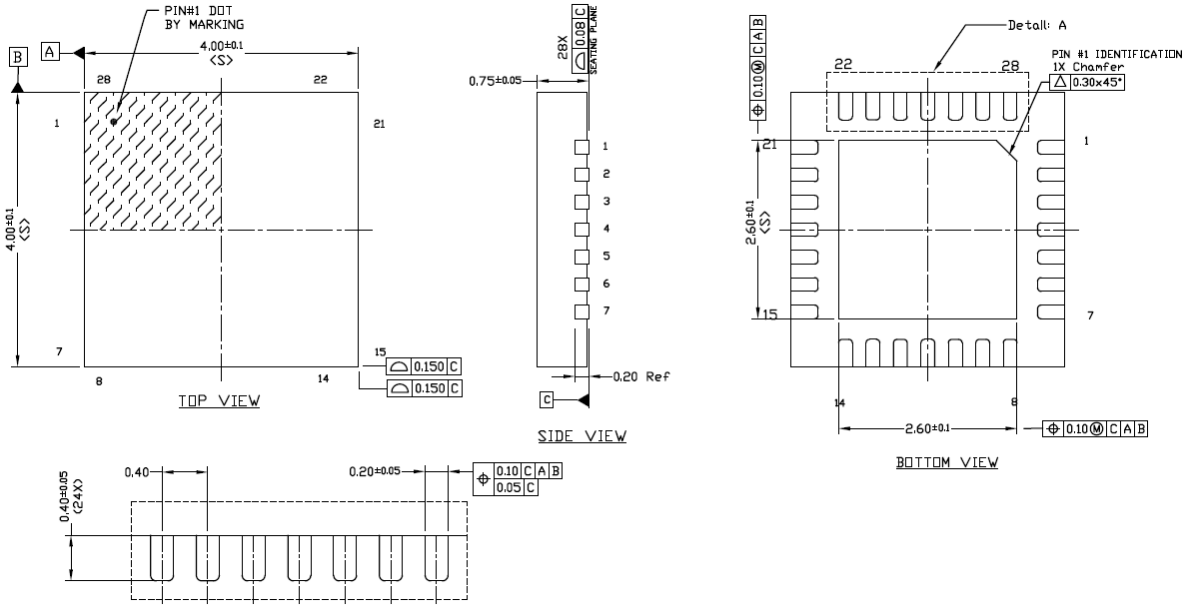


Figure 70 – Typical SFP DDMI Module Application Using GN25L95

Package Information

QFN 28-pin, 4 x 4 mm, 0.4 mm pitch



Dimensions in mm

Figure 71 – 4 mm x 4 mm QFN 28 Lead Mechanical Package Drawing

Ordering Information

Part Number	Package
GN25L95-QFN	4 mm x 4 mm QFN 28
GN25L95-QFN-TR	4 mm x 4 mm QFN 28 on Tape & Reel

Table 41 – Ordering Information

DOCUMENT IDENTIFICATION
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