

GO2925 1310nm Optical Transceiver

Features

- Best-in-class optical receiver sensitivity: -22dBm (over all supported video rates with pathological data)
- Robust error free transmission of signals from 50Mbps to 3Gbps with up to 30km single-mode fiber
- Maximum distance of 10km under worst-case conditions and 3Gbps video pathological signals
- Supports video pathological patterns for SD-SDI, HD-SDI and 3G-SDI
- Hot-pluggable
- Laser disable pin
- Diagnose and control via I²C interface including:
 - Monitoring of the laser bias current, average output power, receive optical power, supply voltage and temperature
 - Alarm reporting
 - Module ID polling
- Single +3.3V power supply
- Low Power Consumption—typical 650mW
- RoHS compliant
- Operating case temperature range: 0°C to 70°C
- 56.5mm x 13.4mm x 8.6mm SFP Package
- SMPTE 297-2006 compatible

Applications

- SMPTE 297-2006 compatible optical-to-electrical interfaces
- Broadcast cameras

Description

The GO2925 is an optical transceiver module engineered for exceptional performance in the presence of SDI pathological patterns. The transceiver features best-in-class optical receiver sensitivity for SMPTE 259M, SMPTE 344M, SMPTE 292M and SMPTE 424M serial rates, thus providing superior optical link budget and robustness.

The GO2925 contains a PIN photodiode receiver and a 1310nm Fabry-Perot laser transmitter designed to provide error-free transmission of signals from 50Mbps to 3Gbps over single mode fiber (9/125). It is also hot-pluggable.

The GO2925 provides extensive operational status monitoring through an I^2C interface. Input optical power is monitored in the receiver; output optical power and bias current are monitored in the transmitter. Other operating conditions, such as power supply and operating temperature, are also monitored. If a monitored parameter falls outside the pre-defined range, an alarm flag associated with the parameter will be raised.

Ordering Information

Part Number	Package	Temperature Range
GO2925-31CM	SFP	T _{CASE} = 0°C to 70°C



GO2925 3G-SDI 1310nm Video Optical Transceiver Module

Revision History

Version	ECR	Date	Changes and/or Modifications
Α	151975	July 2009	New document.
0	152528	September 2009	Converted to Preliminary Data Sheet, Updated Marking Information, Updated Package Information, Modified Extinction Ratio in Table 3-2: Transmitter Optical Performance Specifications, Modified Operating Case Temperature and Storage Temperature in Table 3-1: Absolute Maximum Ratings
1	153151	November 2009	Converted to Data Sheet. Updated second Note in Table 3-3: Receiver Optical Performance Specifications, updated Table 3-1: Absolute Maximum Ratings.



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1. Functional Block Diagram

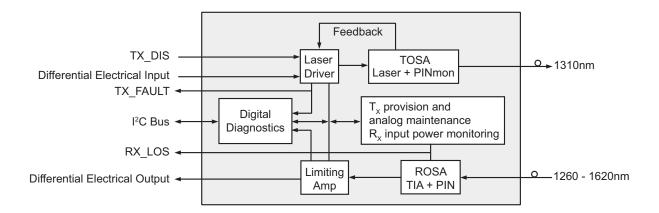


Figure 1-1: GO2925 Functional Block Diagram



2. Pin Specifications

2.1 Pin Configuration

Figure 2-1 shows the host board pad configurations for the GO2925. Figure 2-2 shows the edge connector pad configuration for the GO2925.

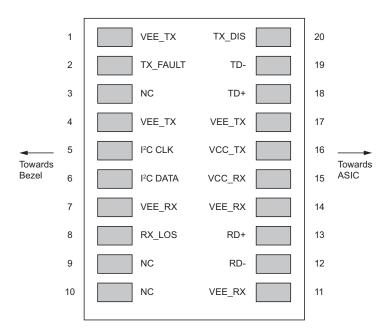


Figure 2-1: GO2925 Host Board Pad Configuration

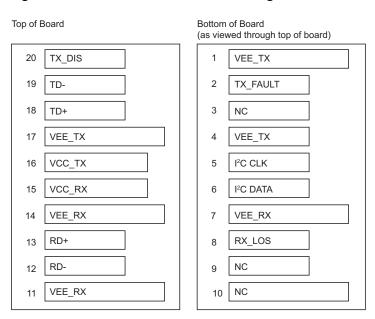


Figure 2-2: GO2925 Edge Connector Pad Configuration



2.2 Pin Descriptions

Table 2-1: Pin Descriptions

Number	Name	Туре	Description
1	VEE_TX	Ground	Transmitter Ground connection
2	TX_FAULT	Output	Transmitter fault indicator (Active high,
2	IX_IAOLI	σαιραί	open-drain)
3	NC	No Connect	No Connection
4	VEE_TX	Ground	Transmitter Ground connection
5	I ² C CLK	Digital (Input)	I ² C Clock
6	I ² C DATA	Digital (Bi-Directional)	I ² C Data
7	VEE_RX	Ground	Receiver Ground connection
8	RX_LOS	Output	Receiver loss of signal indicator (Active high, open-drain)
9	NC	No Connect	No Connection
10	NC	No Connect	No Connection
11	VEE_RX	Ground	Receiver Ground connection
12	RD-	Output	Negative differential output (AC-coupled internally)
13	RD+	Output	Positive differential output (AC-coupled internally)
14	VEE_RX	Ground	Receiver Ground connection
15	VCC_RX	Power	Receiver power supply
16	VCC_TX	Power	Transmitter power supply
17	VEE_TX	Ground	Transmitter Ground connection
18	TD+	Input	Positive differential input (AC-coupled internally)
19	TD-	Input	Negative differential input (AC-coupled internally)
20	TX_DIS	Digital (Input)	Transmitter Disable. Laser is disabled when high. Internal $6k\Omega$ pull-up.

NOTES:

- 1. All VEE_TX are connected together inside the module
- 2. All VEE_RX are connected together inside the module



2.3 Host Board Power Supply Requirements

The host board is required to provide a regulated and filtered power supply of 3.3V +/-5% for the GO2925 via the on board SFP connector. Figure 2-3 shows the recommended board supply filtering. When the host board is loaded with a resistive load in place of the SFP module and sourcing the maximum rated current, the peak-to-peak power supply noise measured on the SFP connector should comply to Table 2-2.

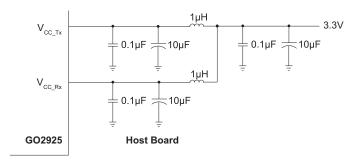


Figure 2-3: Recommended Host Board Supply Filtering

Table 2-2: Maximum Allowable Host Board Power Supply Noise at Vcc_Rx and Vcc_Tx

Frequency (KHz)	Peak-to-Peak Noise Amplitude (%)
0.02-1000	2
1000-10000	3

2.4 Optical Connector Requirements

An LC connector with PC/UPC polish is required for each port.



3. Product Specifications

3.1 Absolute Maximum Ratings

Table 3-1 lists the absolute maximum ratings for the GO2925. Conditions exceeding the limits listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3-1: Absolute Maximum Ratings

Parameter	Conditions	Value/Units
Supply Voltage	-	4V
Operating Case Temperature	-	-20°C ≤ T _{CASE} ≤ 80°C
Storage Temperature	-	-40°C ≤ T _{STG} ≤ 85°C
ESD tolerance on all pins	-	±1kV HBM
Relative Humidity (non-condensing)	-	5% - 95% RH

3.2 Optical Performance Specifications

Table 3-2 lists the optical performance specifications for the transmitter of the GO2925.

Table 3-3 lists the optical performance specifications for the receiver of the GO2925.

Table 3-2: Transmitter Optical Performance Specifications

 V_{CC} = 3.3V ±5%, T_{C} = 0°C to 70°C. Typical values are at V_{CC} = 3.3V, T_{A} = 25°C unless otherwise specified.

Parameter	Symbol	Condition	Min	Тур	Max	Units	Notes
Wavelength	λ	_	1280	1310	1340	nm	1
Spectral Line Width (RMS)	-	-	-	1.5	3	nm	_
Average Optical Output Power	P _{OUT}	-	-5	-2	0	dBm	-
Extinction Ratio	ER	_	7	_	_	dB	_



Table 3-2: Transmitter Optical Performance Specifications (Continued)

 V_{CC} = 3.3V ±5%, T_{C} = 0°C to 70°C. Typical values are at V_{CC} = 3.3V, T_{A} = 25°C unless otherwise specified.

Parameter	Symbol	Condition	Min	Тур	Max	Units	Notes
Optical Signal Intrinsic Jitter	-	2.97Gbps, 1.485Gbps, 270Mbps PRBS	-	30	60	ps	-
		2.97Gbps	_	45	70	ps	_
		SMPTE 424M					
		Pathological					
		1.485Gbps	-	60	100	ps	-
		SMPTE 292M					
		Pathological					
		270Mbps	-	110	180	ps	_
		SMPTE 259M					
		Pathological					
Optical Signal Rise Time	t _r	2.97Gbps	_	105	165	ps	_
(20% to 80%)		SMPTE 424M					
Optical Signal Fall Time	t _f	2.97Gbps	_	120	180	ps	-
(20% to 80%)		SMPTE 424M					
Laser Power Monitoring Accuracy	-	-	-2	-	+2	dB	-
NOTES							
1. Measured at 25°C.							

Table 3-3: Receiver Optical Performance Specifications

 V_{CC} = 3.3V ±5%, T_{C} = 0°C to 70°C. Typical values are at V_{CC} = 3.3V, T_{A} = 25°C unless otherwise specified.

Parameter	Symbol	Condition	Min	Тур	Max	Units	Notes
Wavelength	λ	-	1260	-	1620	nm	-
Sensitivity	_	ER=7dB	_	-25	-22	dBm	1
Overload	_	-	0	_	-	dBm	1
Loss of Signal Asserted	-	2.97Gbps PRBS ER=7dB	-31	-	-	dBm	-
Loss of Signal De-asserted	-	2.97Gbps PRBS ER=7dB	-	-	-23	dBm	-
Loss of Signal Optical Hysteresis	-	2.97Gbps PRBS ER=7dB	0.5	-	-	dB	-
Maximum Back Reflection	-	_	-	-	-27	dB	-



Table 3-3: Receiver Optical Performance Specifications (Continued)

 V_{CC} = 3.3V ±5%, T_{C} = 0°C to 70°C. Typical values are at V_{CC} = 3.3V, T_{A} = 25°C unless otherwise specified.

Parameter	Symbol	Condition	Min	Тур	Max	Units	Notes
Input Power Monitoring Accuracy	-	-	-2	-	2	dB	-

NOTES

3.3 DC Electrical Specifications

Table 3-4 lists the DC electrical specifications of the GO2925. Figure 3-1 shows the definition of the differential signal level.

Table 3-4: DC Electrical Specifications

 $V_{CC} = 3.3 \text{V} \pm 5\%$, $T_{C} = 0^{\circ}\text{C}$ to 70°C . Typical values are at $V_{CC} = 3.3 \text{V}$, $T_{A} = 25^{\circ}\text{C}$ unless otherwise specified.

Parameter	Symbol	Condition	Min	Тур	Max	Units	Notes
Operating Temperature Range	T _{CASE}	-	0	-	70	°C	1
Power Supply Voltage	V _{CC}	-	3.13	3.3	3.47	V	1
Total Power Consumption	-	-	_	650	940	mW	_
Differential Input Data Amplitude	V _{p-pDiff}	-	0.4	-	2.4	Vpp	2
Differential Output Data Amplitude	V _{p-pDiff}	_	0.550	0.660	0.850	Vpp	3
Digital Input Low	V _{IL}	-	0		0.8	V	-
Digital Input High	V _{IH}	-	2		V _{cc}	V	_

NOTES

- 1. Outside the specified range, performance is not guaranteed.
- 2. Signals are AC coupled internally within the module and terminated to a 50Ω (single-ended) termination.
- 3. Each leg must be terminated to a 50Ω (single-ended) termination. Signals are AC coupled internally within the module.

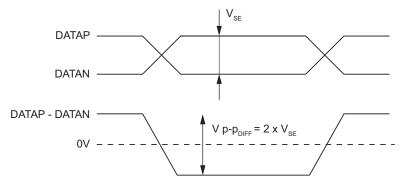


Figure 3-1: Definition of Differential Signal Level



^{1.} The sensitivity and the overload specifications refer to the input power levels for BER = 1E-12 against both PRBS and pathological pattern at SMPTE 259, SMPTE 292M and SMPTE 424M rates.

3.4 AC Electrical Specifications

Table 3-5 lists the AC electrical specifications for the GO2925.

Table 3-5: AC Electrical Specifications

 V_{CC} = 3.3V ±5%, T_{C} = 0°C to 70°C. Typical values are at V_{CC} = 3.3V, T_{A} = 25°C unless otherwise specified.

Parameter	Symbol	Condition	Min	Max	Units
Bit Rate	BR	-	50	3000	Mbps
Time to Initialize	t_init	From power on	_	300	ms
Rise/Fall Time	t _r / t _f	20% to 80%	-	135	ps
Tx_Disable Assert Time	t_off	Time from rising edge of Tx_Disable to when the optical output falls below 10% of nominal.	-	10	μs
Tx_Disable Negate Time	t_on	Time from falling edge of Tx_Disable to when the modulated optical output rises above 90% of nominal.	-	1	ms
Rx_LOS Assert Time	t_loss_on	Time from Rx_LOS state to Rx_LOS assert.	-	10	ms
Rx_LOS De-assert Time	t_loss_off	Time from non-Rx_LOS state to Rx_LOS de-assert.	_	10	ms
Serial ID Clock Rate	f_serial_clock	-	-	400	kHz

3.5 Supporting Circuit Specifications

3.5.1 In-Rush Current Control Circuit

Due to the hot-pluggable requirement, the GO2925 has built-in circuits to limit the in-rush current upon hot insertion. The specifications of the in-rush limiting circuits are summarized in Table 3-6.

Table 3-6: In-rush Current Limiting Circuits Specifications

Parameter	Value
Maximum in-rush current ramp rate	50mA/ms
Maximum in-rush current	30mA over steady state



4. Digital Diagnostics

4.1 I²C Bus Interface

The I^2C interface allows reading of diagnostic information from the module. It is comprised of I^2C DATA and I^2C CLK pins. All address and data bytes are transmitted through the I^2C DATA pin. The I^2C DATA and I^2C CLK pins are open-collector and they must be pulled high (4.75k Ω recommended) externally to the module. Data on the I^2C DATA pin may only change during I^2C CLK 'low' time periods. Data changes during I^2C CLK 'high' periods will indicate either a START or STOP condition. Operations and conditions are described as follows:

START Condition

The START condition is originated by the host. A high-to-low transition of I^2C DATA while I^2C CLK 'high' defines a START condition that must precede any other command, see Figure 4-1.

STOP Condition

The STOP condition is originated by the host. A low-to-high transition of I^2C DATA while I^2C CLK 'high' defines a STOP condition, see Figure 4-1.

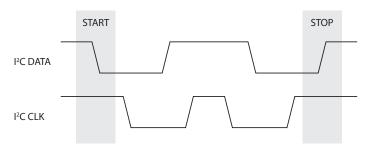


Figure 4-1: I²C START and STOP Condition

Acknowledge or ACK Condition

The acknowledge condition occurs when the I^2C DATA pin is pulled 'low' during the ninth clock pulse following an address or data byte. The module originates this condition after it has received a block or data address. The host originates this condition during a sequential address read operation.

Addressing Operation

The module must receive a block address following a START condition to enable a read operation. The block address is clocked into the module MSB to LSB. There are three read operations: current address read, random read, and sequential address read.

Note that by the convention specified in the SFP MSA, 7-bit block addresses are left shifted by one bit when expressing them in hex. Block addresses for the different



memory regions are specified in Section 4.2. Block addresses A0h, A2h, and B2h would therefore be transmitted defined as binary 1010000, 1011001 and 1011001 respectively.

Current Address Read Operation

The module has an internal register that maintains the data address used during the last read operation, incremented by one. If the most recent data address was FFh, then the register resets to 00h. Once the block address is clocked in by the host with the R/W bit set 'high', the module follows with an ACK condition, and the data byte located at the current data address is serially clocked out of the module MSB to LSB. The operation is terminated when the host does not provide an ACK condition and initiates a STOP condition. See Figure 4-2.

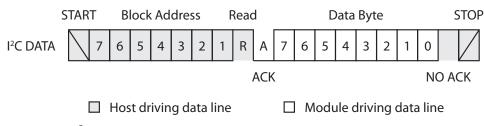


Figure 4-2: I²C Current Address Read Operation

Random Address Read Operation

A random read operation requires a dummy write sequence to load in the data address. Once the block and data addresses are clocked in by the host followed by an ACK condition provided by the module, the host must generate another START condition. The host now initiates a current address read operation by sending the block address with the R/W bit set 'high'. The module provides an ACK condition and serially clocks out the data byte. The operation is terminated when the host does not provide an ACK condition and initiates a STOP condition. See Figure 4-3.

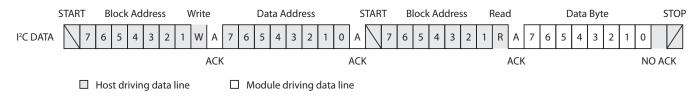


Figure 4-3: I²C Random Access Read Operation

Sequential Address Read Operation

The sequential address read operation is initiated by either a current address read or random address read operation. After the host receives the first data byte, it responds with an ACK condition. As long as the module receives the ACK condition after a data byte is read, the host can clock out additional data bytes from the module. After the data address reaches FFh, it resets to 00h. The operation is terminated when the host does not provide an ACK condition and initiates a STOP condition. See Figure 4-4.



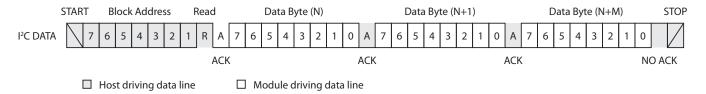


Figure 4-4: I²C Sequential Read Access Operation

4.2 Serial Interface Memory Map

Module identification and digital diagnostic monitoring information is accessible through the memory map addresses shown in this section. The items below outline the different block addresses of the module:

- Block address A0h contains serial ID information of the module.
- Block address A2h contains alarm and warning flags, thresholds and real-time digital diagnostic features set.

The 16-bit digital diagnostic monitoring information is internally calibrated over Gennum's specified operating temperature and voltage. Alarm and warning threshold values are calibrated in the same manner and can be interpreted as defined below.

Internally measured module temperature is represented as a 16-bit signed two's complement value in increments of 1/256 degrees Celsius, yielding a total range of -128°C to +128°C. To calculate the temperature, treat the two's complement value as a 16-bit unsigned integer and divide it by 256. If the result is greater or equal to 128, subtract 256 from the result. See Table 4-1 for temperature conversion examples.

Table 4-1: Temperature Conversion Examples

MSB (BIN)	LSB (BIN)	Temperature (°C)
01000000	00000000	64°C
01000000	00001111	64.059°C
01011111	00000000	95°C
11110110	00000000	-10°C
11011000	00000000	-40°C

Internally measured module supply voltage is represented as a 16-bit unsigned integer with the voltage defined as the full 16-bit value with the LSB equal to $100\mu V$, yielding a total range of 0 to +6.55V. To calculate the supply voltage, multiply the 16-bit unsigned integer by $100\mu V$.

Internally measured laser bias current is represented as a 16-bit unsigned integer with the current defined as the full 16-bit value with the LSB equal to $2\mu A$, yielding a total range of 0 to 131 mA. To calculate the laser bias current, multiply the 16-bit unsigned integer by $2\mu A$.



Internally measured TX and RX optical power are represented as a 16-bit unsigned integer with the power defined as the full 16-bit value with the LSB equal to 0.1 μW , yielding a total range of 0 to 6.5535 mW (~ -40 to +8.2 dBm). To calculate the TX and RX optical power, multiply the 16-bit unsigned integer by 0.1 μW .

Table 4-2: Modules Identification Fields

Block Address: A0h

Address	Size	Name	Description and Value of the Field
0	1	Identifier	Type of serial transceiver. 85h
1	1	Ext. Identifier	Extended identifier of type of serial transceiver. 04h
2	1	Connector	Code for connector type. 07h for LC connectors.
3	1	Standards Compliance	41h, for SMPTE259M/344M/292M/424M and SMPTE 297.
4-10	8	Transceiver Code	Code for electronic compatibility or optical compatibility. Not applicable for GO2925.
11	1	Encoding	Code for serial encoding algorithm. Value: 03H for NRZ.
12	1	BR, Nominal	Nominal bit rate, units of 100Mbps, 1Eh for 3Gbps.
13	1	Reserved	Xxh
14	1	Length(9μm) - km	Link length supported for standard SMF, units of km, 1Eh for 30km (at HD-SDI).
15	1	Length(9μm)	Link length supported for standard SMF, units of 100m, 00h
16	1	Length (50μm)	Link length supported for 50/125 μm fiber, units of 10m, 00h
17	1	Length (62.5μm)	Link length supported for 62.5/125 μm fiber, units of 10 m. 00h
18	1	Length (Copper)	Link length supported for copper, units of meters. 00h
19	1	Reserved	Xxh
20-35	16	Vendor name	SFP with OM transceiver vendor name (ASCII). G E N N U M
20	1	G	47h
21	1	E	45h
22	1	N	4Eh
23	1	N	4Eh
24	1	U	55h
25	1	М	4Dh



Table 4-2: Modules Identification Fields (Continued)

Block Address: A0h

Address	Size	Name	Description and Value of the Field
26-35	10	-	20h for each byte
36	1	Reserved	-
37-39	3	Vendor OUI	SFP with OM transceiver vendor IEEE company ID. 00 00 00h
40-55	16	Vendor PN	Part number provided by SFP with OM transceiver vendor. G O 2 9 2 5-3 1 C M
40	1	G	47h
41	1	0	4Fh
42	1	2	32h
43	1	9	39h
44	1	2	32h
45	1	5	35h
46	1	-	2Dh
47	1	3	33h
48	1	1	31h
49	1	С	43h
50	1	М	4Dh
51-55	6		20h
56-58	3	Reserved	Reserved field.
59	1	Vendor Rev	Revision level for part number provided by vendor.
60	1	Wavelength	05h for the higher two digits of 1310.
61	1	Wavelength	1Eh for the lower two digits of 1310.
62	1	Reserved	Xxh
63	1	CC_BASE	Check code for Base ID Fields (The value of the lower 8 bits of the sum of the contents from address 0 to 62).
64-65	2	Options	Indicates which optional SFP with OM signals are implemented.
64	1	-	Xxh
65	1	-	xx01101xh (1Ah)
66	1	BR, max	Upper bit rate margin, units of %, 5h.
67	1	BR, min	Lower bit rate margin, units of %, 5Fh.
68-83	16	Vendor SN	Serial number provided by vendor (ASCII)



Table 4-2: Modules Identification Fields (Continued)

Block Address: A0h

Address	Size	Name	Description and Value of the Field
84-85	2	Year	Manufacturing date code (ASCII).
86-87	2	Month	Manufacturing date code (ASCII).
88-89	2	Day	Manufacturing date code (ASCII).
90-91	2	Blank	-
92	1	Calibration flag	28h for calibrated average output power
93	1	-	F0h, Enhanced alarm/warning flags.
94	1	Reserved	Xxh
95	1	CC_EXT	Check code for the Extended ID Fields (The value of the lower 8 bits of the sum of the contents from address 64 to 94)
96-127	32	Reserved	-

Table 4-3: Alarm and Warning Thresholds

Block Address: A2h

Address	Size	Name	Description and Value of the Field
0-1	2	Temp High Alarm	MSB at lower address. 78°C case temp.
2-3	2	Temp Low Alarm	MSB at lower address8°C case temp.
4-5	2	Temp High Warning	MSB at lower address. 73°C case temp.
6-7	2	Temp Low Warning	MSB at lower address3°C case temp.
8-9	2	Supply Voltage High Alarm	MSB at lower address. 3.6V
10-11	2	Supply Voltage Low Alarm	MSB at lower address. 3.0V
12-13	2	Supply Voltage High Warning	MSB at lower address. 3.47V
14-15	2	Supply Voltage Low Warning	MSB at lower address. 3.14V
16-17	2	Laser Bias High Alarm	MSB at lower address. 100mA.
18-19	2	Laser Bias Low Alarm	MSB at lower address. 5mA
20-21	2	Laser Bias High Warning	MSB at lower address. 90mA.



Table 4-3: Alarm and Warning Thresholds (Continued)

Block Address: A2h

Address	Size	Name	Description and Value of the Field
22-23	2	Laser Bias Low Warning	MSB at lower address. 10mA
24-25	2	Tx Power High Alarm	MSB at lower address. 0dBm
26-27	2	Tx Power Low Alarm	MSB at lower address7dBm
28-29	2	Tx Power High Warning	MSB at lower address1dBm
30-31	2	Tx Power Low Warning	MSB at lower address6dBm
32-33	2	Rx Power High Alarm	MSB at lower address. 0dBm
34-35	2	Rx Power Low Alarm	MSB at lower address24dBm
36-37	2	Rx Power High Warning	MSB at lower address1dBm
38-39	2	Rx Power Low Warning	MSB at lower address23dBm
40-95	56	Reserved.	-

Table 4-4: Alarms and Real time Diagnostic information

Block Address: A2h

Address	Size	Name	Description and Value of the Field
96	1	Temperature MSB	Internally measured module temperature (approximately equal to case temperature)
97	1	Temperature LSB	Internally measured module temperature (approximately equal to case temperature)
98	1	V _{CC} MSB	Internally measured module supply voltage
99	1	V _{CC} LSB	Internally measured module supply voltage
100	1	Laser Bias MSB	Internally measured laser bias current
101	1	Laser Bias LSB	Internally measured laser bias current
102	1	T _X Power MSB	Internally measured T _X power
103	1	T _X Power LSB	Internally measured T _X power
104	1	R _X Power MSB	Internally measured R _X power
105	1	R _X Power LSB	Internally measured R _X power



Table 4-4: Alarms and Real time Diagnostic information

Block Address: A2h (Continued)

Address	Size	Name	Description and Value of the Field
106-109	9	Reserved	-
110 1	Reserved	Bit 7-3	
		T _X Fault	Bit 2: Indicates T _X Fault state
		Rx_LOS	Bit 1: Indicates Rx_LOS state
		Data_Ready	Bit 0
111	1	Temp Update	Bit 7 goes to high after a temperature update
		V _{CC} Update	Bit 6 goes to high after a V _{CC} update
		T _X bias Update	Bit 5 goes to high after a T _X bias current update
		T _X power Update	Bit 4 goes to high after a T _X power update
		R _X power Update	Bit 3 goes to high after a R _X input power update
		Reserved	Bit 0 to Bit 2
112	112 1	Temp High Alarm Flag	Bit 7, set when the internal temperature exceeds the high temp alarm threshold
		Temp Low Alarm Flag	Bit 6, set when the internal temperature goes below the low temp alarm threshold
		Supply Voltage High Alarm Flag	Bit 5, set when the internal V_{CC} exceeds the supply voltage high alarm threshold
		Supply Voltage Low Alarm Flag	Bit 4, set when the internal V _{CC} goes below the supply voltage low alarm threshold
	Laser Bias High Alarm Flag	Bit 3, set when the monitored laser bias current exceeds the laser bias high alarm threshold	
	Laser Bias Low Alarm Flag	Bit 2, set when monitored laser bias current goes below the laser bias low alarm threshold	
		T _X Power High Alarm Flag	Bit 1, set when the monitored T _X power exceeds the T _X power high alarm threshold
		T _X Power Low Alarm Flag	Bit 0, set when monitored T_X power current goes below the T_X power low alarm threshold



Table 4-4: Alarms and Real time Diagnostic information

Block Address: A2h (Continued)

Address	Size	Name	Description and Value of the Field
113	1	R _X Power High Alarm Flag	Bit 7, set when the monitored $R_{\rm X}$ power exceeds the $R_{\rm X}$ power high alarm threshold
		R _X Power Low Alarm Flag	Bit 6, set when the monitored R_X power goes below the R_X power low alarm threshold
		Reserved	Bit 0 - 5
114-115	2	Reserved	-
116	1	Temp High Warning Flag	Bit 7, set when the internal temperature exceeds the high temp warning threshold
		Temp Low Warning Flag	Bit 6, set when the internal temperature goes below the low temp warning threshold
		Supply Voltage High Warning Flag	Bit 5, set when the internal V _{CC} exceeds the supply voltage high warning threshold
		Supply Voltage Low Warning Flag	Bit 4, set when the internal V _{CC} goes below the supply voltage low warning threshold
		Laser Bias High Warning Flag	Bit 3, set when the monitored laser bias current exceeds the laser bias high warning threshold
		Laser Bias Low Warning Flag	Bit 2, set when monitored laser bias current goes below the laser bias low warning threshold
		T _X Power High Warning Flag	Bit 1, set when the monitored T_X power exceeds the T_X power high warning threshold
		T _X Power Low Warning Flag	Bit 0, set when monitored T_X power current goes below the T_X power low warning threshold
117	1	R _X Power High Warning Flag	Bit 7, set when the monitored R_X power exceeds the R_X power high warning threshold
		R _X Power Low Warning Flag	Bit 6, set when the monitored R_X power goes below the R_X power low warning threshold
		Reserved	Bit 0 - 5
118-127	2	Reserved	_



5. Application Reference Design

5.1 Typical Application Circuit

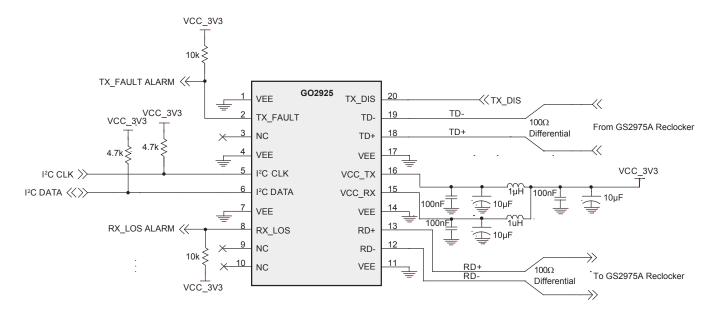


Figure 5-1: Typical Application Circuit



6. References and Relevant Standards

Table 6-1: References and Relevant Standards

INF-8074i Rev 1.0	SFP (Small Formfactor Pluggable) Transceiver
SMPTE 259M-2008	SDTV Digital Signal/Data – Serial Digital Interface
SMPTE 292M-2008	1.5 Gb/s Signal / Data Serial Interface
SMPTE 297-2006	Serial Digital Fiber Transmission System for SMPTE 259M, SMPTE 344M, SMPTE 292 and SMPTE 424M Signals
SMPTE 344M-2000	540 Mb/s Serial Digital Interface
SMPTE 424M-2006	3 Gb/s Signal/Data Serial Interface



7. Package Information

7.1 Package Dimensions

A common mechanical outline, as shown in Figure 7-1, is used for all SFP modules.

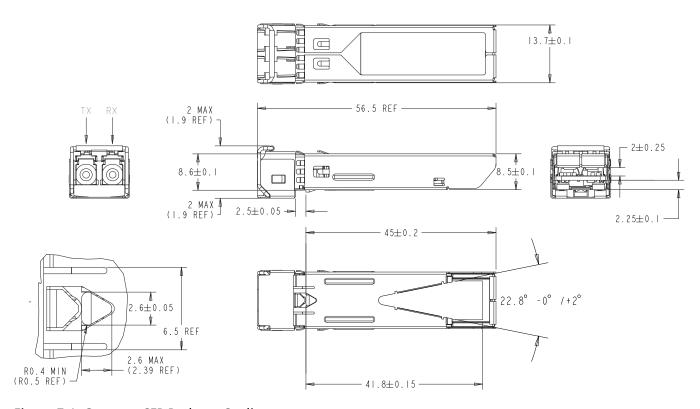


Figure 7-1: Common SFP Package Outline

7.2 Marking Information

Figure 7-2 illustrates the markings on the GO2925. Table 7-1 provides a description of the parameters in the marking diagram.

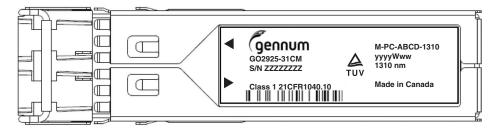


Figure 7-2: GO2925 Marking Diagram

Table 7-1: Marking Parameter Description

Parameter	Description
ZZZZZZZZ	8-digit serial number.
yyyyWww	Date code. Example: 2008W36



7.3 PCB Layout Recommendations

Notes:

- 1. All dimensions in mm.
- 2. Datum and basic dimensions established by customer
- 3. Pads and vias are chassis-ground in 11 places
- 4. Through-holes and plating are optional

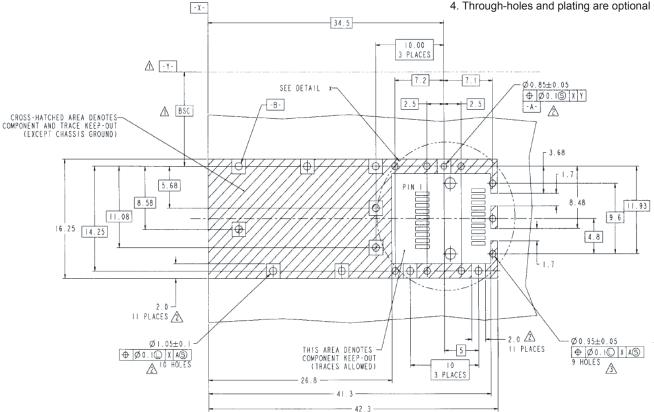


Figure 7-3: Host PCB Layout - Part 1



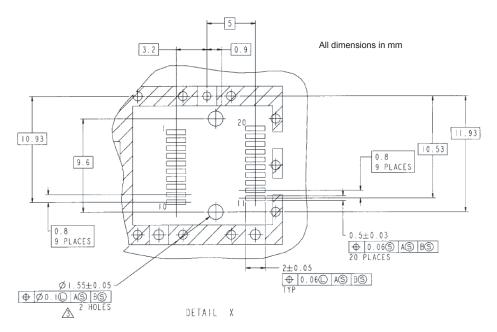


Figure 7-4: Host PCB Layout – Part 2



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