# General Purpose Controller / Memory Chip for Hearing Instruments

GP521 - DATA SHEET

## FEATURES

- **general purpose**
- **EEPROM non-volatile memory**
- **8 programmable current sink (PCS) control outputs**
- **can be configured with 6 PCS outputs for hearing instruments (two switchable, four non-switchable)**
- **status register**
- **data transmission error detection**
- **synchronization of GP521 internal clocks with program unit clock**

## STANDARD PACKAGING

- Chip (129 x 112 mils)
  Au Bump

## DESCRIPTION

The GP521 is a general purpose controller/memory chip intended for use with audio signal path circuits in programmable hearing instruments.

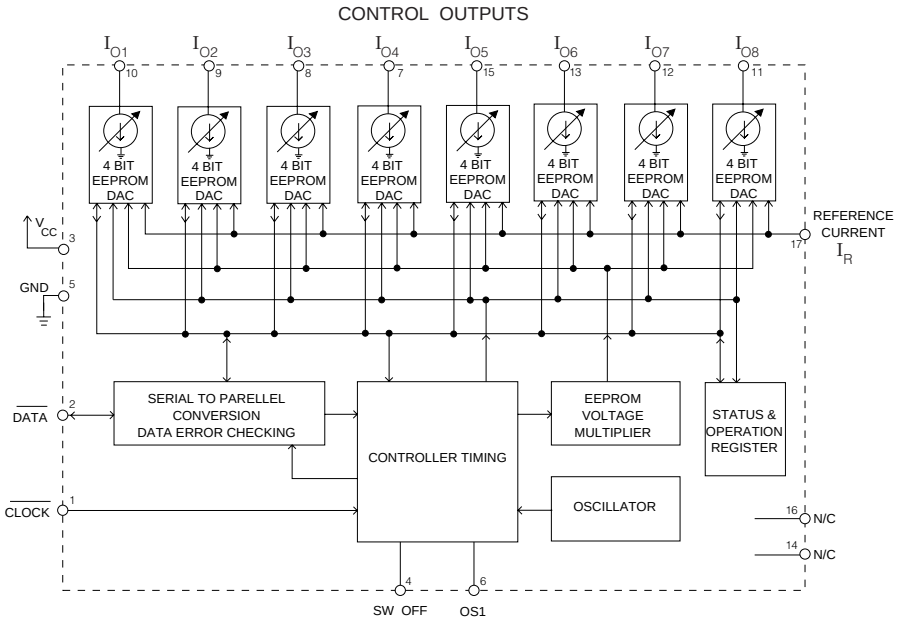
The GP521 uses a flexible communication standard which allows room for future growth in programmable functions for hearing instruments. The communication with the program unit is over a bi-directional serial data link. Error detection circuitry is used to avoid undesired changes in programmed settings.

An information transfer dialogue consists of the address and data for a register sent to the GP521 and the register contents returned by the GP521. The function controlled by an output of the GP521 is defined by the signal path circuit allowing current controlled parameters. The relationship between the GP521 register addresses and the function on the signal path circuit is defined by a data file in the programming unit. With this format, any software developed for the GP521 can be used for future generations of Gennum's controller/memory circuits and audio signal path circuits.

The GP521 uses EEPROM cells as the long term memory element. These cells will retain the stored data when the power supply is disconnected. Each EEPROM cell is combined with a temporary (RAM) memory cell which makes it possible to evaluate various control settings prior to saving them in the long term EEPROM memory.

The GP521 controls the audio signal path circuit using eight Programmable Current Sinks (PCS). Each PCS has 16 programmable settings. The circuit can be configured for either 6 or 8 PCS outputs. When used with a single pole single throw switch (SPST) under the 6 PCS configuration , it is possible to design a hearing instrument with two programmed settings (i.e. adjusting a low cut filter for either noisy or quiet background environments). The 8 output configuration may be used for circuits that require more programmable but non-switchable settings. An external reference current is used for the PCS's so that the PCS outputs can track with the currents in the audio signal path circuit.

## BLOCK DIAGRAM




Revision Date: May 1998

Document No. 510 - 79 - 06

GENNUM CORPORATION P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3 tel. +1 (905) 632-2996
Web Site: www.gennum.com E-mail: hipinfo@gennum.com

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | VALUE / UNITS |
|---|---|
| Supply Voltage | 3 V DC |
| Min. voltage any pin | GND - 200 mV |
| Max. voltage any pin | $V_{CC}$ + 200 mV |
| Operating temperature | 0 to 50 °C |

**CAUTION**
CLASS 1 ESD SENSITIVITY

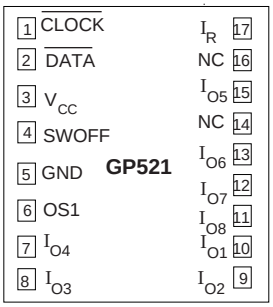



Fig. 1 Chip Pad Diagram

## ELECTRICAL CHARACTERISTICS

Current into IC considered positive.

Conditions: Temperature = 25°C, $I_R$ = 4 µA, $V_{cc}$ = 1.3 V

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | - | 1.3 | 3 | V |
| Supply Current: | $I_{CC}$ | Normal operation mode<br>Program mode | -<br>- | -<br>- | 25<br>1 | µA<br>mA |
| EEPROM read / write cycles | | | 1000 | - | - | cycles |
| Low Input Voltage "low" | $V_L$ | | - | - | 200 | mV |
| High Input Voltage "high" | $V_H$ | | $V_{CC}$ - 0.2 | - | - | V |
| Clock Rate | $f_{CL}$ | | - | 6 | 50 | kHz |
| PROGRAMMABLE CURRENT SINKS | | | | | | |
| Reference current | $I_R$ | | - | - | 14 | µA |
| PCS Bias Voltage | $V_{PCS}$ | | 400 | 500 | - | mV |
| Number of Settings | | | N/A | 16 | N/A | |
| Output Current for set "15" | $I_{o15}$ | DAC set to 15 $V_{PCS}$ = 0.5 V (note 2) | 6.81 | 7.5 | 8.25 | µA |
| Linearity Error | $\eta$ | DAC set for 1,2,4,8 (note 1, 2) | N/A | ±10% | N/A | |
| Output Current offset "0" | $I_{OFFS}$ | DAC set to 0 (note 1, 2) | - | 0 | - | nA |
| Output Leakage Current | $I_L$ | DAC set to 0 $V_{PCS}$ = 0.5 V (note 1, 2) | - | 0 | - | nA |
| Early Voltage = $\frac{1}{\text{Channel length modulation}}$ | $V_a$ | DAC set to 15 (note 1, 2)<br>Set $V_{PCS}$ = 0.5V and<br>$V_{PCS}$ = 0.7V (S9 = b) | - | 37 | - | V |

All switches remain as shown in Test Circuit unless otherwise stated in condition columns.

**NOTES:**

1. Refer to the definition section
2. Measurements performed for all DAC's separately (SWS 1 to 8 closed sequentially).

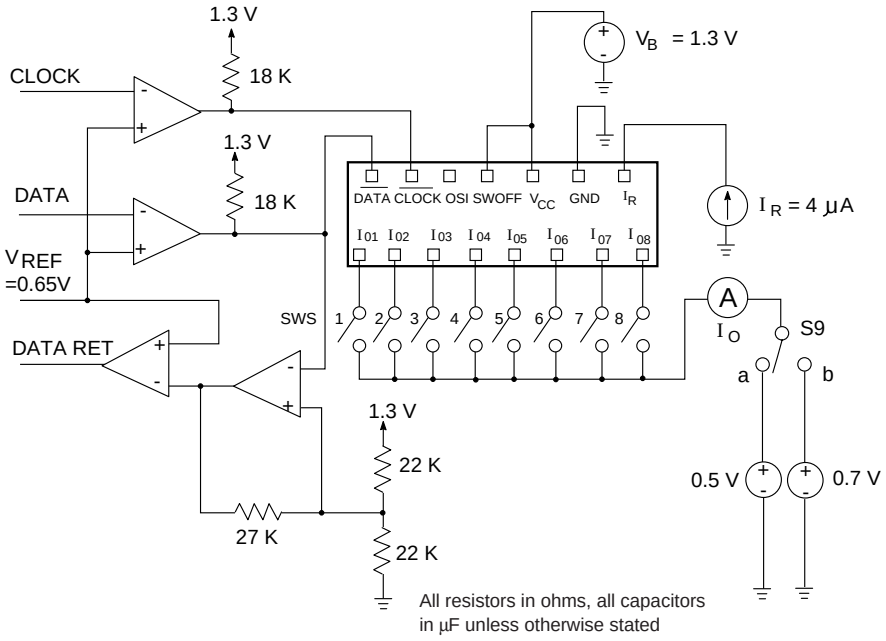



Fig. 2 Digital Test Circuit

## GP521 DIGITAL TESTING

The GP521 is tested for digital functionality via a series of *reads* and *writes* to the GP521.
For a summary of the actual testing refer to Document No. 520-35

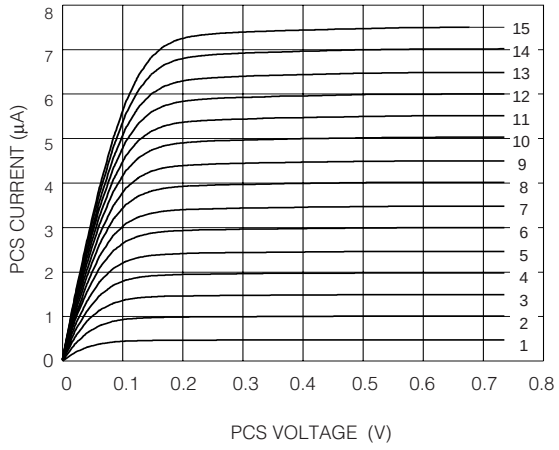



Fig. 3 PCS Current (Sink) vs PCS Voltage at DAC Setting 0 to 15, $I_R$ = 4µA

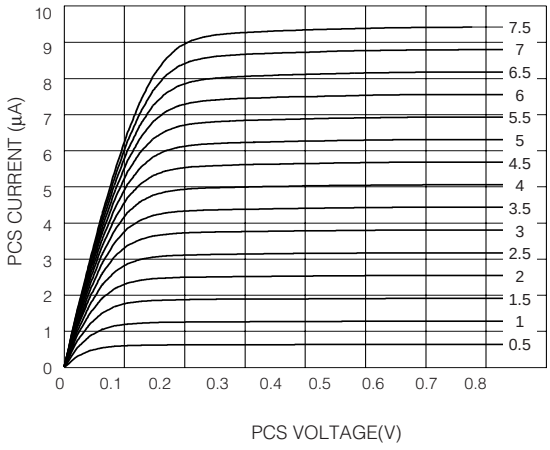



Fig. 4 PCS Current (Sink) vs PCS Voltage $I_R$ = 0 to 7.5µA (step 0.5µA) DAC set at 10

TYPICAL DISTRIBUTION of PCS CURRENT

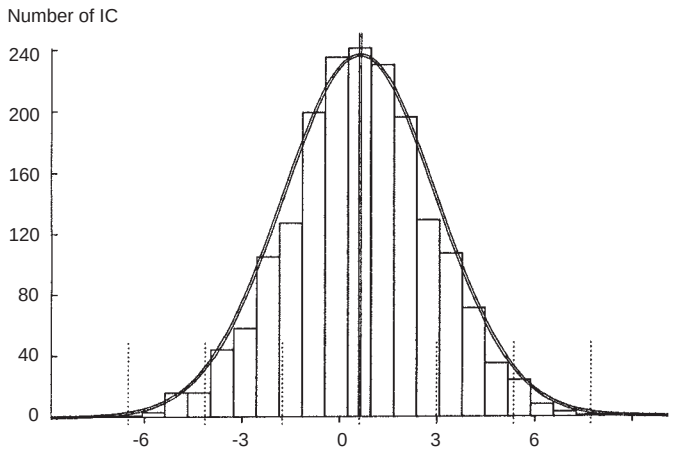



Fig. 5 Linearity Error (Digital Input set to 2) [%]

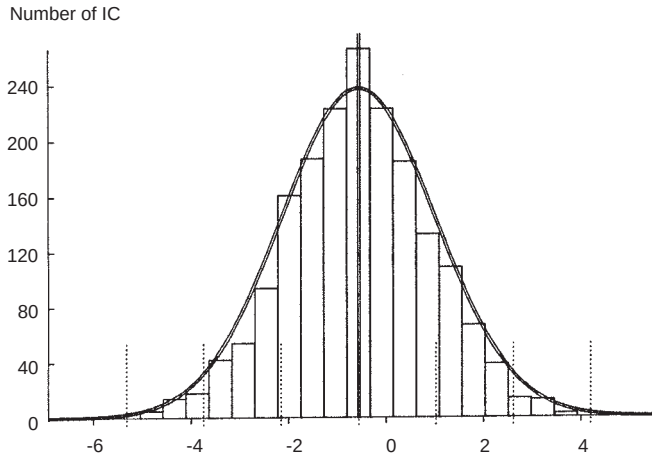



Fig. 6 Linearity Error (Digital Input set to 4) [%]

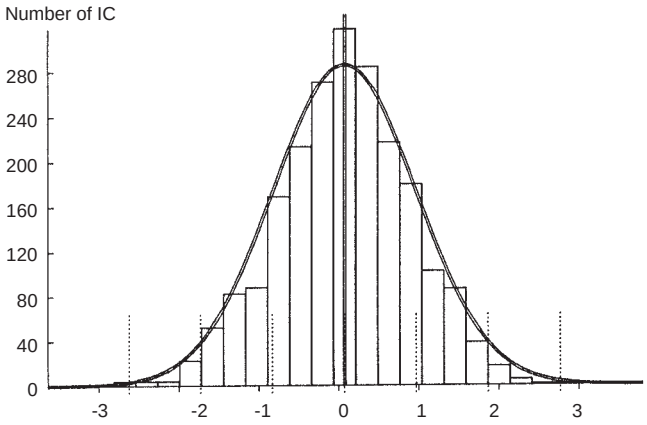



Fig. 7 Linearity Error (Digital Input set to 8) [%]

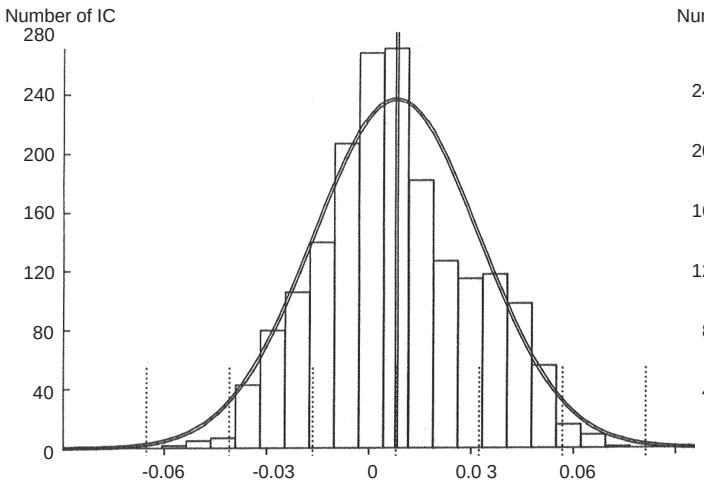



Fig. 8 Output Current Off set [μA]

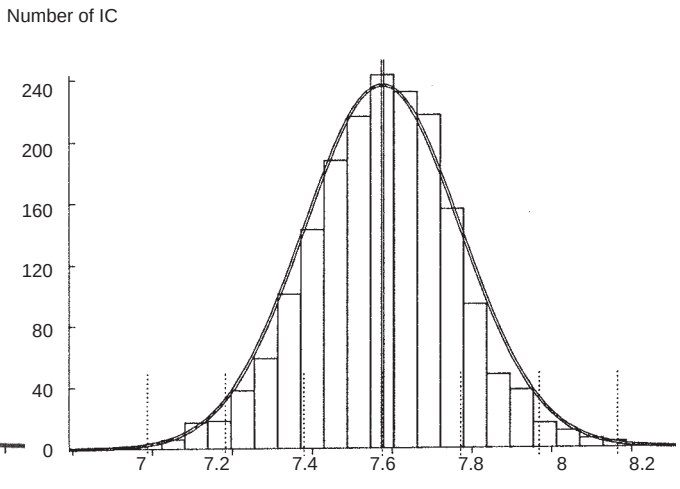



Fig. 9 Output Current for Digital Input set to 15 [μA]

* The data was collected on limited numbers of the chips.

## PIN DESCRIPTION

$\overline{\text{CLOCK}}$ - The clock pulses for synchronization of the data transfer. The clock pulses are provided by the programming unit.

$\overline{\text{DATA}}$ - The input/output pin allow for serial data transfer between the GP521 and the programming unit.

$V_{CC}$ - Recommended supply voltage for GP521 is 1.3V

SWOFF - The logic state of SWOFF determines whether the GP521 operates at 6 or 8 PCS configuration. When SWOFF is high, all eight ($I_{O1}$ to $I_{O8}$) PCS are available (8 PCS configuration) Figure 10.

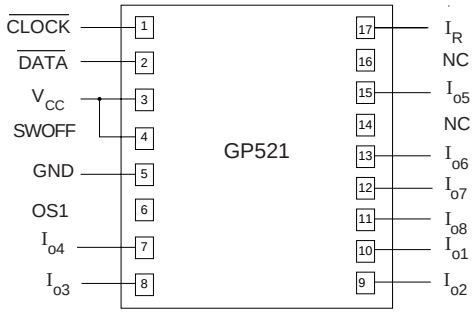



Fig.10 EIGHT OUTPUT CONFIGURATION

When SWOFF is low, four PCS ($I_{O5}$ to $I_{O8}$) are available; availablility of other two PCS is dependent on the voltage on pin OS1. For this configuration (6 PCS configuration) the necessary hardware connections are presented in Figure 11.

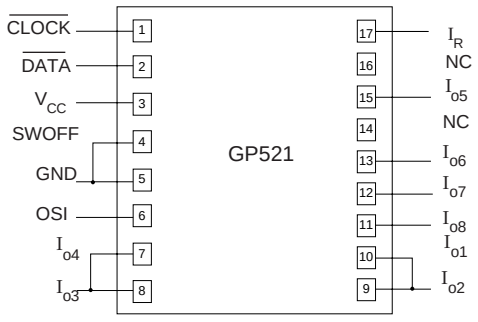



Fig. 11 SIX OUTPUT CONFIGURATION

OS1 - The voltage level on this pin determines the selection of four PCS ($I_{O1}$ to $I_{O4}$) for 6 PCS configuration. As indicated on Figure 11, pin $I_{O1}$, $I_{O2}$ and $I_{O3}$, $I_{O4}$ are connected together. If OS1 is low, $I_{O1}$ and $I_{O3}$ are set to high impedance. Therefore the PCS, $I_{O2}$ and $I_{O4}$ are permitted to sink current.

Similarly if OS1 is high, $I_{O2}$ and $I_{O4}$ are set as high impedance points. This allows PCS $I_{O1}$ and $I_{O3}$ to sink current.

TABLE 1 EFFECTS OF SWOFF AND OS1 INPUTS

| SWOFF | OS1 | OUTPUT | PCS Register Address |
|---|---|---|---|
| 0 | 1 | ( $I_{O1}$ and $I_{O3}$)* | (0001000 and 0001010) |
| 0 | 0 | ( $I_{O2}$ and $I_{O4}$)* | (0001001 and 0001011) |
| 1 | x | $I_{O1}$ | 0001000 |
| 1 | x | $I_{O2}$ | 0001001 |
| 1 | x | $I_{O3}$ | 0001010 |
| 1 | x | $I_{O4}$ | 0001011 |
| x | x | $I_{O5}$ | 0001100 |
| x | x | $I_{O6}$ | 0001101 |
| x | x | $I_{O7}$ | 0001110 |
| x | x | $I_{O8}$ | 0001110 |

Note* The complementary outputs are set as high impedance points.

$I_{O1}$ - $I_{O8}$ - Each pin is the output of the specific Programmable Current Sink (PCS). Each PCS consists of four bit EEPROM memory, Digital to Analog Converter (DAC) and current sink. The EEPROM stores the four bit information written during initialization of the system. Four bit memory allows for 16 settings of the current sink. For simplicity, consider the current sink as a variable resistor. The value of this resistor is dependent on the DAC setting; DAC is controlled by the binary value of the RAM memory. To define output current of the current sink, it is necessary to set the voltage applied to the PCS output. This voltage is recommended to be 0.5 V. If the binary value of the EEPROM increases by one, the value of the output current increases by 0.125 x $I_R$.

$I_R$ - The reference current delivered from the outside source (eg. GP520A). This current determines the incremental value of the programmable current sink for each increase of the EEPROM address value. The valid addresses run from 0 through to 15. Each step is defined as $\Delta I = I_R \times 0.125$, therefore maximum current at setting 15 is equal to $I_{15} = I_R \times 0.125 \times 15$.

## GP521 REGISTERS

There are four types of registers used in the GP521. Their functions are described as follows:

ID - Hearing instruments identification register. The contents are set to 0000000 indicating a visual identification is required.

STATUS - Monitors the present state of the GP521 and records whether an error has occurred in the previous dialogue with the program unit. The STATUS is *read only* register.

OPERATION - Performs EEPROM *read to* (*write from*) RAM operations. The desired operation is specified by the data sent to the register. This is *write-only* register.

PCS - Stores the programmable current sink settings.

The register address definitions and the data bit definitions are given in Tables 2 and 3. The STATUS and OPERATION registers are two different registers sharing a common address.

TABLE 2 REGISTER ADDRESS DEFINITIONS

| ADDRESS | FUNCTION | TYPE | MEMORY CELL |
|---|---|---|---|
| 0000000 | ID | read only | ROM* |
| 0000001 | STATUS/OP | read/write | RAM / ROM |
| 0000010 to 0000111 | unused* | | |
| 0001000 | PCS $I_{O1}$ | read/write | RAM +EEPROM |
| 0001001 | PCS $I_{O2}$ | read/write | RAM +EEPROM |
| 0001010 | PCS $I_{O3}$ | read/write | RAM +EEPROM |
| 0001011 | PCS $I_{O4}$ | read/write | RAM +EEPROM |
| 0001100 | PCS $I_{O5}$ | read/write | RAM +EEPROM |
| 0001101 | PCS $I_{O6}$ | read/write | RAM +EEPROM |
| 0001110 | PCS $I_{O7}$ | read/write | RAM +EEPROM |
| 0001111 | PCS $I_{O8}$ | read/write | RAM +EEPROM |
| 0010000 to 1111111 | unused* | | |

*The GP521 will indicate an error if an unused register is accessed or a *write to* is attempted to a *read-only* register.

TABLE 3 DATA BIT DEFINITIONS

| DATA BIT | STATUS REGISTER | OPERATION REGISTER | PCS REGISTER* |
|---|---|---|---|
| 0000000 | | No operation | set $I_O = 0$ |
| XXXXXX1 | PCS outputs may be different than EEPROM values | Load EEPROM values into PCS | set $I_O = 0.125\ I_R$ |
| XXXXX1X | Circuit busy with EEPROM write | Save PCS values in EEPROM memory | set $I_O = 0.25\ I_R$ |
| XXXX1XX | Transmission error on previous dialogue | unused | set $I_O = 0.5\ I_R$ |
| XXX1XXX | Bad Address and/or Operation Error on previous dialogue | unused | set $I_O = 1.0\ I_R$ |
| XX1XXXX | unused | unused | unused |
| X1XXXXX | unused | unused | unused |
| 1XXXXXX | unused | unused | unused |

*Note: 1. Combining data bits in a word is equivalent to combining the corresponding definitions. (i.e. 0001101 in the PCS register would set the output to $I_O = 1.625\ I_R$ ).
2. The upper 3 data bits are ignored except for parity checking.

## ERROR DETECTION

The errors detected and recorded in the STATUS register are defined as follows:

TRANSMISSION ERROR

This error occurs whenever an incoming parity error is detected and/or the GP521 detects that it is not synchronized with the programming unit. This type of error sets a STATUS bit and puts the circuit in unsynchronized mode. The STATUS bit clears after a successful *read/write* operation.

BAD ADDRESS and / or OPERATION ERROR:
Status register is set when:

- any *write* operation is attempted while an EEPROM *write* is in progress
- a *write* operation is attempted on the ID register
- any operation is attempted on an unused address.

This type of error sets a STATUS bit and sets the parity bit of the returned data stream to the incorrect value. This bit is reset at the conclusion of a acceptable *read* or *write* operation.

## COMMUNICATION FORMAT

The dialogue between the programming unit and the GP521 consists of 32 bits being sent to the GP521 which responds by returning 16 bits to the programming unit. A complete dialogue consisting of 48 bits as seen on the $\overline{DATA}$ line is as follows:

From Program Unit:

$\overline{f}\ 1\ \overline{a_0}\ 0\ \overline{a_1}\ 1\ \overline{a_2}\ 0\ \overline{a_3}\ 1\ \overline{a_4}\ 0\ a_5\ 1\ a_6\ 0$

$d_0\ 1\ d_1\ 0\ d_2\ 1\ d_3\ 0\ d_4\ 1\ d_5\ 0\ d_6\ 1\ p_0\ 0$

From GP521:

$r_0\ 1\ r_1\ 0\ r_2\ 1\ r_3\ 0\ r_4\ 1\ r_5\ 0\ r_6\ 1\ p_1\ 0$

The dialogue begins with the bit *f* and ends with the two bits $p_1$, 0. The data and synchronization bits must be correct on the falling edge of CLOCK. This relationship is shown in Figure 12.

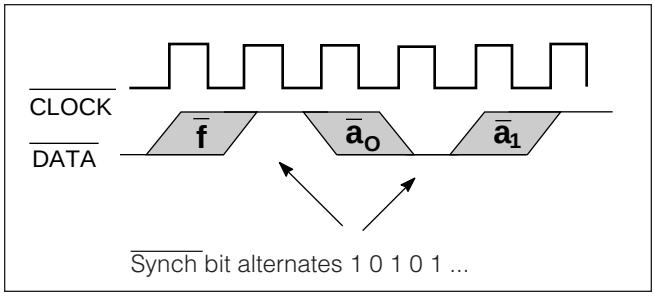



Fig. 12

The alternating 1's and 0's between information bits are used to check whether the GP521 is synchronized with the prgramming unit. The information bits are defined as:

f (function bit) f = 0 *Write* data to specified memory address
f = 1 *Read* data from specified memory address

$a_6a_5a_4a_3a_2a_1a_0$ 7 bit address to read/write to
$d_6d_5d_4d_3d_2d_1d_0$ 7 bit data to *write to* memory

$p_O$ parity bit for information from program unit (odd parity)

$r_6r_5r_4r_3r_2r_1r_0$ 7 bit data. If f=0, the data will echo the 7 bit data sent by the programming unit. If f=1, the data is read from the memory address.

$p_1$ Parity bit for data sent by GP521 (odd parity)

## SYNCHRONIZATION OF THE GP521 WITH PROGRAMMER

The synchronization of the program with the GP521 is done using a code in the data stream which cannot occur during a correct dialogue. The GP521 looks for the following data sequence in the data stream:

$\overline{DATA}$ = 1010

where the final synchronization bit is a low. The next bit following the 4 bit synch code is assumed to be part of a valid dialogue. Once the GP521 is synchronized with the program unit, it is possible to perform a continuous sequence of dialogues without having to re-synchronize unless transmission errors occur. It is also possible to pause and continue the transmission provided the proper relationship between $\overline{CLOCK}$ and $\overline{DATA}$ is maintained.

To guarantee that the circuit synchronizes properly, the internal shift registers should be cleared by preceding the synch code with a string of bits containing a synch error.

An example of the data sequence that guarantees a correctly synchronized circuit is:

$\overline{DATA}$ = 11111010

## DEFINITIONS

### LINEARITY ERROR

Linearity error is defined as the difference between the actual current value for a given digital input setting and the current value indicated by the straight line through point $P_1$ and $P_{15}$.

The point $P_1$ is the current at the setting 1 (0001) of the digital input. (Figure 13)

The point $P_{15}$ is the current at the setting 15 (1111) of the digital input (Figure 13)

The current at set 0(0000) of the digital input is left out of the linearity error definition. This point on the characteristic is not correlated to other points (there is no current commutation through the current sink at set 0000).

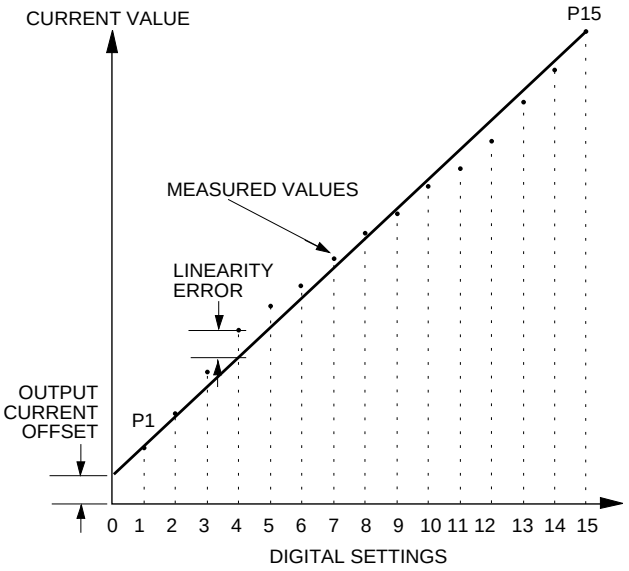



Fig. 13 PCS Current vs Digital Setting

### OUTPUT CURRENT OFFSET FOR SETTING 0

The current value determined by the extrapolation of the straight line (defined by the linearity error definition) at setting 0 (0000) of the digital input ( Figure 13) is defined as the ouput current offset.

### OUTPUT LEAKAGE CURRENT

Maximum sink current of the control output at setting 0 of the digital input is defined as output leakage current.

### EARLY VOLTAGE

The early voltage is defined by the following equation:

$$V_a = \text{Early Voltage} = \frac{1}{\text{channel length modulation}} =$$

$$= 0.5 - \frac{I_{0.5}\,(0.5 - 0.7)}{(I_{0.5} - I_{0.7})}$$

where

$V_a$ - Early Voltage

$I_{0.5}$ - sink output current at bias voltage $V_{PCS}$ = 0.5 V

$I_{0.7}$ - sink output current at bias voltage $V_{PCS}$ = 0.7 V

DOCUMENT IDENTIFICATION: DATA SHEET
The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

REVISION NOTES:

Updated to Data sheet