DATA SHEET

GPBA02A

I/O Extender

JAN. 06, 2011

Version 1.6

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I/O Extender

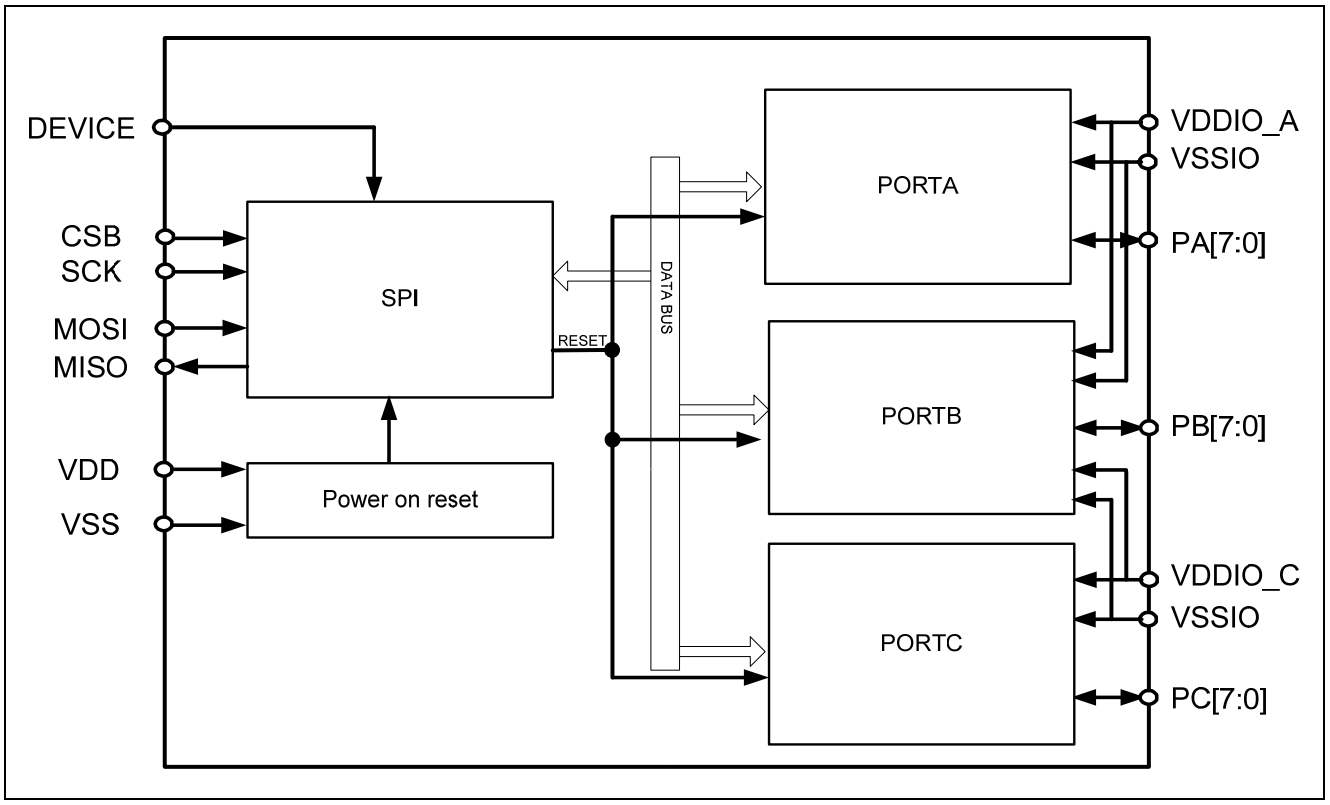
1. GENERAL DESCRIPTION

GPBA02A, a newly invented I/O Extender for micro-controller extends I/O pads usage. It equips with a standard SPI (Mode 0) communication-processing block, and combines with 24 I/O ports. With high-speed bit AND/OR/XOR capability for each bit in internal configuration registers, I/Os' status can be modified within fewer host CPU cycles. These I/Os are provided with strong driver ability to drive LED directly. More details are described as follow.

2. FEATURES

- Operating Voltage
  - Chip operating voltage (VDD): 2.2V – 5.5V
  - I/O operating voltage (VDDIO): 2.2V – 5.5V
- Standard SPI（Mode 0）Interface
  - 4 pins for SPI communication
  - Chip select signal CSB as transmit enable signal
  - Serial clock SCK (max 6MHz) as data synchronization signal for transmitting and receiving
  - Receives command and data from host via MOSI pin
  - Transmits data to host via MISO pin
- 24 I/Os
  - 24 bi-directional I/O lines
  - Users can set the corresponding registers to select pull high/low resistors, or buffer/open-drain outputs.
  - Users can write the corresponding registers to execute high-speed AND/OR/XOR function for each bit in those I/O configuration registers.
- Reset Management
  - Power on reset
  - Software control reset

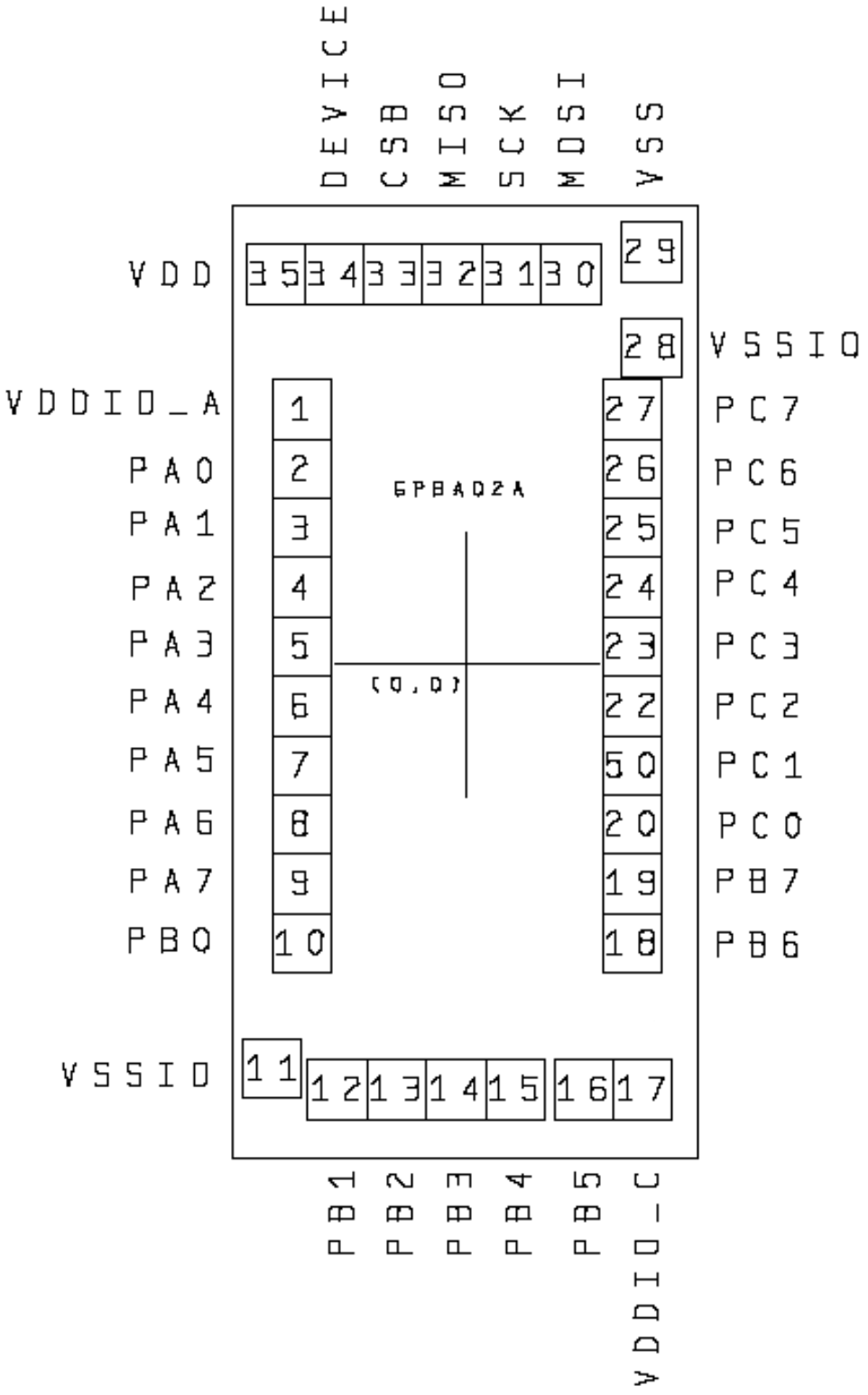
3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Package PIN No.	Type	Description
DEVICE	34	30	I	Device select signal, optional. (Device is defaulted as 0 when DEVICE pin is floating)
CSB	33	29	I	Chip select signal for SPI interface, low active.
SCK	31	27	I	Clock signal for SPI interface.
MOSI	30	26	I	Data input pin for SPI interface.
MISO	32	28	O	Data output pin for SPI interface.
PA [7:0]	2-9	42-35	I/O	General-purpose inputs/outputs, software command configurable. Belong to VDDIOA power group.
PB [7:0]	10, 12-16, 18-19	13-12, 8-4, 43	I/O	General-purpose inputs/outputs, software command configurable. PB0 belong to VDDIOA power group, PB[7:1] belong to VDDIOC power group.
PC[7:0]	20-27	21-14	I/O	General-purpose inputs/outputs, software command configurable. Belong to VDDIOC power group.
VDD	35	31	P	Digital circuit power input.
VSS	29	25	P	Digital circuit ground input.
VDDIO_A	1	34	P	Port A and Port B circuit power input, supply power for PA[7:0] and PB0.
VSSIO	11, 28	3, 22	P	Port A, Port B, Port C circuit ground input.
VDDIO_C	17	9	P	Port B and Port C circuit power input, supply power for PB[7:1] and PC[7:0].

4.1. PAD Assignment

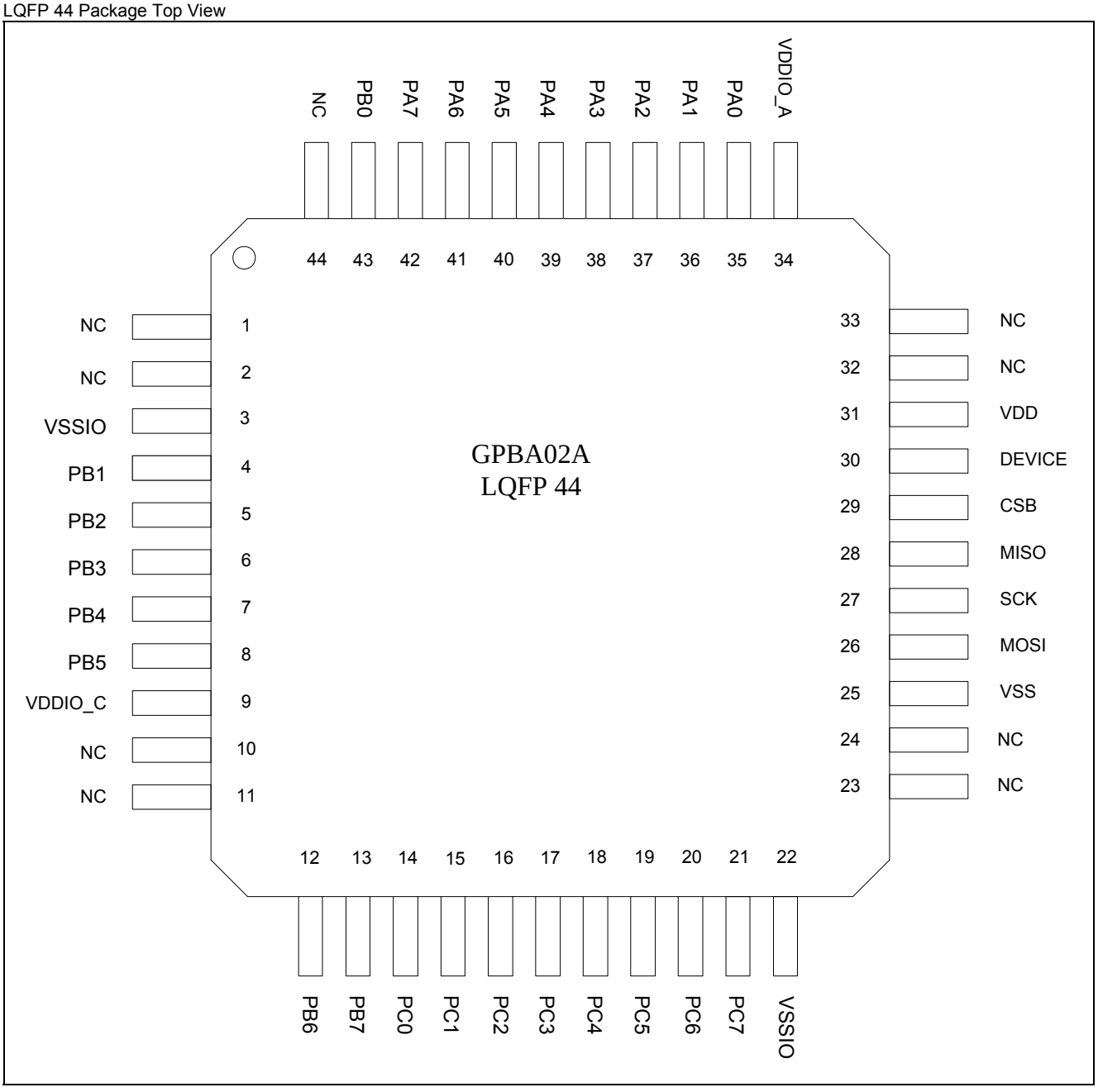


Please connect substrate to VSS or keep floating

Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.
Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

4.2. Pin Map

LQFP 44 Package Top View



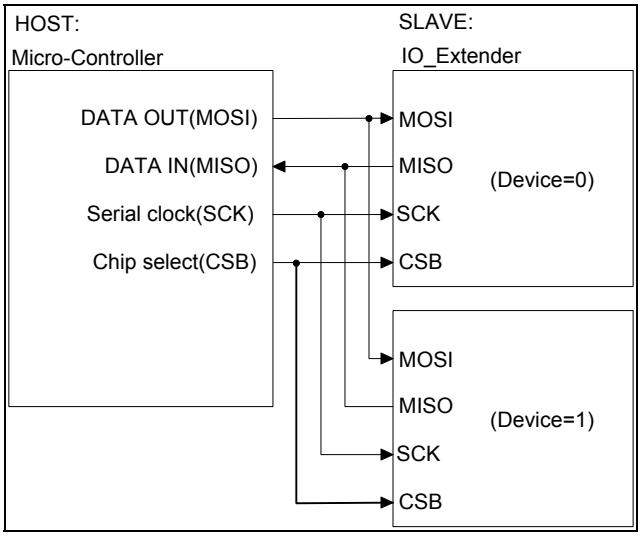
5. FUNCTIONAL DESCRIPTIONS

The I/O extender provides 24 I/O ports. Which are divided into three groups: Port A, Port B and Port C. These I/O ports can be configured as normal I/O ports. Also, each port has programmable pull high/low input and open drain output function. The device is optimal for various fields such industrial and commercial applications.

5.1. SPI

The SPI supports full-duplex synchronous transfer between a Master device and a Slave device. GPBA02A only supports Slave Modes for SPI transfer (MODE 0).

5.1.1. SPI Serial Interface



As shown in the above diagram, the host can connect to two I/O extenders. The device selecting bit is controlled by software command from the host. If the corresponding bit (B6) of the command is set as 0, the apparatus signed with Device=0 will selected. And else, if the corresponding bit (B6) of the command is set as 1, the apparatus signed with Device=1 will selected. The I/O extender has separated pins designated for data transmission (MISO) and reception (MOSI). When the device is selected and the CSB pin is low, data and command are able to be transmitted via MOSI and MISO pins. And when the device is not selected or the CSB pin is not low, data will not be accepted via MOSI pin, and the serial output pin (MISO) will remain in high impedance state. The serial clock pin (SCK) of I/O extender is always set as an input; the I/O extender always operates as a slave.

5.1.2. Data Frame Description

When the host writes data into I/O extender registers, one writing data frame will form 16 bits data. The first 8 bits are command data, and the following 8 bits data will be written into register. The host sends command and value from MSB to LSB via MOSI pin. During write operation cycles, the MISO pin keeps in high impedance status.

When the host reads data from I/O extender registers or I/O ports, the read command byte will first be sent to I/O extender from MSB to LSB via MOSI pin during the first 8 SCK clock cycles. And the value byte read from corresponding register will be sent to host via MISO pin during the following 8 SCK clock cycles from MSB to LSB.

HOST writes data to register:

MOSI	COMMAND	DATAIN
MISO	Z	Z

HOST reads data from register:

MOSI	COMMAND	X
MISO	Z	DATAOUT

5.1.3. Command List

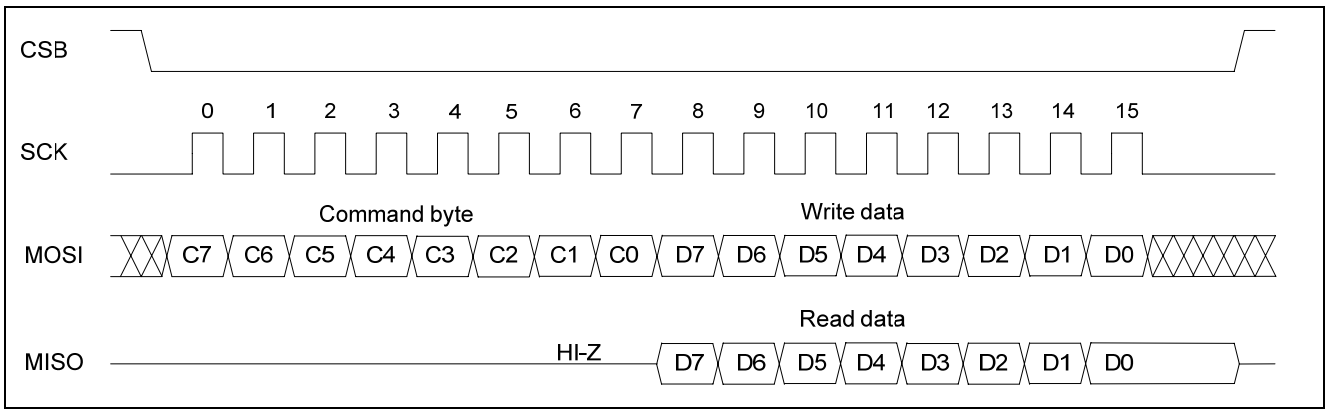
Command	B7(MSB)	B6	B5	B4	B3	B2	B1	B0
Write register	1	1*	Register address					
Read register	0	1*	Register address					
Reset	FFH							
No response	others							

Note: 1* is optional and user can choice device 1 or 0 (two device) in one SPI interface with bonding option PAD (DEVICE).

As shown in the command list, the read or write command consists of 8 bits data. The highest bit B7 represents reading or writing. When this bit is low, the command executes a read instruction. On the contrary, when this bit is high, the command executes a write instruction. The bit B6 is used for device selecting and the value depends on the bonding option bit. This option bit should be configured as low or high by users in advance. When DEVICE pin is floating, the value of B0 will be defaulted as 0. If the value of B6 is the same as the option bit, this I/O extender is selected, and this command will be executed. Otherwise, this I/O extender will not respond. The content of B5-0 is used for register address. The reading or writing command is executed for the register with this address. In addition, if the B7-0 of the command is equal to FFH, all those built-in registers will be reset to the initial values. This software command and power-on reset can make all the registers to reset.

5.1.4. Waveform of SPI Pins

The following diagram shows that when the host writes data into or reads data from this I/O extender, it will send a low voltage chip-selecting signal on CSB pin. And the host needs to generate 16 clock pulses on SCK pin for a data frame's synchronization. The CSB should keep in low voltage until this data frame transmission is done (It is suggested the CSB should keep in low voltage at least half a SCK clock cycle after the 16th pulse). And when the host starts a new data frame transmission, the CSB signal should change from high voltage to low voltage. It means that the CSB cannot maintain in low voltage even if the host transmits two or more data frames continuously. The CSB needs shift to high voltage between every two data frames transmission. The I/O extender receives command-byte and writing-byte via MOSI pin, and transmits reading-byte via MISO pin.



5.2. Control Registers

As shown in the registers list, the address can be represented by 6 bits binary data (suppose to be B [5:0]). For the normal I/O operation, users can write data into address 0xH (B[5:4]=00) registers (BUFA/B/C, DIRA/B/C and ATTA/B/C) to achieve various IO functions, and read data from address 0xH (AB5-4=00) registers (BUFA/B/C, DIRA/B/C and ATTA/B/C) and ports (DATA/B/C) to obtain register and IO ports states.

In order to speed up I/O operation, GPBA02A provides some special designed registers to help users to reduce operation time. Users can write data to address 1xH (AB5-4=01) registers (BUFA/B/C, DIRA/B/C and ATTA/B/C) to speed up AND operation for these corresponding 0xH registers. Users can write data to address 2xH (AB5-4=10) registers (BUFA/B/C, DIRA/B/C and ATTA/B/C) to speed up OR operation for these corresponding 0xH registers. Users can write data to address 3xH (AB5-4=11) registers (BUFA/B/C, DIRA/B/C and ATTA/B/C) to speed up XOR operation for these corresponding 0xH registers.

Control registers list:

Function	Address	B7	B6	B5	B4	B3	B2	B1	B0	Comment	Default
IO Port	00H(R/W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	BUFA	00
	01H(R/W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	BUFB	00
	02H(R/W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	BUFC	00
	03H(R/W)	-	-	-	-	-	-	-	-	N/A	--
	04H(R/W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	DIRA	00
	05H(R/W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	DIRB	00
	06H(R/W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	DIRC	00
	07H(R/W)	-	-	-	-	-	-	-	-	N/A	--
	08H(R/W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	ATTA	00
	09H(R/W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	ATTB	00
	0AH(R/W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	ATTC	00
	0BH(R/W)	-	-	-	-	-	-	-	-	N/A	--

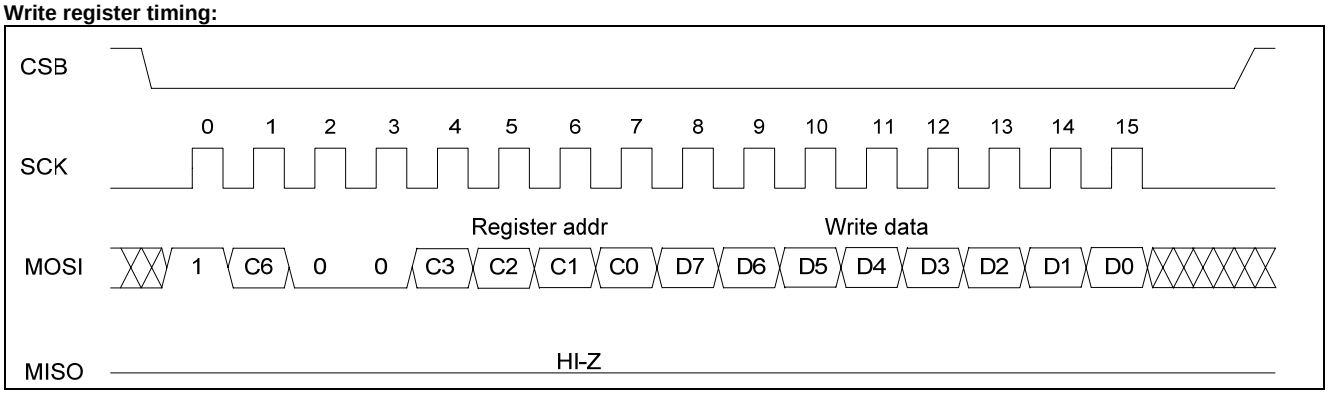
Function	Address	B7	B6	B5	B4	B3	B2	B1	B0	Comment	Default
IO Port	0CH(R)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	DATA	--
	0DH(R)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	DATB	--
	0EH(R)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	DATC	--
AND Group	10H(W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	BUFA AND	--
	11H(W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	BUFB AND	--
	12H(W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	BUFC AND	--
	13H(W)	-	-	-	-	-	-	-	-	N/A	--
	14H(W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	DIRAAND	--
	15H(W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	DIRBAND	--
	16H(W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	DIRCAND	--
	17H(W)	-	-	-	-	-	-	-	-	N/A	--
	18H(W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	ATTAAND	--
	19H(W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	ATTBAND	--
	1AH(W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	ATTCAND	--
	1BH(W)	-	-	-	-	-	-	-	-	N/A	--
	1CH(W)	-	-	-	-	-	-	-	-	N/A	--
	1DH(W)	-	-	-	-	-	-	-	-	N/A	--
	1EH(W)	-	-	-	-	-	-	-	-	N/A	--
	1FH(W)	-	-	-	-	-	-	-	-	N/A	--
OR Group	20H(W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	BUFAOR	--
	21H(W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	BUFBOR	--
	22H(W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	BUFCOR	--
	23H(W)	-	-	-	-	-	-	-	-	N/A	--
	24H(W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	DIRAOR	--
	25H(W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	DIRBOR	--
	26H(W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	DIRCOR	--
	27H(W)	-	-	-	-	-	-	-	-	N/A	--
	28H(W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	ATTAOR	--
	29H(W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	ATTBOR	--
	2AH(W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	ATTCOR	--
	2BH(W)	-	-	-	-	-	-	-	-	N/A	--
	2CH(W)	-	-	-	-	-	-	-	-	N/A	--
	2DH(W)	-	-	-	-	-	-	-	-	N/A	--
	2EH(W)	-	-	-	-	-	-	-	-	N/A	--
	2FH(W)	-	-	-	-	-	-	-	-	N/A	--
XOR Group	30H(W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	BUFAXOR	--
	31H(W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	BUFBXOR	--
	32H(W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	BUFCXOR	--
	33H(W)	-	-	-	-	-	-	-	-	N/A	--
	34H(W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	DIRAXOR	--
	35H(W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	DIRBXOR	--
	36H(W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	DIRCXOR	--
	37H(W)	-	-	-	-	-	-	-	-	N/A	--
	38H(W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	ATTAXOR	--
	39H(W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	ATTBXOR	--
	3AH(W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	ATTCXOR	--

Function	Address	B7	B6	B5	B4	B3	B2	B1	B0	Comment	Default
XOR Group	3BH(W)	-	-	-	-	-	-	-	-	N/A	--
	3CH(W)	-	-	-	-	-	-	-	-	N/A	--
	3DH(W)	-	-	-	-	-	-	-	-	N/A	--
	3EH(W)	-	-	-	-	-	-	-	-	N/A	--
	3FH(W)	-	-	-	-	-	-	-	-	N/A	--

5.3. Timing Diagram for SPI Control

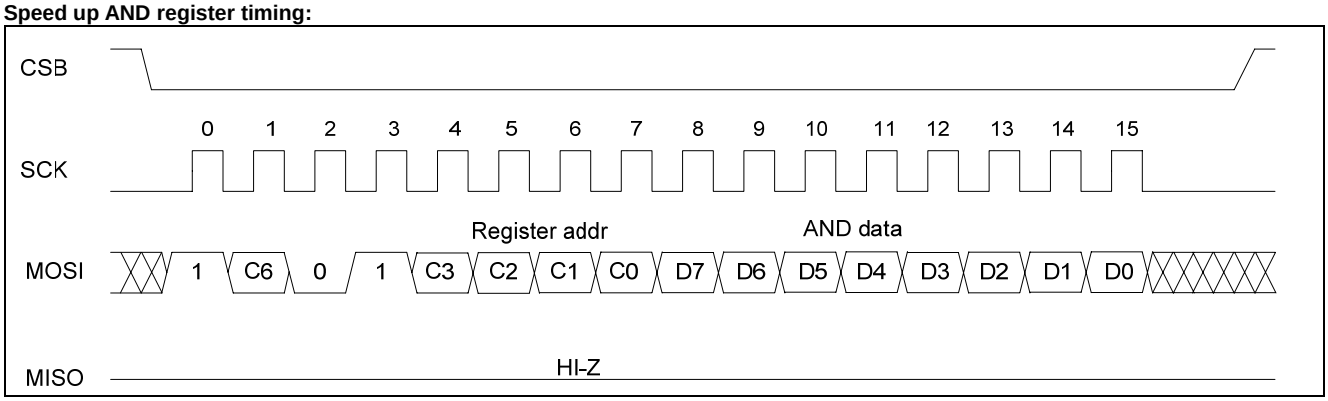
5.3.1. I/O Operation Function Timing

Write register timing:



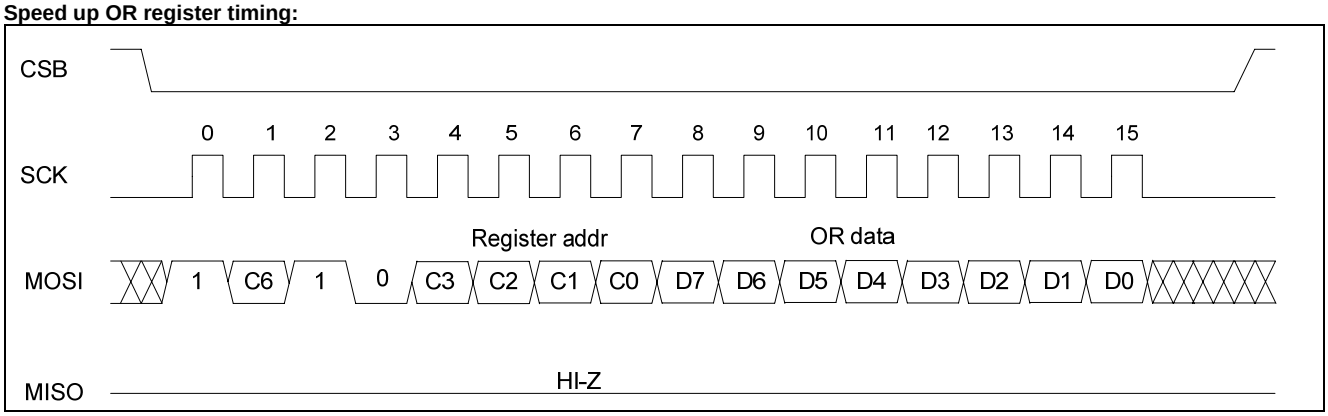
The command byte: C7=1; C6=device option value; C5-4=00; C3-0=register address. The write data byte: D7-0 is the value that will be written to the corresponding register. In write register cycles, the output pin (MISO) remains in high impedance state.

Speed up AND register timing:



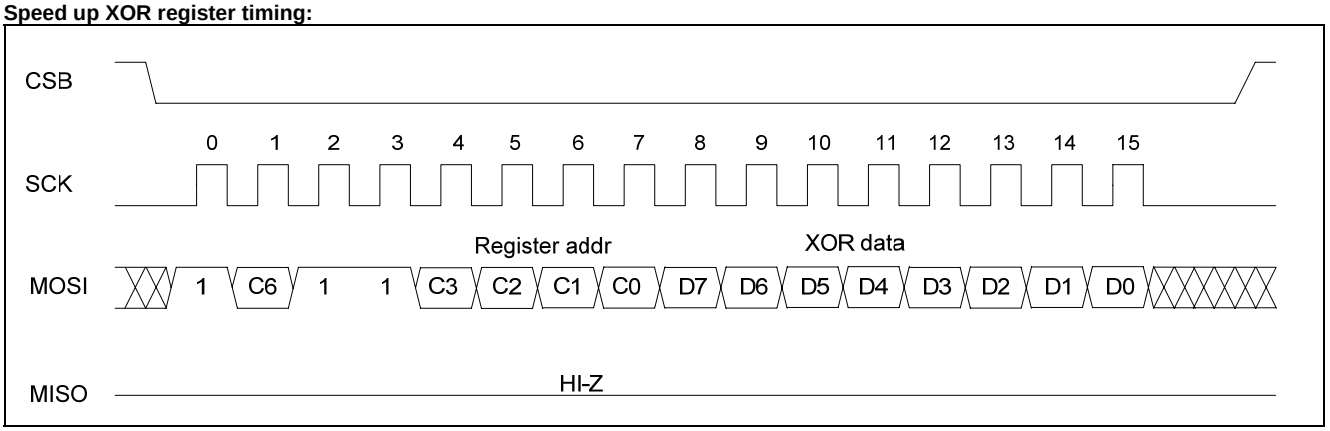
The command byte: C7=1; C6=device option value, C5-4=01, C3-0=register address. The speed up AND data byte: D7-0 is the value that will be AND with the corresponding 0xH register's value and then be written to the corresponding 0xH register. In speed up AND register cycles, the output pin (MISO) remains in high impedance state.

Speed up OR register timing:



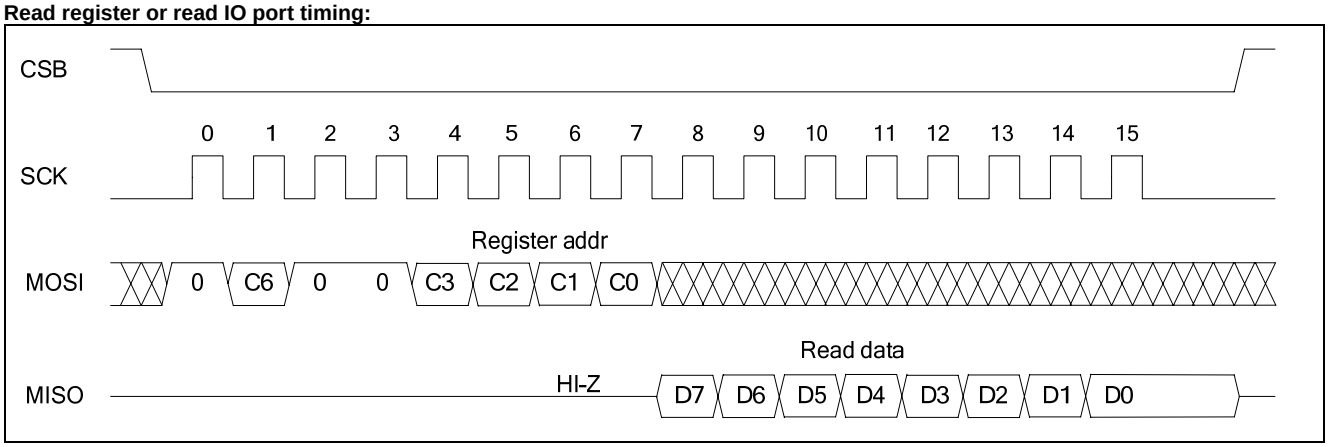
The command byte: C7=1; C6=device option value; C5-4=10; C3-0=register address. The speed up OR data byte: D7-0 is the value that will be OR with the corresponding 0xH register's value and then be written to the corresponding 0xH register. In speed up OR register cycles, the output pin (MISO) remains in high impedance state.

Speed up XOR register timing:



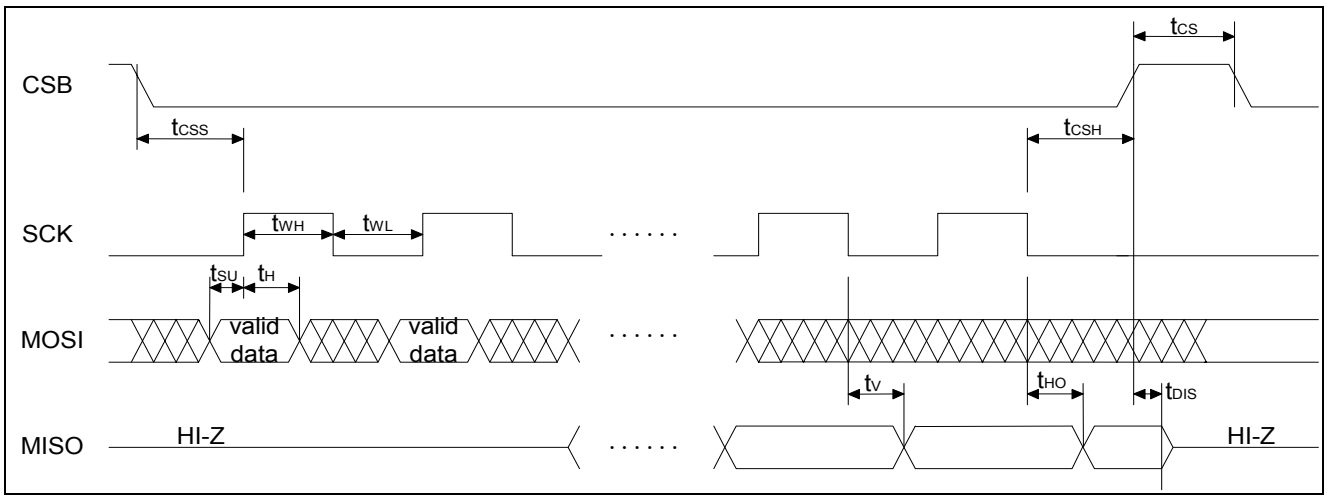
The command byte: C7=1; C6=device option value; C5-4=11; C3-0=register address. The speed up XOR data byte: D7-0 is the value that will be XOR with the corresponding 0xH register's value and then be written to the corresponding 0xH register. In speed up XOR register cycles, the output pin (MISO) remains in high impedance state.

Read register or read IO port timing:



The command byte: C7=0, C6=device option value, C5-4=00, C3-0=register address. The read data byte: D7-0 is the value that will be read from the corresponding register or corresponding IO ports. In read register or IO port cycles, the read data byte is transmitted via output pin (MISO) during the last 8 SCK clock cycles. After the 16th SCK clock, MISO remains the value of B0 until CSB is high.

5.3.2. SPI Synchronous Data Timing Specifications



Symbol	Parameter	Min.	Typ.	Max.	Units
f_{SCK}	SCK Clock Frequency	-	-	8	MHz
t_{RI}	Input Rise Time	-	-	4	ns
t_{FI}	Input Fall Time	-	-	4	ns
t_{WH}	SCK High Time	80	-	-	ns
t_{WL}	SCK Low Time	80	-	-	ns
t_{CSS}	CSB Setup Time	80	-	-	ns
t_{CSH}	CSB Hold Time	80	-	-	ns
t_{CS}	CSB High Time	50	-	-	ns
t_{SU}	Data In Setup Time	5	-	-	ns
t_{H}	Data In Hold Time	5	-	-	ns
t_{V}	Output Valid	-	-	75	ns
t_{HO}	Output Hold Time	0	-	-	ns
t_{DIS}	Output Disable Time	0	-	-	ns

5.4. Port A/B/C

Port A, Port B and Port C, each has eight programmable I/Os that are controlled by data register BUFA/B/C, direction control register DIRA/B/C, and attribution control register ATTA/B/C. BUFA/B/C is used to store the data content for output. Reading DATA/B/C will get pad's status and latch current's status into internal latching register.

There is a built-in pull-high/low resistor on each pad. PA/B/C [7:0] has pull-high/low resistors that can be configured with pull-high or pull-low registers. These pull-high/low resistors can be selected by I/O configuration register (BUFA/B/C, DIRA/B/C, and ATTA/B/C).

The maximum number of IO ports used for LED driver is 8 (with sink output). And these IO ports closed to VSSIO pad are recommended to be firstly for LED driver.

For example:

8 should select PA6, PA7, PB0, PB1, PB2, PB3, PC6 and PC7.

6 should select PA7, PB0, PB1, PB2, PC6 and PC7.

5 should select PA7, PB0, PB1, PB2 and PC7.

The corresponding pads are assigned for GPBA02A as following:

PIN	Pull High/Low Resistance@VDDIO=5V	IN	OUT Current @VDDIO=3V
PA7	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PA6	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PA5	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PA4	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PA3	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PA2	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PA1	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PA0	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PB7	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PB6	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PB5	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PB4	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PB3	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PB2	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PB1	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PB0	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA

PIN	Pull High/Low Resistance@VDDIO=5V	IN	OUT Current @VDDIO=3V
PC7	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PC6	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PC5	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PC4	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PC3	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PC2	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PC1	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PC0	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA

5.4.1. I/O Cell Configuration

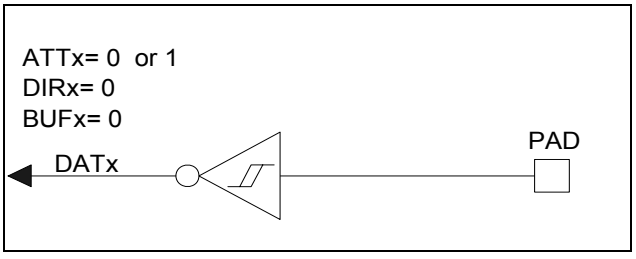
Mode: output high, output low, input with PL, input with PH, input with high Z, open drain NMOS output, open drain PMOS output.
IO function:

5.4.2. Combination IO Status to Archive IO Function

ATT_X	DIR_X	BUF_X	IO status	Function
0	0	0	Floating(default)	Floating input
0	0	1	Pull low	Pull low input
1	0	1	Pull high	Pull high input
0	1	0	Output low	Buffer output
0	1	1	Output high	
1	0	0	Floating	Open drain P-MOS output
1	1	0	Output high	
1	0	1	Pull high	Wire AND (inverted)
1	1	1	Output low	
0	1	0	Output low	Open drain N-MOS output (inverted)
0	0	0	Floating	
0	0	1	Pull low	Wired OR
0	1	1	Output high	
0	0	0	Floating	Dynamic pull low input
0	0	1	Pull low	
1	0	0	Floating	Dynamic pull high input
1	0	1	Pull high	
1	1	0	Output high	Inverted buffer output
1	1	1	Output low	

Input with high Z:

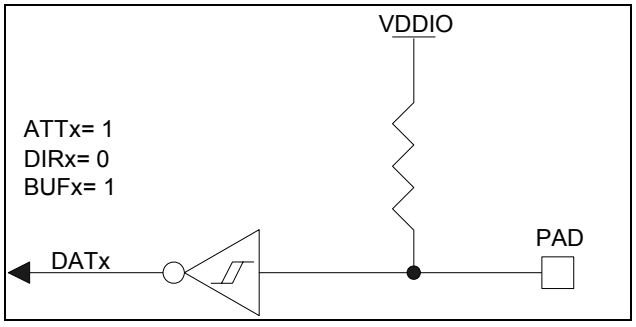
As shown in the above I/O Cell Configuration table and Control Registers table, the default values of all these registers are 0. And the default states of all these I/O ports are input with high Z. If PA/B/Cx is expected to set as input with high Z port (floating), the corresponding Bx of 00H/01H/02H (BUFA/B/C) and 04H/05H/06H (DIRA/B/C) both should be cleared as 0. In this case, the values of corresponding ATTA/B/Cx bit do not have to consider it.



Input with pull high resistor (PH):

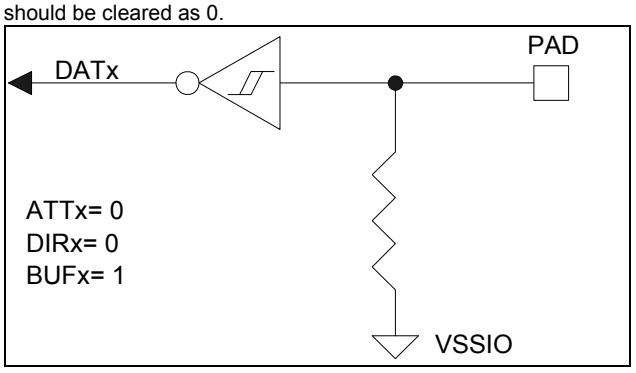
As shown in the above I/O Cell Configuration table and Control Registers table, each I/O port can be set as Input with pull high

resistor port independently. If PA/B/Cx is expected to set as Input with pull high resistor port, the corresponding Bx of 00H/01H/02H (BUFA/B/C) and 08H/09H/0AH (ATTA/B/C) both should be set as1, and the corresponding Bx of 04H/05H/06H (DIRA/B/C) should be cleared as 0.



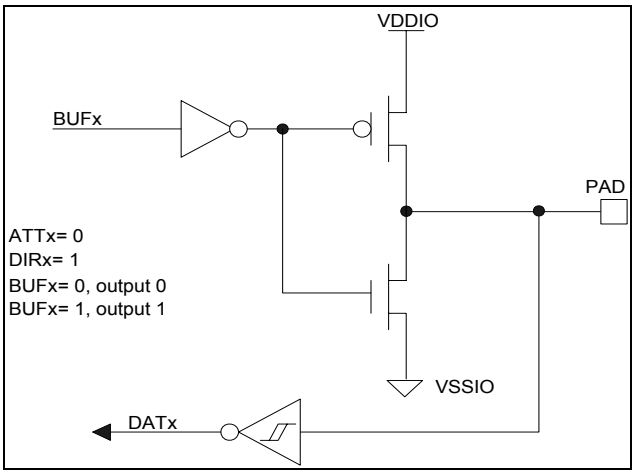
Input with pull low resistor (PL):

As shown in the above I/O Cell Configuration table and Control Registers table, each I/O port can be set as Input with pull low resistor port independently. If PA/B/Cx is expected to set as Input with pull low resistor port, the corresponding Bx of 00H/01H/02H (BUFA/B/C) should be set as 1, and the corresponding Bx of 04H/05H/06H (DIRA/B/C) and 08H/09H/0AH (ATTA/B/C) both should be cleared as 0.



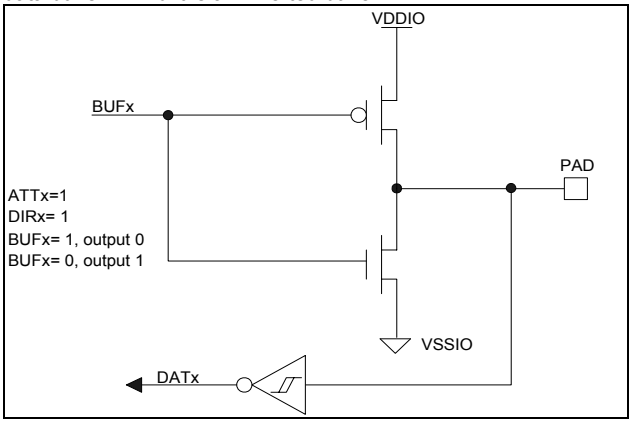
CMOS output high/low:

As is shown in the above I/O Cell Configuration table and Control Registers table, each I/O port can be set as CMOS output port independently. If PA/B/Cx is expected to set as CMOS output port, the corresponding Bx of 08H/09H/0AH (ATTA/B/C) should be configured as 0, and the corresponding Bx of 04H/05H/06H (DIRA/B/C) should be configured as 1. In addition, if the host writes 0 to corresponding Bx of 00H/01H/02H (BUFA/B/C), the PA/B/Cx will output low. And else if the host writes 1 to corresponding Bx of 00H/01H/02H (BUFA/B/C), the PA/B/Cx will output high. The register BUFA/B/C acts as output data buffer.



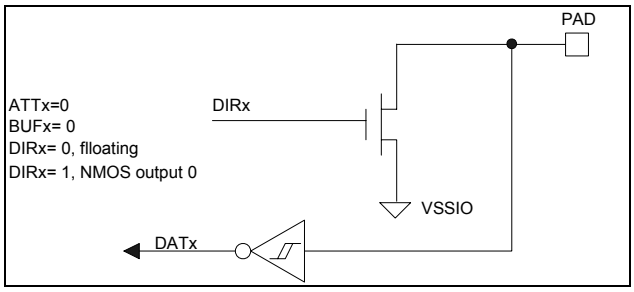
Inverted CMOS output high/low:

As is shown in the above I/O Cell Configuration table and Control Registers table, each I/O port can be set as CMOS output port independently. If PA/B/Cx is expected to set as CMOS output port, the corresponding Bx of 08H/09H/0AH (ATTA/B/C) and 04H/05H/06H (DIRA/B/C) should be configured as 1. In addition, if the host writes 0 to corresponding Bx of 00H/01H/02H (BUFA/B/C), the PA/B/Cx will output high. And else, if the host writes 1 to corresponding Bx of 00H/01H/02H (BUFA/B/C), the PA/B/Cx will output low. The register BUFA/B/C acts as output data buffer. And it is an inverted buffer.



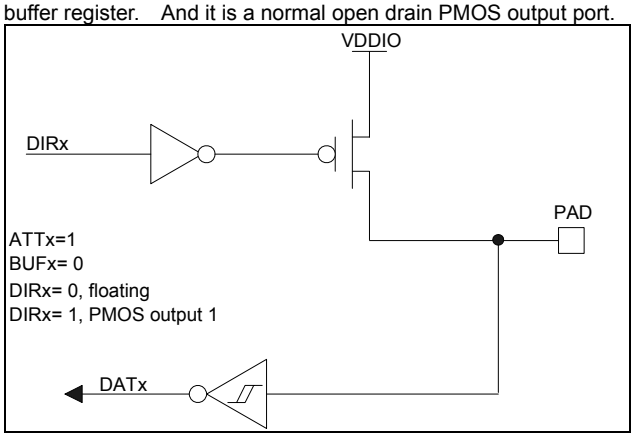
Inverted open drain NMOS output:

As is shown in the above I/O Cell Configuration table and Control Registers table, each I/O port can be set as open drain NMOS output port independently. If PA/B/Cx is expected to set as open drain NMOS output port, the corresponding Bx of 00H/01H/02H (BUFA/B/C) and 08H/09H/0AH (ATTA/B/C) should be cleared as 0, and then if the host writes 1 to the corresponding Bx of 04H/05H/06H (DIRA/B/C), the PA/B/Cx will output low. And if the host writes 0 to the corresponding Bx of 04H/05H/06H (DIRA/B/C), the PA/B/Cx is floating. In this case, the register DIRx acts as the output data buffer register. And it is an inverted open drain NMOS output port.



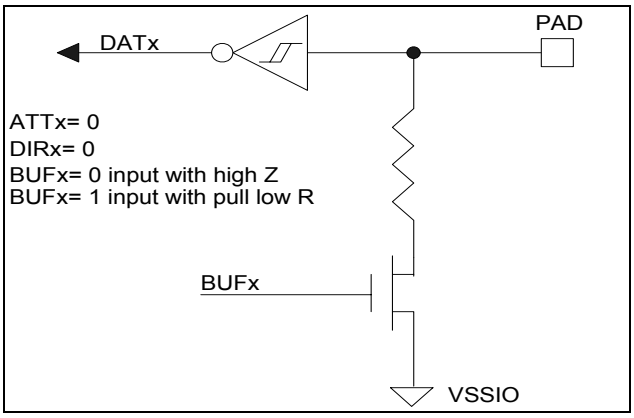
Open drain PMOS output:

As shown in the above I/O Cell Configuration table and Control Registers table, each I/O port can be set as open drain NMOS output port independently. If PA/B/Cx is expected to be set as open drain PMOS output port, the corresponding Bx of 00H/01H/02H (BUFA/B/C) should be cleared as 0, and 08H/09H/0AH (ATTA/B/C) should be set as1. If the host write 1 to the corresponding Bx of 04H/05H/06H (DIRA/B/C), the PA/B/Cx is an open drain PMOS output, and if host write 0 to the corresponding Bx of 04H/05H/06H (DIRA/B/C), the PA/B/Cx is floating. In this case, the register DIRx acts as the output data buffer register. And it is a normal open drain PMOS output port.



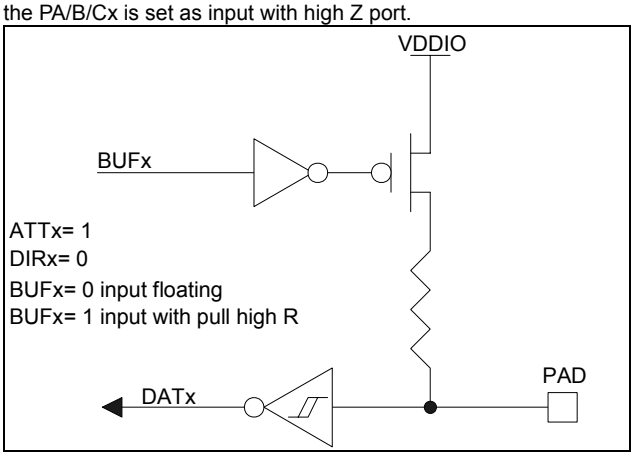
Dynamic pull low input:

As shown in the above I/O Cell Configuration table and Control Registers table, each I/O port can be set as dynamic Input with pull low resistor port independently. If PA/B/Cx is expected to set as dynamic Input with pull low resistor port, the corresponding Bx of 04H/05H/06H (DIRA/B/C) and 08H/09H/0AH (ATTA/B/C) both should be cleared as 0. If the corresponding Bx of 00H/01H/02H (BUFA/B/C) is set as 1, the PA/B/Cx is set as input with pull low resistor port, and else if the corresponding Bx of 00H/01H/02H (BUFA/B/C) is cleared as 0, the PA/B/Cx is set as input with high Z port.



Dynamic pull high input:

As is shown in the above I/O Cell Configuration table and Control Registers table, each I/O port can be set as dynamic Input with pull high resistor port independently. If PA/B/Cx is expected to set as dynamic Input with pull high resistor port, the corresponding Bx of 04H/05H/06H (DIRA/B/C) should be cleared as 0. And the corresponding Bx of 08H/09H/0AH (ATTA/B/C) should be set as1. If the corresponding Bx of 00H/01H/02H (BUFA/B/C) is set as1, the PA/B/Cx is set as input with pull high resistor port, and else if the corresponding Bx of 00H/01H/02H (BUFA/B/C) is cleared as 0, the PA/B/Cx is set as input with high Z port.



Note: Also, there are some other I/O register status combinations that can archive other IO functions, such as wired OR and wired AND functions. Users can use these functions dexterously.

5.4.3. Special Functions

Register Speed up AND function:

The content of ATTA/B/C, BUFA/B/C and DIRA/B/C can be speed up AND with any data by executing a special write instruction. According to the command data frame, when user writes data into register address of 1xH (B5-4 of command is 01), the writing data will be AND with the current data of this register and then be load in the exact register again. While executing AND instruction, the I/O extender reads the primary value of the register. This speed up AND operation only spends the host a write command cycle. It is a very useful function for I/Os' real time control.

Register Speed up OR function:

The content of ATTA/B/C, BUFA/B/C and DIRA/B/C can be speed up OR with any data by executing a special write instruction. According to the command data frame, when user writes data into register address of 2xH (B5-4 of command is 10), the writing data will be OR with the current data of this register and then be load in the exact register again. While executing OR instruction, the I/O extender reads the primary value of the register. This speed up OR operation only spends the host a write command cycle. It is a very useful function for I/Os' real time control.

Register Speed up XOR function:

The content of ATTA/B/C, BUFA/B/C and DIRA/B/C can be speed up XOR with any data by executing a special write instruction. According to the command data frame, when user writes data into register address of 3xH (B5-4 of command is 11), the writing data will be XOR with the current data of this register and then be load in the exact register again. While executing XOR instruction, the I/O extender reads the primary value of the register. This speed up XOR operation only spends the host a write command cycle. It is a very useful function for I/Os' real time control.

Comparing traditional AND/OR/XOR operation with speed up AND/OR/XOR operation (Reference by 6502 assembler):

	Traditional	Speed Up
AND Operation	Read a byte from I/O extender → MCU internal "AND" → Write a byte to I/O extender (Example: LDX #$01 JSR READ_SPI AND #$55 JSR WRITE_SPI)	Write a byte to "AND" address (Example: LDA #$55 LDX #$11 JSR WRITE_SPI)
OR Operation	Read a byte from I/O extender → MCU internal "OR" → Write a byte to I/O extender (Example: LDX #$01 JSR READ_SPI OR #$55 JSR WRITE_SPI)	Write a byte to "OR" address (Example: LDA #$55 LDX #$21 JSR WRITE_SPI)
XOR Operation	Read a byte from I/O extender → MCU internal "XOR" → Write a byte to I/O extender (Example: LDX #$01 JSR READ_SPI XOR #$55 JSR WRITE_SPI)	Write a byte to "XOR" address (Example: LDA #$55 LDX #$31 JSR WRITE_SPI)

Note: The sub routine READ_SPI and WRITE_SPI depends on the host structure, it takes at least 34 IO access cycles (enable*2+data_clock*8*2*2, no include data and flow control process) while using software to generate SPI waveform.

6. ELECTRICAL SPECIFICATION

6.1. Item Definition

Symbol	Definition	Symbol	Definition
V_{IH}	Input High Voltage	R_{LOW}	Pull low Resistor value
V_{IL}	Input Low Voltage	I_{OH}	Output High Current (Source)
I_{OP}	Operation Voltage	I_{OL}	Output Low Current (Sink)
R_{HIGH}	Pull high Resistor value	IZ	Output Leakage Current (Source)

6.2. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +85℃
I/O Total MAX Current	I_M	-120mA/400mA
LQFP44 Thermal resistance Junction to Case	θ_{JC}	20°C/W
LQFP44 Thermal resistance Junction to Ambient	θ_{JA}	55°C/W

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions, please see DC Electrical Characteristics.

6.3. DC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage1	VDDIO_A	2.2	-	5.5	V	-
Operating Voltage2	VDDIO_C	2.2	-	5.5	V	-
Operating Voltage3	VDD	2.2	-	5.5	V	-
Operating Current	I_{OP}	-	-	100	μA	VDDIO_X, VDD=5.5V, SCK=6MHz
Standby Current	I_{STB}	-	-	1.0	μA	VDDIO_X, VDD=5.5V, CSB=VDD
Input High Voltage (PA[7:0], PB[7:0], PC[7:0])	V_{IH}	0.7*VDDIO_X	-	-	V	VDDIO_X = 3.0V
Input Low Voltage (PA[7:0], PB[7:0], PC[7:0])	V_{IL}	-	-	0.3*VDDIO_X	V	VDDIO_X = 3.0V
Output High Voltage (PA[7:0], PB[7:0], PC[7:0])	V_{OH}	2.5	-	-	V	VDDIO_X = 3.0V I_{OH} = -8mA
Output Sink Voltage (PA[7:0], PB[7:0], PC[7:0])	V_{OL}	-	-	0.5	V	VDDIO_X = 3.0V I_{OL} = 20mA
Pull High Resistor (PA[7:0], PB[7:0], PC[7:0])	R_{HIGH}	-	100	-	kΩ	VDDIO_X =5.0V
Pull Low Resistor (PA[7:0], PB[7:0], PC[7:0])	R_{LOW}	-	100	-	kΩ	VDDIO_X = 5.0V

7. PACKAGE/PAD LOCATIONS

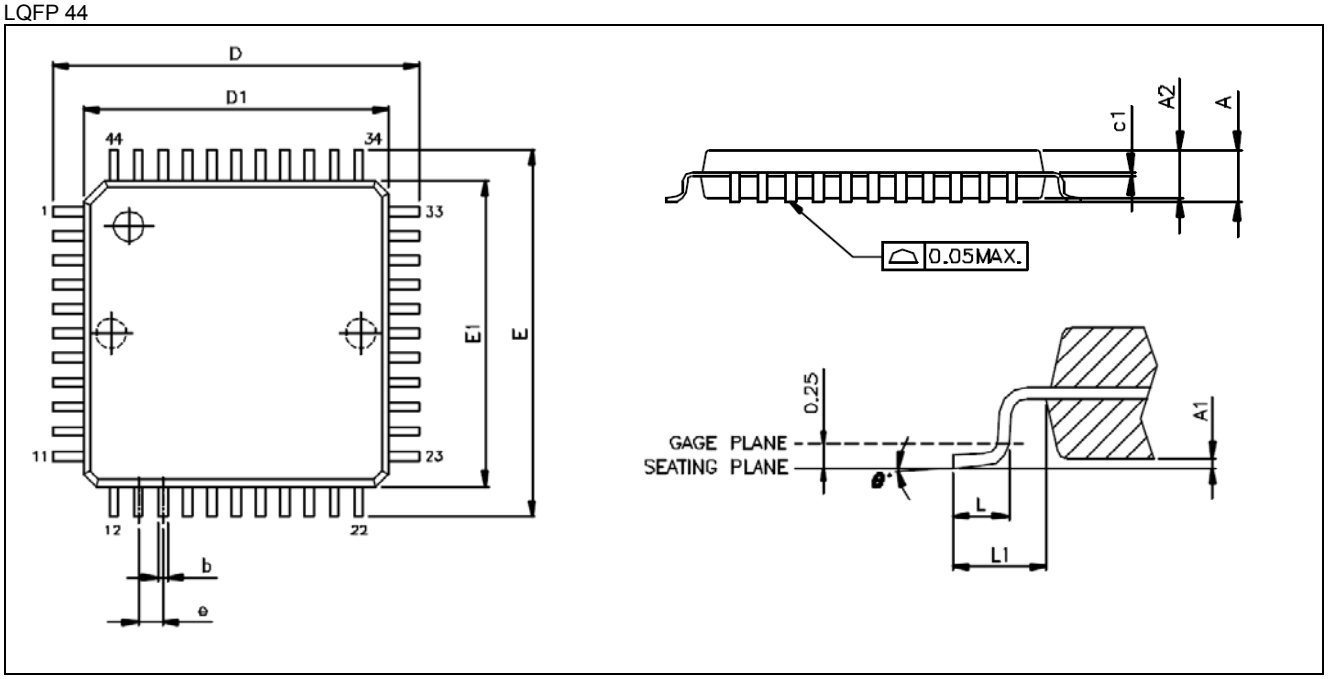
7.1. Ordering Information

Product Number	Package Type
GPBA02A -C	Chip form
GPBA02A-HL01x	Green Package - LQFP 44 RoHS

Note1: x = 1 - 9, serial number.

7.2. Package Information

LQFP 44



Symbol	Dimension in Millimeter		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
c1	0.09	-	0.16
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.80 BSC		
b	0.30	0.37	0.45
L	0.45	0.60	0.75
L1	1.00 REF		
θ°	0°	3.5°	7°

8. DISCLAIMER

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9. REVISION HISTORY

Date	Revision #	Description	Page
JAN. 06, 2010	1.6	1. Update read timing diagram 2. Modify product number 3. Remove wakeup function description.	12 20 3, 7, 8,12, 13, 16
JUN. 03, 2010	1.5	1. Modify 5.4.3 Special functions: Wakeup source function.	18
OCT. 06, 2008	1.4	1. Modify 4.SIGNAL DESCRIPTION. 2. Modify 6.2 Absolute Maximum Ratings.	4 20
APR. 28, 2008	1.3	Modify 6.3 DC Characteristics (T_A = 25℃).	20
AUG. 28, 2007	1.2	Add “LQFP44 Thermal resistance Junction to Case” and “LQFP44 Thermal resistance Junction to Ambient” to section 6.2.	23
AUG. 15, 2007	1.1	1. Modify “SIGNAL DESCRIPTION” in section 4. 2. Add “Pin Map” to section 4.1. 3. Modify “Ordering Information” in section 7.2. 4. Add “Package Information” to section 7.3.	4 5 20 21
JUL. 31, 2007	1.0	Modify the “DC Characteristics (T_A = 25℃)” in section 6.3.	18
JUL. 05, 2007	0.1	Preliminary Data Sheet.	21