

DATA SHEET



GPC11122A

128KB Sound Controller (OTP)

OCT. 14, 2010

Version 1.3

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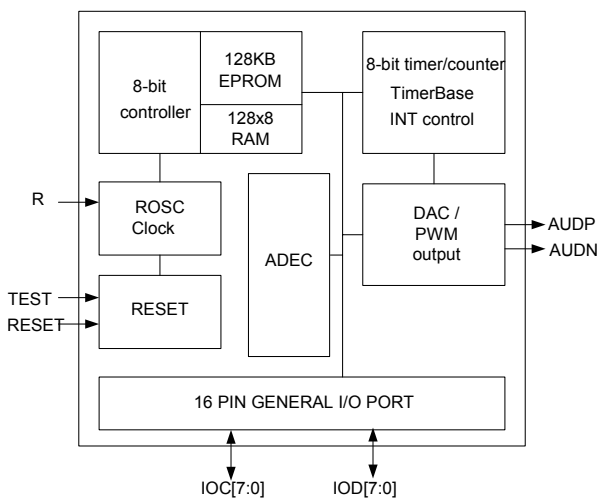
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128KB SOUND CONTROLLER(OTP)

1. GENERAL DESCRIPTION

The GPC11122A, a speech/wavetable synthesizer, equips an 8-bit CMOS microprocessor, and 128K-byte OTP EPROM, 128-byte working SRAM. Other primary features include two 8-bit Timer/Counters and can cascade to one 16-bit timer/counter, 16 Software Selectable I/Os, One 8-bit DAC and a pair of PWM output. It operates at a wide voltage range of 2.4V - 5.5V. Plus, a Clock Stop mode is built in for power savings. The unique power saving mode saves the RAM contents, but freezes the oscillator to stop executing other functions. The maximum CPU frequency can run up to 8MHz and the instruction cycle is two clock cycles (min.) ~ six clock cycles (max.). The GPC11122A loads, not only the latest technology, but also the full commitment and technical support of Generalplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- 128K bytes OTP EPROM
- 128-byte working SRAM
- Software-based audio processing
- Wide operating voltage: 2.4V - 3.6V @ 6.0MHz
3.6V - 5.5V @ 8.0MHz
- Supports ROSC only
- Max. CPU clock: 6.0MHz @ 3.0V, 8MHz @ 5.0V
- Standby mode (Clock Stop mode) for power savings.
Max. 5.0μA @ 5.0V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- 16 general I/Os
- Two 8-bit timer/counters and can cascade to one 16-bit timer/counter
- Six INT sources
- Key wake -up function
- IR function
- External feedback input
- Watch dog function
- One DAC and A pair of PWM output

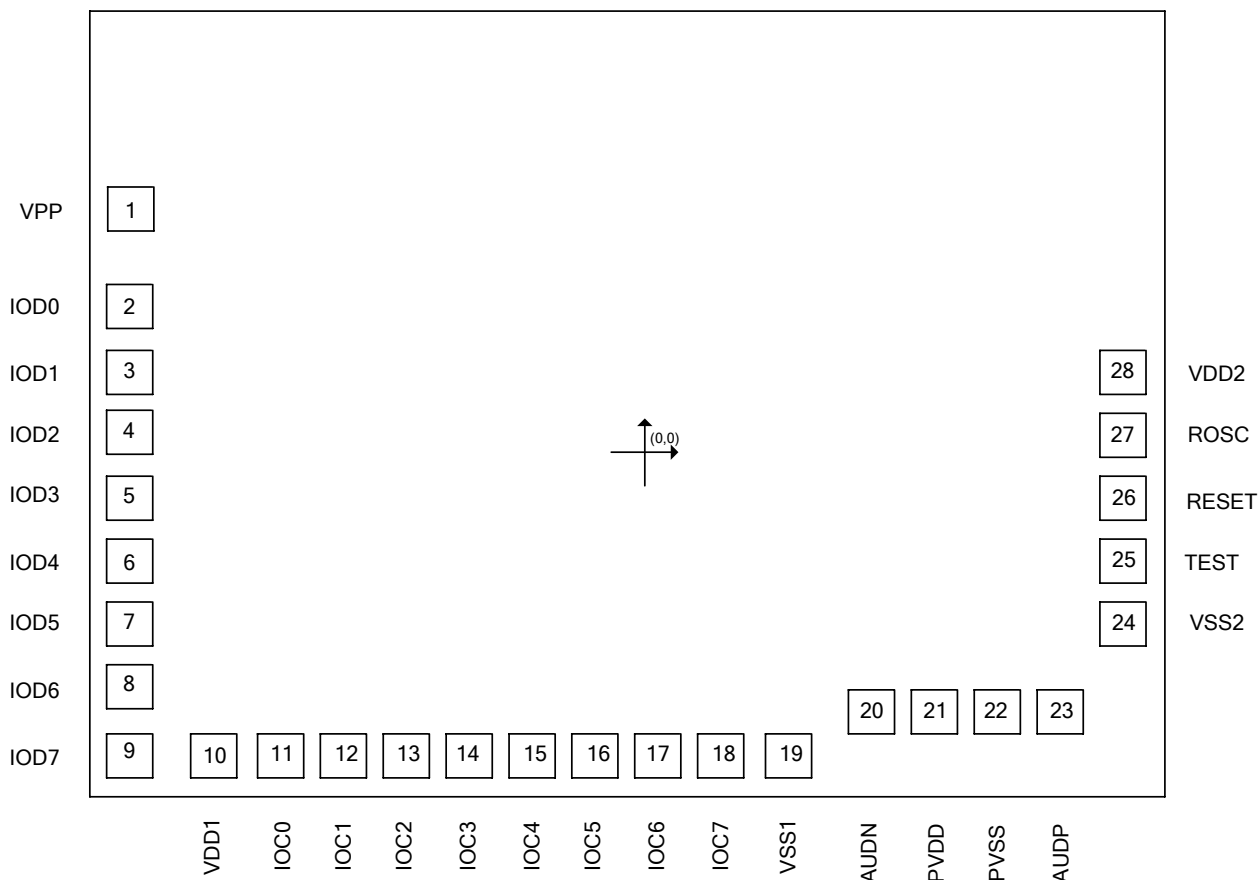
4. APPLICATION FIELD

- Intelligent education toys
Ex. Pattern to voice (animal, car, color, etc.)
Spelling (English or Chinese)
Math
- Advanced toy controller
- General speech synthesizer
- Industrial controller

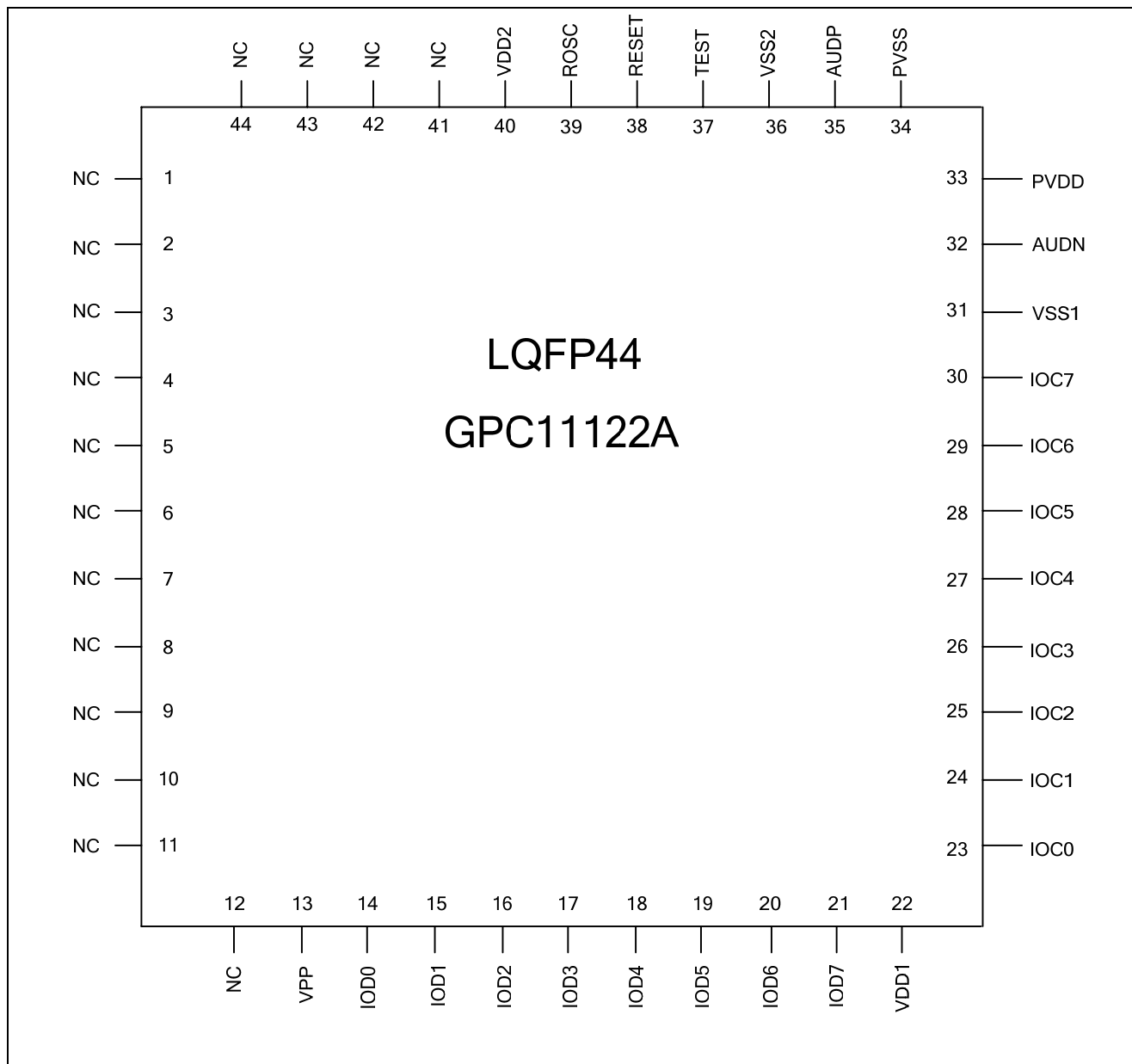
5. SIGNAL DESCRIPTIONS*

Mnemonic	PIN No	Type	Description
VDD1	10	I	Digital Power Pad.
VSS1	19	I	Digital Ground.
VDD2	28	I	Digital Power Pad.
VSS2	24	I	Digital Ground.
PVDD	21	I	PWM Power Pad.
VPP	1	I	High voltage input for EPROM programming use, keep it floating in normal run.
PVSS	22	I	PWM Ground.
ROSC	27	I	ROSC Resistor input. (Resistor must be connected to VDD)
RESET	26	I	RESET pin, Active low to reset whole system.
TEST	25	I	TEST MODE.
AUDP	23	O	Audio OUTPUT1.
AUDN	20	O	Audio OUTPUT2.
IOC0	11	I/O	Port C is a 8-bit bi-directional programmable Input / Output port with Pull-low. In input mode, Port C can be either Pure or Pull-low states. In output mode, Port C can be Buffer.
IOC1	12	I/O	
IOC2	13	I/O	
IOC3	14	I/O	
IOC4	15	I/O	
IOC5	16	I/O	
IOC6	17	I/O	
IOC7	18	I/O	
IOD0	2	I/O	Port D is a 8-bit bi-directional programmable Input / Output port with Pull-low. In input mode, Port D can be either Pure or Pull-low states. In output mode, Port D can be Buffer. (Key change, Wake up I/O) In EPROM serial programming mode, IOD4 is used as the serial clock, IOD6 as the serial data.
IOD1	3	I/O	
IOD2	4	I/O	
IOD3	5	I/O	
IOD4	6	I/O	
IOD5	7	I/O	
IOD6	8	I/O	
IOD7	9	I/O	

5.1. PAD Assignment



5.2. PIN Map



5.3. Generalplus COB28 Pin Map

	PVSS	PVDD	AUDN	VSS1	IOC7	IOC6	IOC5	
	22	21	20	19	18	17	16	15
AUDP	23							14
VSS2	24							13
TEST	25							12
RESET	26							11
ROSC	27							10
VDD2	28							9
	1	2	3	4	5	6	7	8
	VPP	IOD0	IOD1	IOD2	IOD3	IOD4	IOD5	IOD6
								IOC4
								IOC3
								IOC2
								IOC1
								IOC0
								VDD1
								IOD7

6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The microprocessor in GPC11122A is a high performance 8-bit processor equipped Accumulator, Program Counter, X and Y Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure). The maximum CPU speed of 8.0MHz is capable of bringing you the cleaner speech, pleasant music as well as achieving the best performance.

6.2. RAM Area

The total RAM size is 128-bytes (including Stack) starting from address \$0080 through \$00FF or mapping to \$0180 through \$01FF.

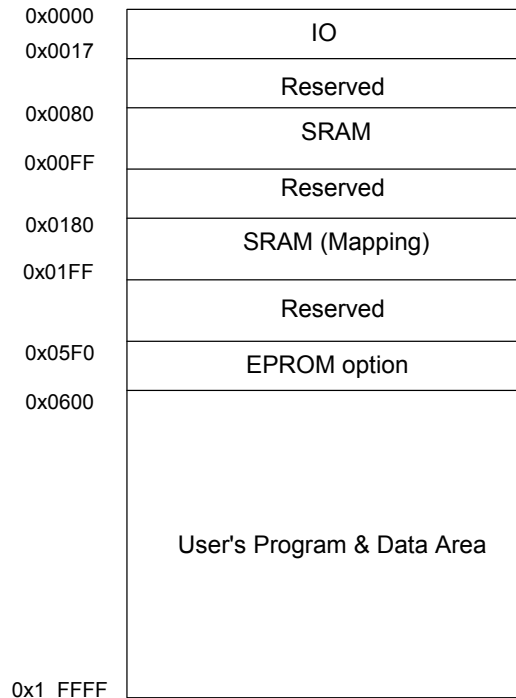
6.3. OTP EPROM Area

The GPC11122A provides a 128K-byte OTP EPROM that can be defined as the program area, audio data area, or both. To access OTP EPROM, users should program the BANK SELECT Register, choose bank, and access address to fetch data.

6.4. Power Saving Mode

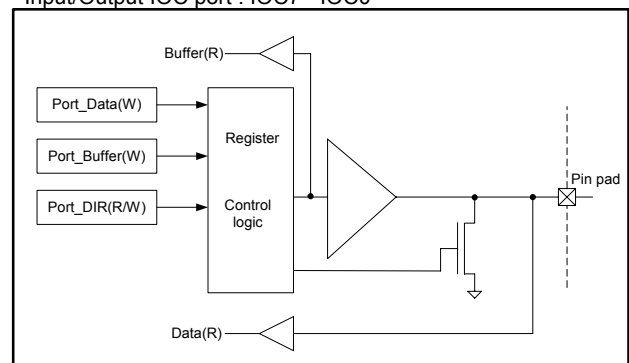
The GPC11122A includes a power saving mode (Standby mode) for those applications that require very low standby current. To enter standby mode, the Wake-Up Register must be enabled and then stop the CPU clock by writing the STOP CLOCK Register to enter standby mode. In such mode, RAM and I/Os will remain in their previous states until being awoken. Port IOD7-0 is the only wake-up source in the GPC11122A. After the GPC11122A is awoken, the internal CPU will go to the RESET State ($T_w \geq 64 \times T_1$) and continue to execute program from Reset Vector. Wakeup Reset will not affect RAM nor I/Os.

6.5. Map of Memory and I/Os

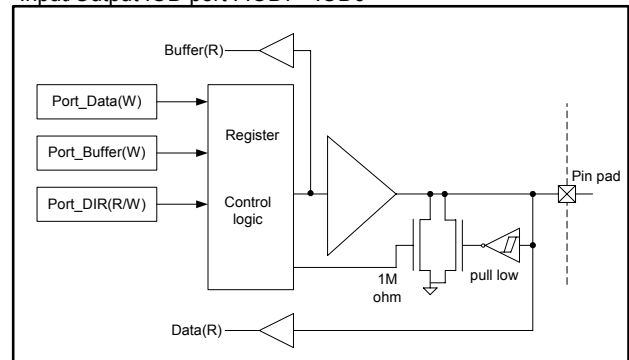


6.6. I/O Port Configuration*

Input/Output IOC port : IOC7 - IOC0



Input/Output IOD port : IOD7 - IOD0



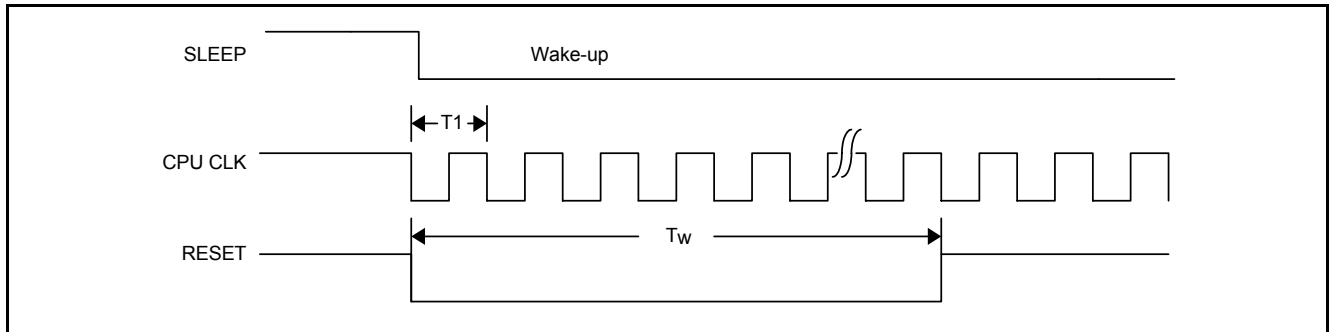


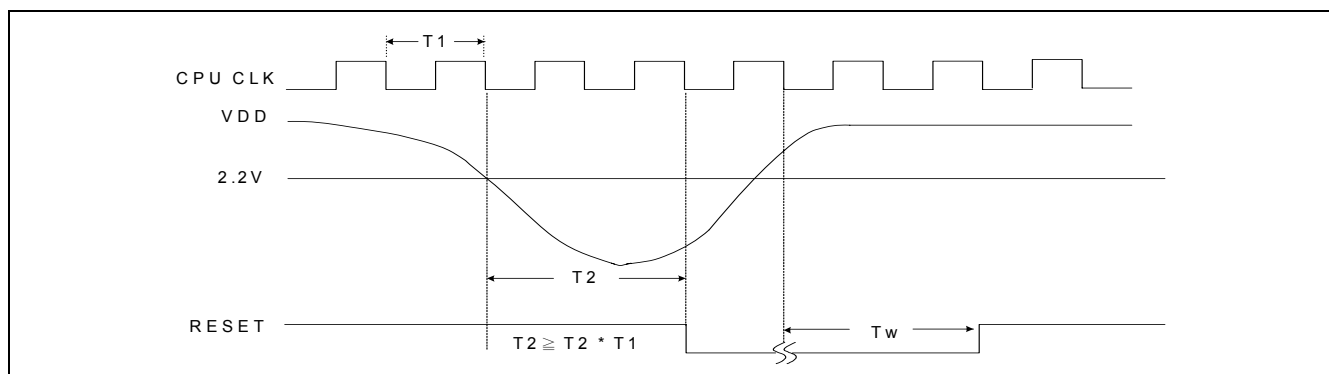
FIG. 1

$$T1 = 1 / (F_{CPU}), Tw \geq 64 \times T1$$

6.7. Low Voltage Reset

The GPC11122A has a Low Voltage Reset (LVR) function. In general, the CPU becomes unstable and malfunctions when the power voltage drops below certain operating voltage. With the

unique design of Low Voltage Reset in GPC11122A, it is able to reset all functions to the initial operational (stable) state if the VDD power-supply voltage drops below 2.2V.



(The LVR function is the same as Power ON Reset or External Reset.)

6.8. Timer/Counter

The GPC11122A has two 8-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer, but TMB can be used as a timer or a counter. In the timer mode, TMA and TMB are re-loaded up-counters. When timer rollovers from \$FF to \$00, the carry (overflow) signal will make the user's preset value to be loaded into timer automatically and up-count again. At the same

time, the carry signal will generate an INT signal if the corresponding bit is enabled in the INT ENABLE Register. Suppose TMB is specified as a counter, users can reset it by writing #0 into the counter. After the counter has been activated, the value in the counter can also be read at the same time. The read instruction will not affect the value of the counter nor reset it.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	8-BIT TIMER	CPU CLOCK (T) or T/8, T/64, TMB overflow
TMB	8-BIT TIMER	T, T/65536, EXTCLK, 0, 1

6.9. Speech and Melody

In speech synthesis, the GPC11122A can use NMI for accurate sampling frequency. The user can store the speech data in ROM and play it back with realistic sound quality. Several algorithms

are recommended for high fidelity and compression of sound: PCM, LOG PCM, ADPCM and SACMA34.

6.10. EPROM Option

\$5F0[0]: Watchdog enable/disable.

'1': disable watchdog timer.

'0': enable watchdog timer.

\$5F0[1]: PWM/DAC Select.

'1': Software DAC/Software PWM.

'0': PWM only.

※GPC100xxB series must set '0'.

\$5F8[7]: Security option

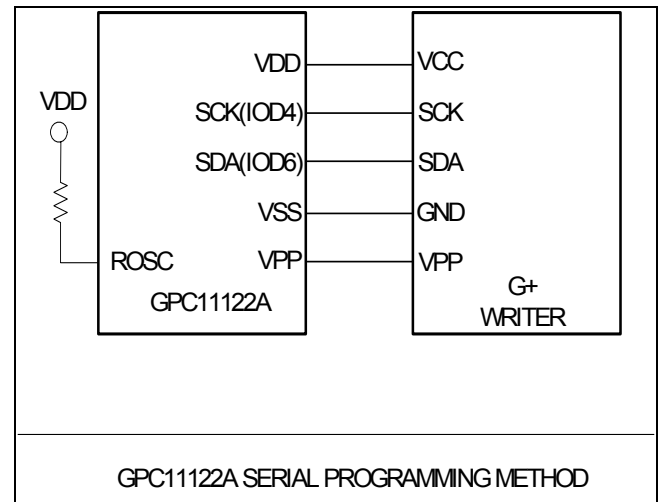
'1': security disable.

'0': security enable.

\$5F6, \$5F7 for identifying use

All the above option bits can be read by serial interface even security bit is enabled.

6.11. OTP Programming Circuit



Note1: It has to pull high a resistor on ROSC when programming.

Note2: Don't connect any component with IOD4 and IOD6 when programming.

Note3: Make sure the power source of Generalplus Writer is 18Volts.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to $V_+ + 0.5V$
Operating Temperature	T_A	0°C to +60°C
Storage Temperature	T_{STO}	-50°C to +150°C

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. AC Characteristics ($T_A = 25^\circ\text{C}$)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC2}	-	4.0	6.0	MHz	VDD = 2.4V - 3.6V, for 2-battery
		-	6.0	8.0	MHz	VDD = 3.6V - 5.5V, for 3-battery

7.3. DC Characteristics (VDD = 3.0V, $T_A = 25^\circ\text{C}$)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	5.5	V	-
Operating Current	I_{OP}	-	2.5	-	mA	$F_{CPU} = 4.0\text{MHz}$ @ 3.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 3.0V
Audio Output Current	I_{AUD}	-	1.0	-	mA	VDD = 3.0V
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
PWM Output Current	I_{OH}	-	150	-	mA	VDD = 3.0V, $V_{OH} = 2.0V$
	I_{OL}	-	-160	-		VDD = 3.0V, $V_{OL} = 1.0V$
Output Source Current	I_{OH}	-2	-	-	mA	VDD = 3.0V, $V_{OH} = 2.0V$
Output Sink Current	I_{OL}	4	-	-	mA	VDD = 3.0V, $V_{OL} = 0.8V$
Input Resistor (IOD)	R_{IN}	-	1600	-	Kohm	Pull Low, VDD = 3.0V, $V_{IN} = VDD$
Input Resistor (IOC)	R_{IN}	-	180	-	Kohm	Pull Low, VDD = 3.0V, $V_{IN} = VDD$

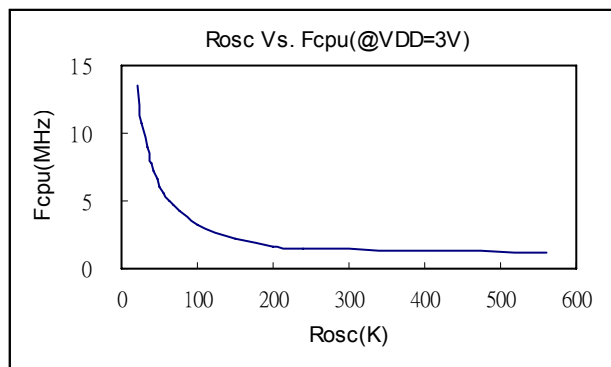
7.4. DC Characteristics (VDD = 5.0V, $T_A = 25^\circ\text{C}$)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	5.5	V	-
Operating Current	I_{OP}	-	6.0	-	mA	$F_{CPU} = 6.0\text{MHz}$ @ 5.0V, no load
Standby Current	I_{STBY}	-	-	5.0	μA	VDD = 5.0V
Audio Output Current	I_{AUD}	-	2.0	-	mA	VDD = 5.0V
Input High Level	V_{IH}	3.0	-	-	V	VDD = 5.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 5.0V
PWM Output Current	I_{OH}	-	180	-	mA	VDD = 5.0V, $V_{OH} = 4.0V$
	I_{OL}	-	-250	-		VDD = 5.0V, $V_{OL} = 1.0V$
Output Source Current	I_{OH}	-4	-	-	mA	VDD = 5.0V, $V_{OH} = 3.3V$
Output Sink Current	I_{OL}	8	-	-	mA	VDD = 5.0V, $V_{OL} = 0.8V$

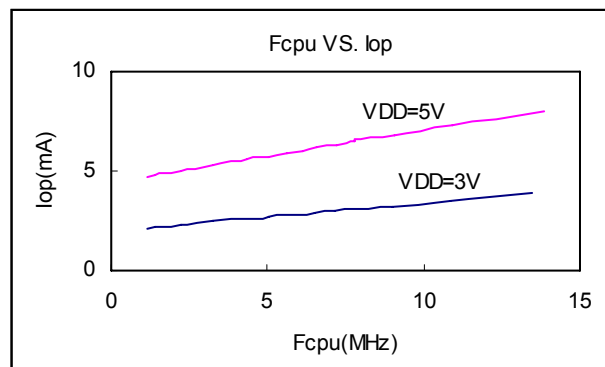
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Resistor (IOD)	R_{IN}	-	850	-	Kohm	Pull Low, VDD = 5.0V, $V_{IN} = VDD$
Input Resistor (IOC)	R_{IN}	-	88	-	Kohm	Pull Low, VDD = 5.0V, $V_{IN} = VDD$

7.5. The Relationship between the R_{OSC} and the F_{CPU}

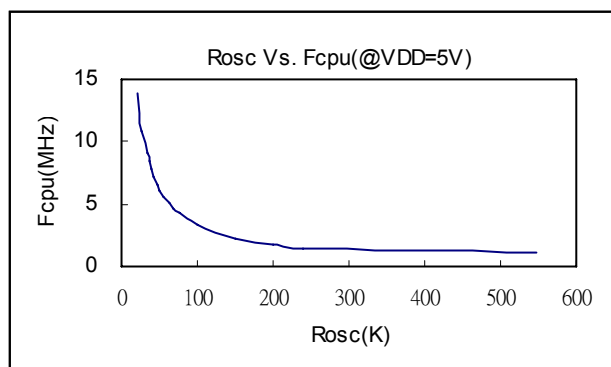
7.5.1. VDD = 3.0V, $T_A = 25^\circ C$



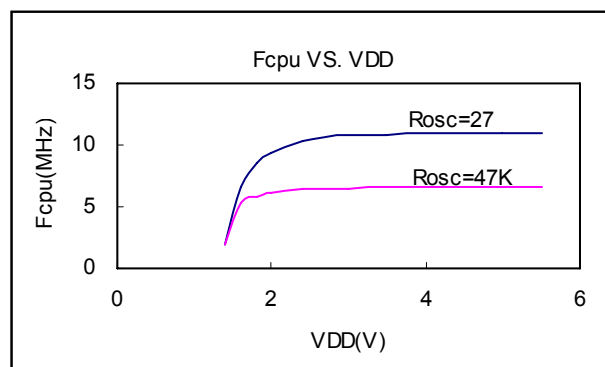
7.5.3. Operating current vs. frequency vs. VDD



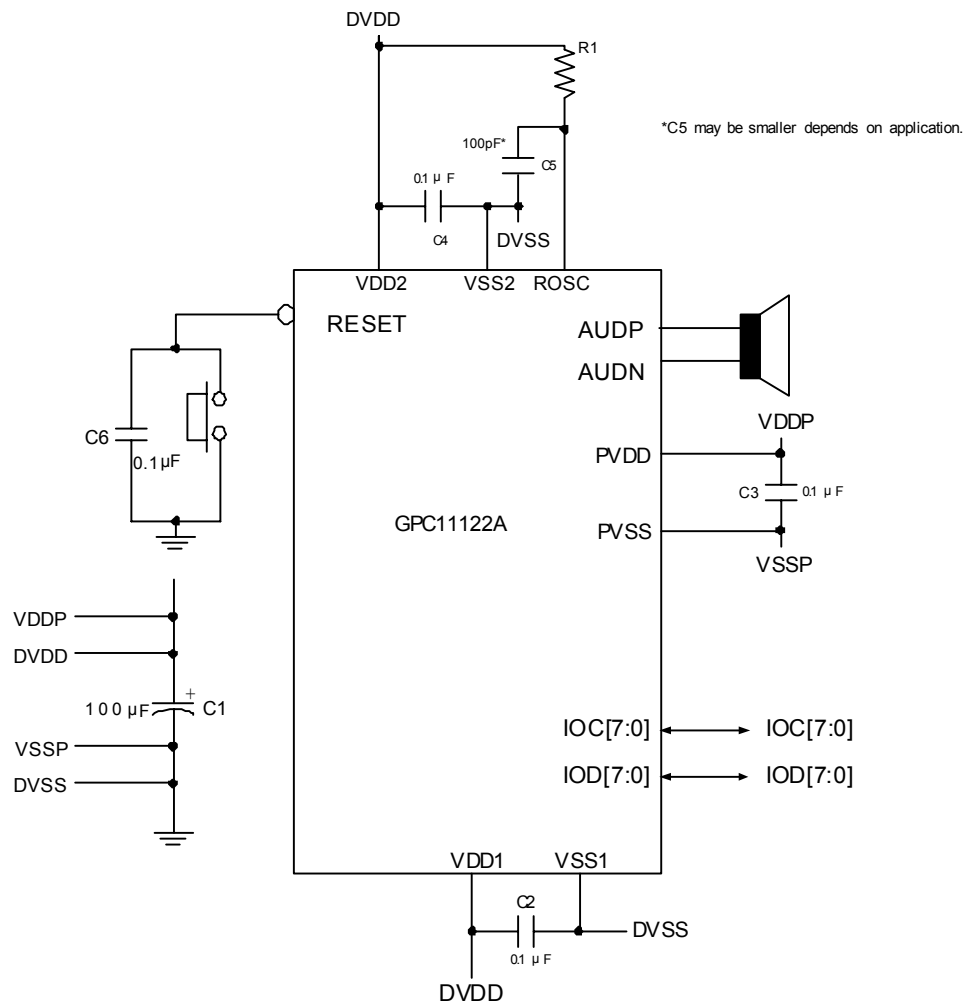
7.5.2. VDD = 5.0V, $T_A = 25^\circ C$



7.5.4. Frequency vs. VDD

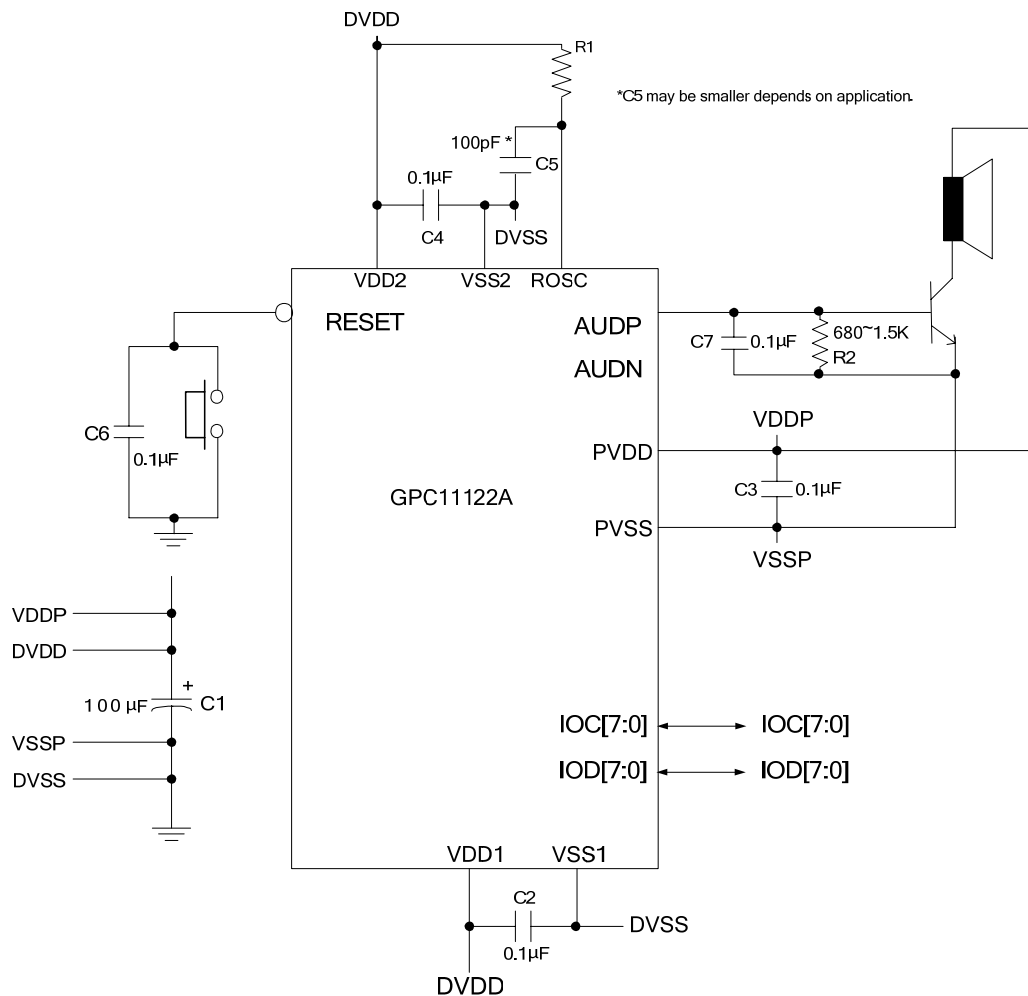


8.APPLICATION CIRCUITS



PCB Layout Guidelines:

- 1.VDD1, VDD2, PVDD must be connected to power input port directly, not to be the branch of each other.
- 2.VSS1, VSS2, PVSS must be connected to ground input port directly, not to be the branch of each other.
- 3.R1 and C5 should be as close as possible to ROOSC pin.
- 4.C2 should be as close as possible to VDD1/VSS1 pin.
- 5.C3 should be as close as possible to PVDD/PVSS pin.
- 6.C4 should be as close as possible to VDD2/VSS2 pin.



PCB Layout Guidelines:

- 1.VDD1, VDD2, PVDD must be connected to power input port directly, not to be the branch of each other.
- 2.VSS1, VSS2, PVSS must be connected to ground input port directly, not to be the branch of each other.
- 3.R1 and C5 should be as close as possible to ROSC pin.
- 4.C2 should be as close as possible to VDD1/VSS1 pin.
- 5.C3 should be as close as possible to PVDD/PVSS pin.
- 6.C4 should be as close as possible to VDD2/VSS2 pin.

9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

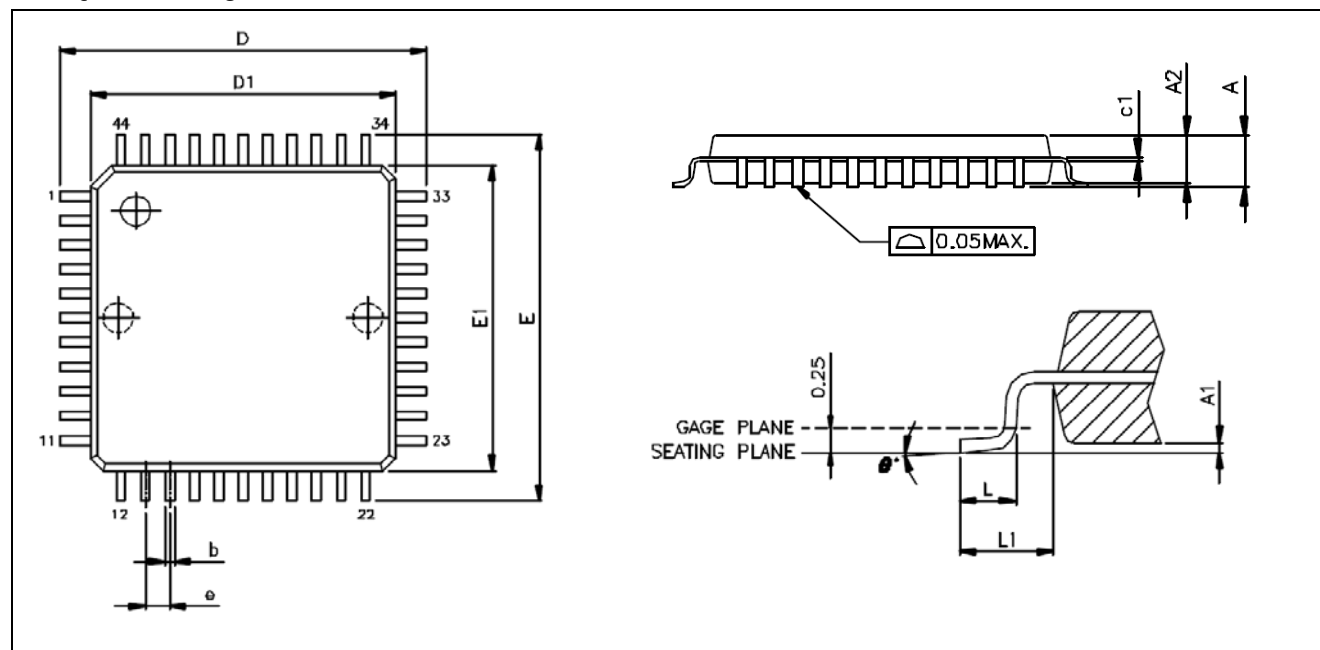
Product Number	Package Type
GPC11122A - NnnV - C	Chip form
GPC11122A - NnnV - QL01x	Halogen Free Package

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

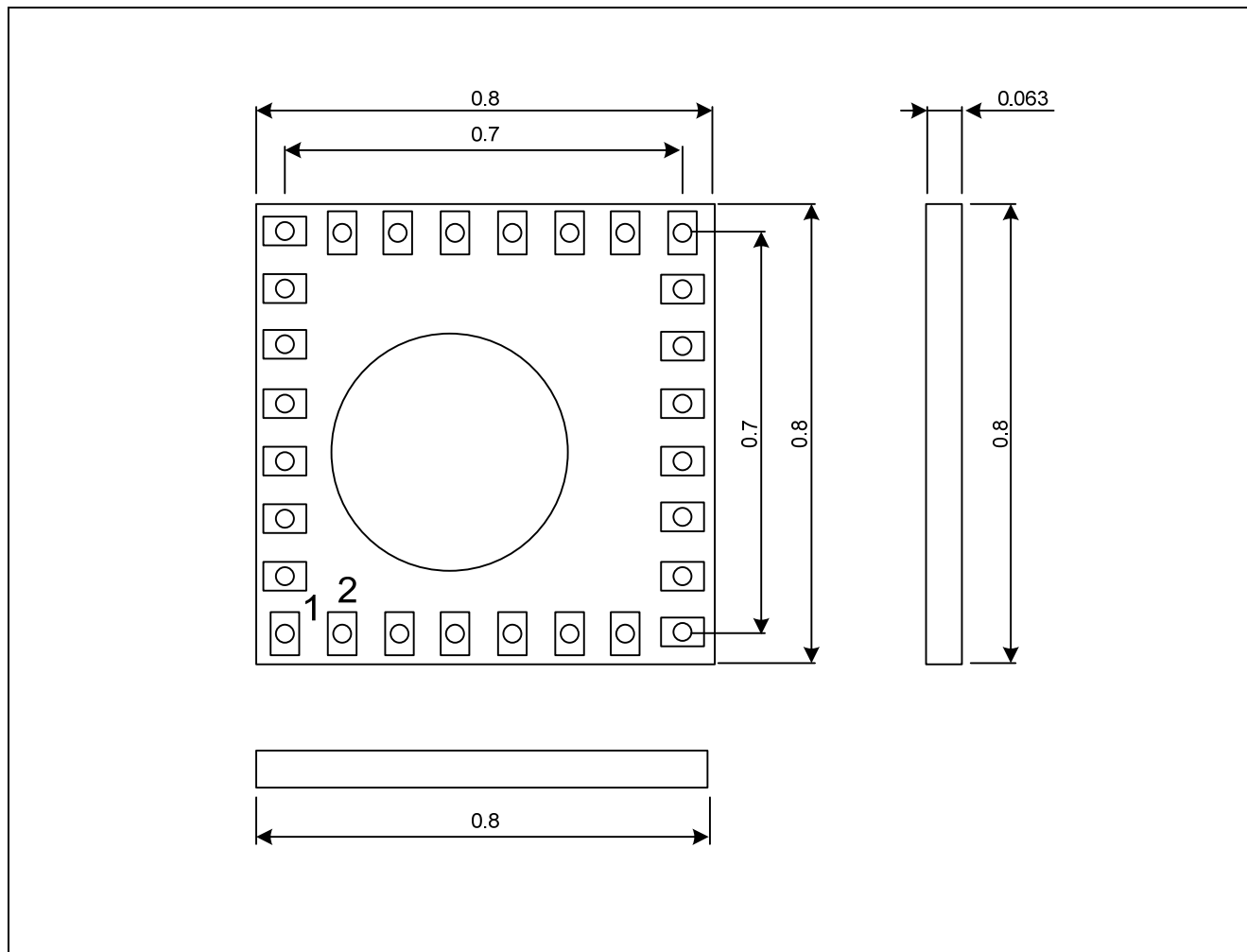
Note3: Package form number (x = 1 - 9, serial number).

9.2. LQFP44 Package Information



Symbol	Dimension in Millimeter		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
c1	0.09	-	0.16
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.80 BSC		
b	0.30	0.37	0.45
L	0.45	0.60	0.75
L1	1.00 REF		
θ°	0°	3.5°	7°

9.3. Generalplus 28 Pins COB Information



10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
OCT. 14, 2010	1.3	Add 6.11 OTP Programming Guide.	10
FEB. 13, 2008	1.2	1. Add "PIN Map" in section 5.2	6
		2. Add "Generalplus COB28 PIN Map" in section 5.3.	7
		3. Modify "Ordering Information" in section 9.1.	15
		4. Add "LQFP44 package information" in section 9.2.	15
MAR. 07, 2006	1.1	1. Modify the "DC Characteristics (VDD = 3.0V, T _A = 25°C)" in section 7.3.	8
		2. Modify the "DC Characteristics (VDD = 5.0V, T _A = 25°C)" in section 7.4.	8
		3. Modify the "PAD No." in section 9.1.	12
		4. Remove the section "9.3. Package information" and "9.4. Package dimension".	13, 14
		5. Add the section "9.3. Generalplus 28 pins COB information".	13
DEC. 02, 2005	1.0	Original	16