DATA SHEET

GPC11A24A1

Sound Controller with 1MB ROM

AUG. 08, 2008

Version 1.0

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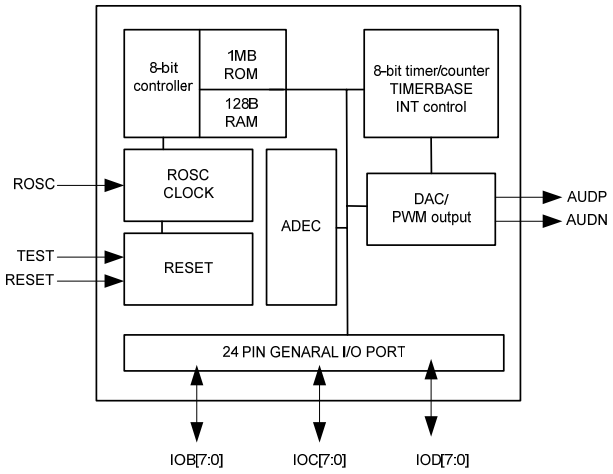
SOUND CONTROLLER WITH 1MB ROM

1. GENERAL DESCRIPTION

The GPC11A24A1, a speech/wavetable synthesizer, equips an 8-bit CMOS microprocessor, and 1M-byte Working ROM, 128-byte working SRAM. Other primary features include two 8-bit Timer/Counters and can cascade to one 16-bit timer/counter, 24 Software Selectable I/Os, One 8-bit DAC and a pair of PWM output. It operates at a wide voltage range of 2.4V - 5.5V. Plus, a Clock Stop mode is built in for power savings. The unique power saving mode saves the RAM contents, but freezes the oscillator to stop executing other functions. The maximum CPU frequency can run up to 8MHz and the instruction cycle is two clock cycles (min.) ~ six clock cycles (max.). The GPC11A24A1 loads, not only the latest technology, but also the full commitment and technical support of Generalplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- 1M bytes ROM
- 128-byte working SRAM
- Software-based audio processing
- Wide operating voltage: 2.4V - 5.5V @ 6.0MHz
  3.6V - 5.5V @ 8.0MHz
- Supports ROSC only
- Max. CPU clock: 6.0MHz @ 3.0V, 8MHz @ 5.0V
- Standby mode (Clock Stop mode) for power savings
  Max. 2.0μA @ 5.0V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- 24 general I/Os
- Low Voltage Reset (LVR) function
- Two 8-bit timer/counters and can cascade to one 16-bit timer/counter
- Six INT sources
- Key wake -up function
- IR function
- External feedback input
- Watch dog function
- One DAC and A pair of PWM output

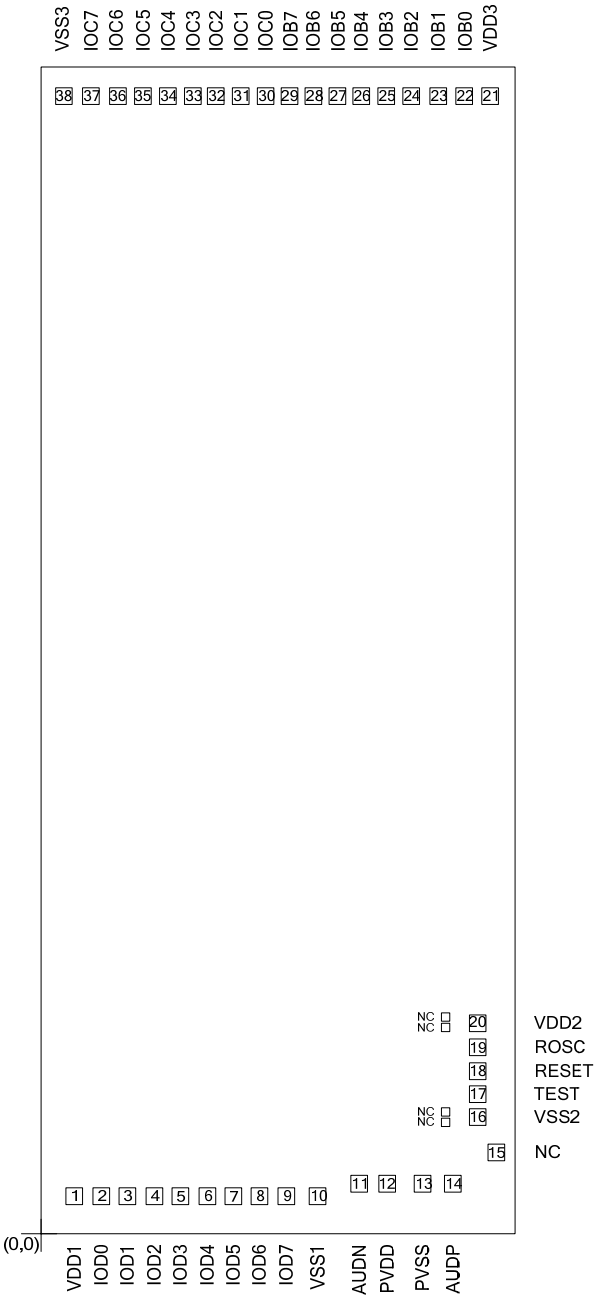
4. APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- Advanced toy controller
- General speech synthesizer
- Industrial controller

5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No	Type	Description
VDD1	1	I	Digital Power Pad
VSS1	10	I	Digital Ground
VDD2	20	I	Digital Power Pad
VSS2	16	I	Digital Ground
VDD3	21	I	Digital Power Pad
VSS3	38	I	Digital Ground
PVDD	12	I	PWM Power Pad
PVSS	13	I	PWM Ground
ROSC	19	I	ROSC Resistor input (Resistor must be connected to VDD)
RESET	18	I	Reset pin, active low to reset whole system.
TEST	17	I	Test pin, NC
AUDP	14	O	Audio OUTPUT1
AUDN	11	O	Audio OUTPUT2
NC	15	-	NC
IOB0	22	I/O	Nibble-controlled programmable I/O pins.
IOB1	23	I/O	In input mode, port B can be either pure or pull-low states. In output mode, port B can
IOB2	24	I/O	be buffer
IOB3	25	I/O	
IOB4	26	I/O	
IOB5	27	I/O	
IOB6	28	I/O	
IOB7	29	I/O	
IOC0	30	I/O	Nibble-controlled programmable I/O pins.
IOC1	31	I/O	In input mode, port C can be either pure or pull-low states. In output mode, port C can
IOC2	32	I/O	be buffer
IOC3	33	I/O	
IOC4	34	I/O	
IOC5	35	I/O	
IOC6	36	I/O	
IOC7	37	I/O	
IOD0	2	I/O	Bit-controlled programmable I/O pins.
IOD1	3	I/O	In input mode, port D can be either pure or pull-low states.
IOD2	4	I/O	In output mode, port D can be buffer.
IOD3	5	I/O	Port D are the key wakeup I/O pins.
IOD4	6	I/O	IOD4: feedback input of clock generator
IOD5	7	I/O	IOD5: feedback output of clock generator
IOD6	8	I/O	IOD6 : external interrupt
IOD7	9	I/O	IOD7: IR transmitter

5.1. PAD Assignment



The IC substrate should be connected to VSS

Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The microprocessor in GPC11A24A1 is a high performance 8-bit processor equipped Accumulator, Program Counter, X and Y Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure). The maximum CPU speed of 8.0MHz is capable of bringing you the cleaner speech, pleasant music as well as achieving the best performance.

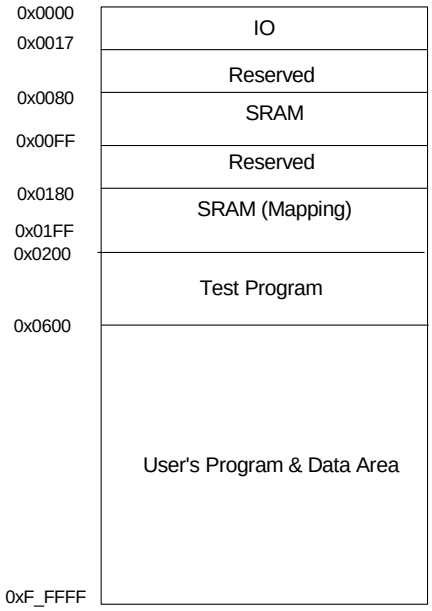
6.2. RAM Area

The total RAM size is 128-bytes (including Stack) starting from address $0080 through $00FF or mapping to $0180 through $01FF.

6.3. ROM Area

The GPC11A24A1 provides a 1M-byte ROM that can be defined as the program area, audio data area, or both. To access ROM, users should program the BANK SELECT Register, choose bank, and access address to fetch data.

6.4. Map of Memory and I/Os

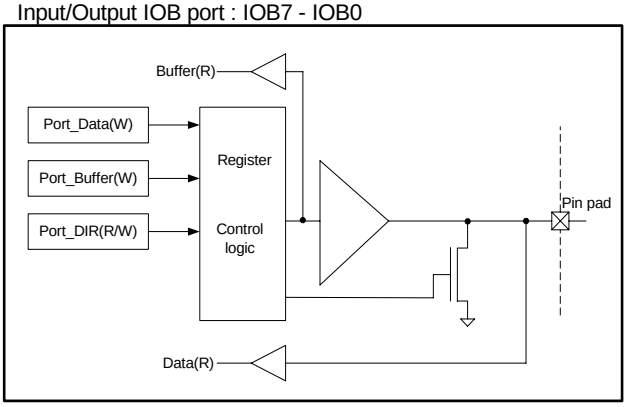


6.5. I/O Port

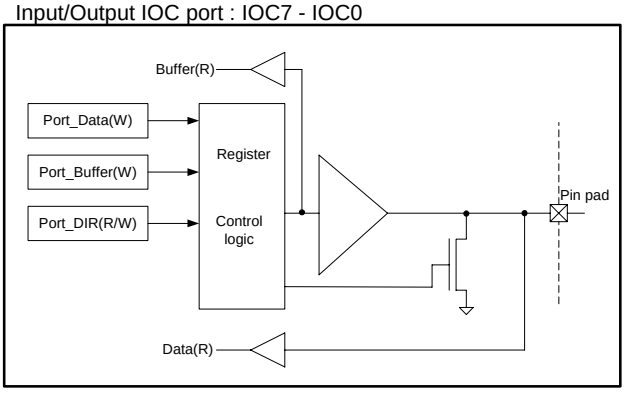
There are 24 IOs (IODB7-0, IOC7-0 and IOD7-0) in the GPC11A24A1. IOB7-0 and IOC7-0 are nibble-controlled IOs, but IOD7-0 are bit-controlled IOs. They can be programmed as input (pure input or pull-low) or output buffer. As pull-low input IOD7-0 keep a less impedance to get good noise immunity. While pressing the key (IOD7-0 to VDD), a large impedance remained to save the DC power. IOD4, IOD5 can be programmed as a RC clock generator by adding external resistor and capacitor. IOD6 can be programmed as a external interrupt source. IOD7 can be programmed as an IR transmitter.

IO port configuration:

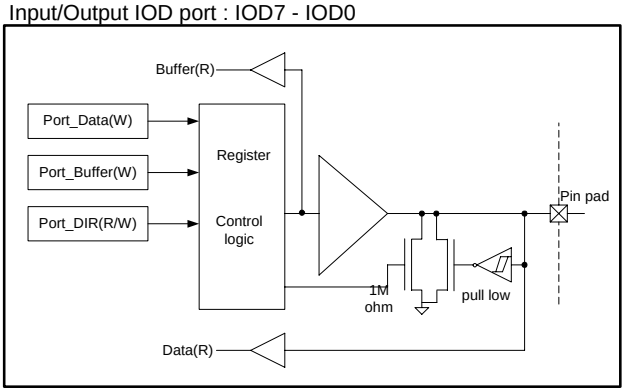
Input/Output IOB port : IOB7 - IOB0



Input/Output IOC port : IOC7 - IOC0



Input/Output IOD port : IOD7 - IOD0



6.6. Power Saving Mode

The GPC11A24A1 includes a power saving mode (Standby mode) for those applications that require very low standby current. To enter standby mode, the Wake-Up Register must be enabled and then stop the CPU clock by writing the STOP CLOCK Register to enter standby mode. In such mode, RAM and I/Os will remain in their previous states until being awaken. Port IOD7-0 is the only wake-up source in the GPC11A24A1. After the GPC11A24A1 is awaken, the internal CPU will go to the RESET State (Tw ≧ 64 x T1) and continue to execute program. Wakeup Reset will not affect RAM nor I/Os.

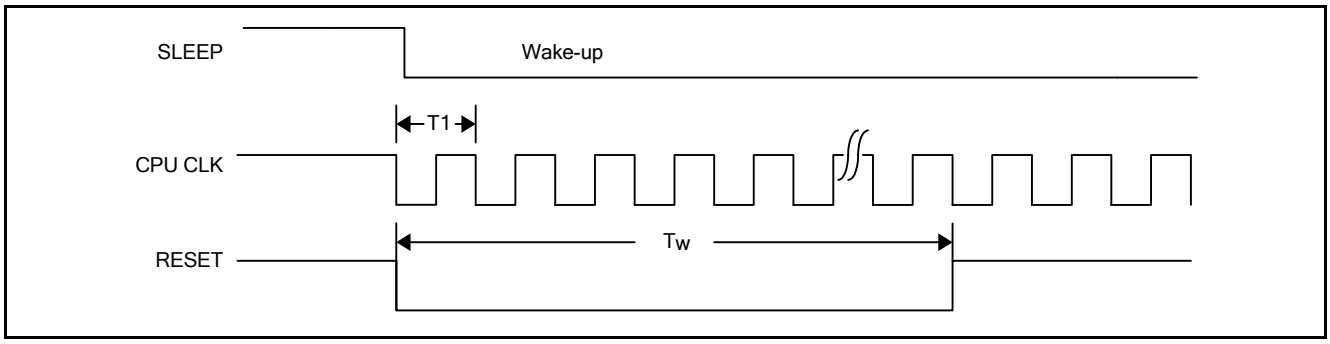
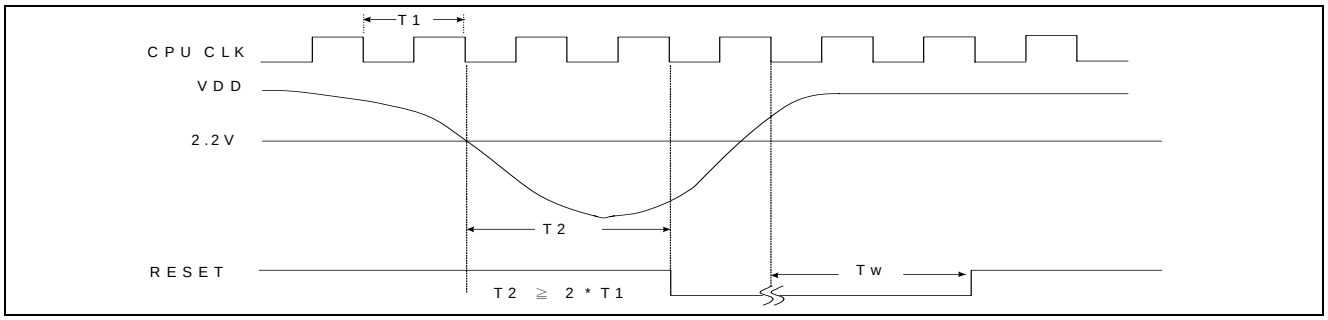


FIG. 1

$T1 = 1 / (F_{CPU})$, $Tw \geqq 64 \times T1$

6.7. Low Voltage Reset

The GPC11A24A1 has a Low Voltage Reset (LVR) function. In general, the CPU becomes unstable and malfunctions when the power voltage drops below certain operating voltage. With the unique design of Low Voltage Reset in GPC11A24A1, it is able to reset all functions to the initial operational (stable) state if the VDD power-supply voltage drops below 2.2V.



(The LVR function is the same as Power ON Reset or External Reset.)

6.9. Timer/Counter

The GPC11A24A1 has two 8-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer, but TMB can be used as a timer or a counter. In the timer mode, TMA and TMB are re-loaded up-counters. When timer rollovers from $FF to $00, the carry (overflow) signal will make the user's preset value to be loaded into timer automatically and up-count again. At the same time, the carry signal will generate an INT signal if the corresponding bit is enabled in the INT ENABLE Register. Suppose TMB is specified as a counter, users can reset it by loading #0 into the counter. After the counter has been activated, the value in the counter can also be read at the same time. The read instruction will not affect the value of the counter nor reset it.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	8-BIT TIMER	CPU CLOCK (T) or T/8, T/64, TMB overflow
TMB	8-BIT TIMER	T, T/65536, EXTCLK, 0, 1

6.10. Speech and Melody

In speech synthesis, the GPC11A24A1 can use NMI for accurate sampling frequency. The user can store the speech data in ROM and play it back with realistic sound quality. Several algorithms are recommended for high fidelity and compression of sound: PCM, LOG PCM, ADPCM and SACMA3400.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC}	-	-	6.0	MHz	VDD = 2.4V - 3.6V, for 2-battery
		-	-	8.0	MHz	VDD = 3.6V - 5.5V, for 3-battery

7.3. DC Characteristics (VDD = 5.0V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	-
Operating Current	I_{OP}	-	5.0	-	mA	F_{CPU} = 6.0MHz@ 5.0V (no load)
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 5.0V
Audio Output Current	I_{AUD}	-	5.0	-	mA	VDD = 5.0V
Input High Level	V_{IH}	4.0	-	-	V	VDD = 5.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 5.0V
Output Source Current (IOB,IOC, IOD)	I_{OH}	-	-9	-	mA	VDD = 5.0V, V_{OH} = 4V
Output Sink Current (IOB,IOC, IOD)	I_{OL}	-	20	-	mA	VDD = 5.0V, V_{OL} = 1V
PWM Output Current	I_{OH}	-	-170	-	mA	VDD = 5.0V, V_{OH} = 4.0V
	I_{OL}	-	208	-	mA	VDD = 5.0V, V_{OL} = 1.0V
Input Resistor (IOB,IOC)	R_{IN}	-	85	-	KΩ	VDD = 5.0V, V_{IN} = VDD
Input Resistor (IOD)	R_{IN}	-	85	-	KΩ	VDD = 5.0V, V_{IN} = 0V
Input Resistor (IOD)	R_{IN}	-	770	-	KΩ	VDD = 5.0V, V_{IN} = VDD

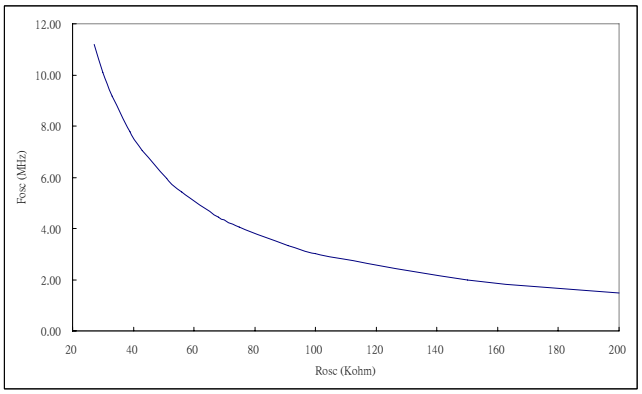
7.4. DC Characteristics (VDD = 3.0V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test condition
		Min	Typ	Max		
Operating Voltage	VDD	2.4	-	3.6	V	-
Operating Current	I_{OP}	-	2.0	-	mA	F_{CPU} = 6.0MHz @ 3.0V (no load)
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 3.0V
Audio Output Current	I_{AUD}	-	2.6	-	mA	VDD = 3.0V
Input High Level	V_{IH}	2.4	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output Source Current (IOB,IOC, IOD)	I_{OH}	-	-4	-	mA	VDD = 3.0V, V_{OH} = 2.4V

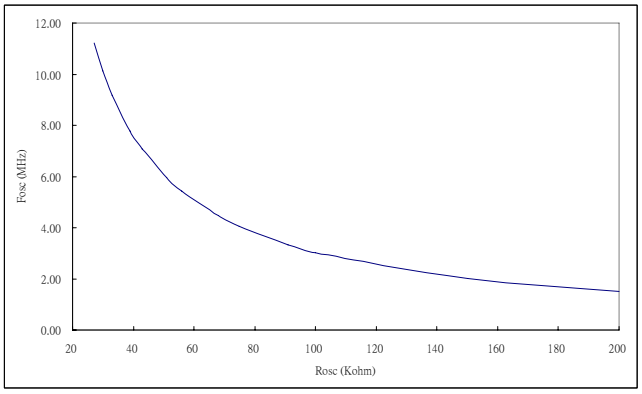
Characteristics	Symbol	Limit			Unit	Test condition
		Min	Typ	Max		
Output Sink Current (IOB,IOC, IOD)	I_{OL}	-	10	-	mA	VDD = 3.0V, V_{OL} = 0.6V
PWM Output Current	I_{OH}	-	-86	-	mA	VDD = 3.0V, V_{OH} = 2.4V
	I_{OL}	-	116	-	mA	VDD = 3.0V, V_{OL} = 0.6V
Input Resistor (IOB,IOC)	R_{IN}	-	170	-	KΩ	VDD = 3.0V, V_{IN} = VDD
Input Resistor (IOD)	R_{IN}	-	170	-	KΩ	VDD = 3.0V, V_{IN} = 0V
Input Resistor (IOD)	R_{IN}	-	1580	-	KΩ	VDD = 3.0V, V_{IN} = VDD

7.5. The Relationship between the R_{OSC} and the F_{CPU}

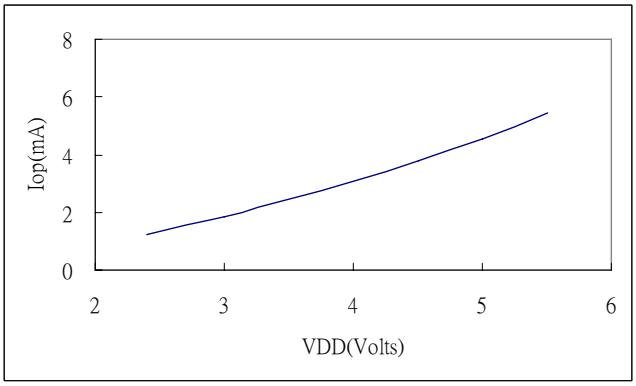
7.5.1. VDD = 3.0V, T_A = 25℃



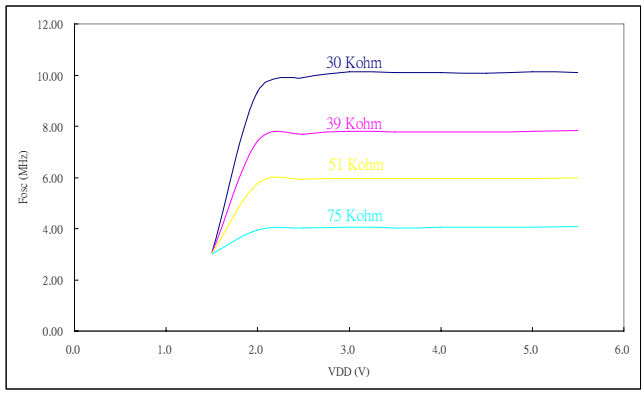
7.5.2. VDD = 4.5V, T_A = 25℃



7.5.3. Operating current vs. VDD @ 6MHz

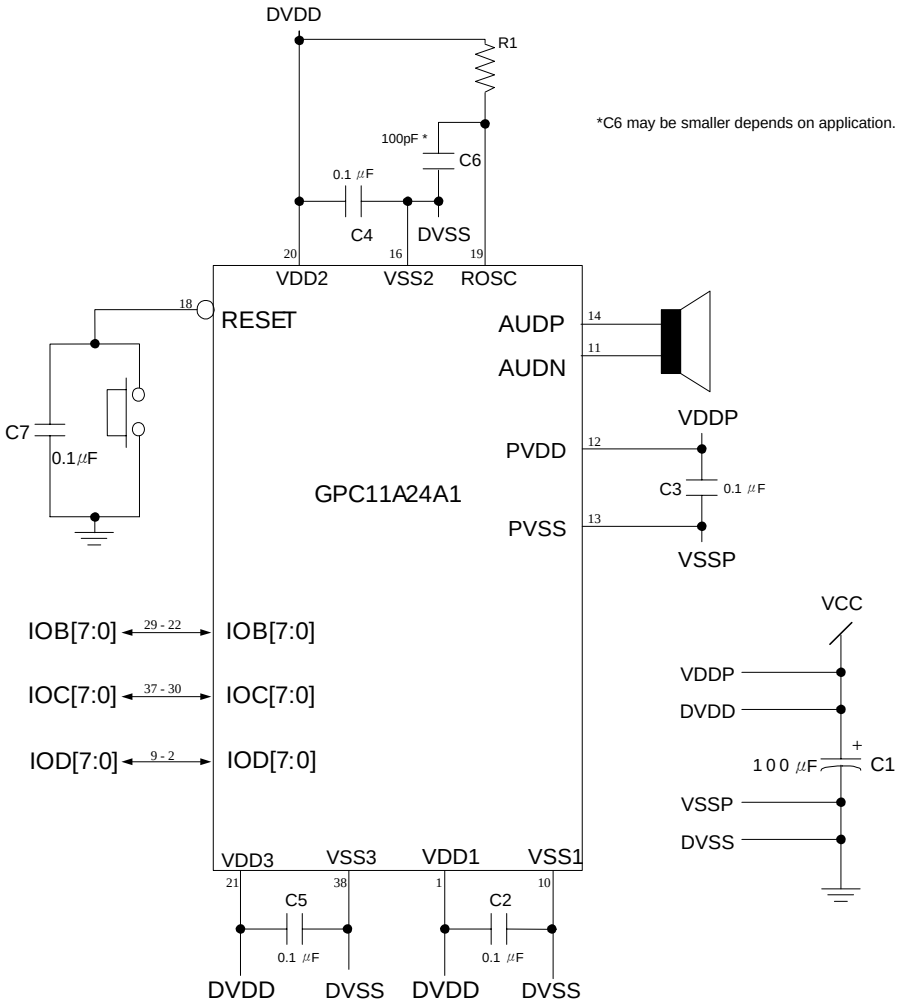


7.5.4. Frequency vs. VDD



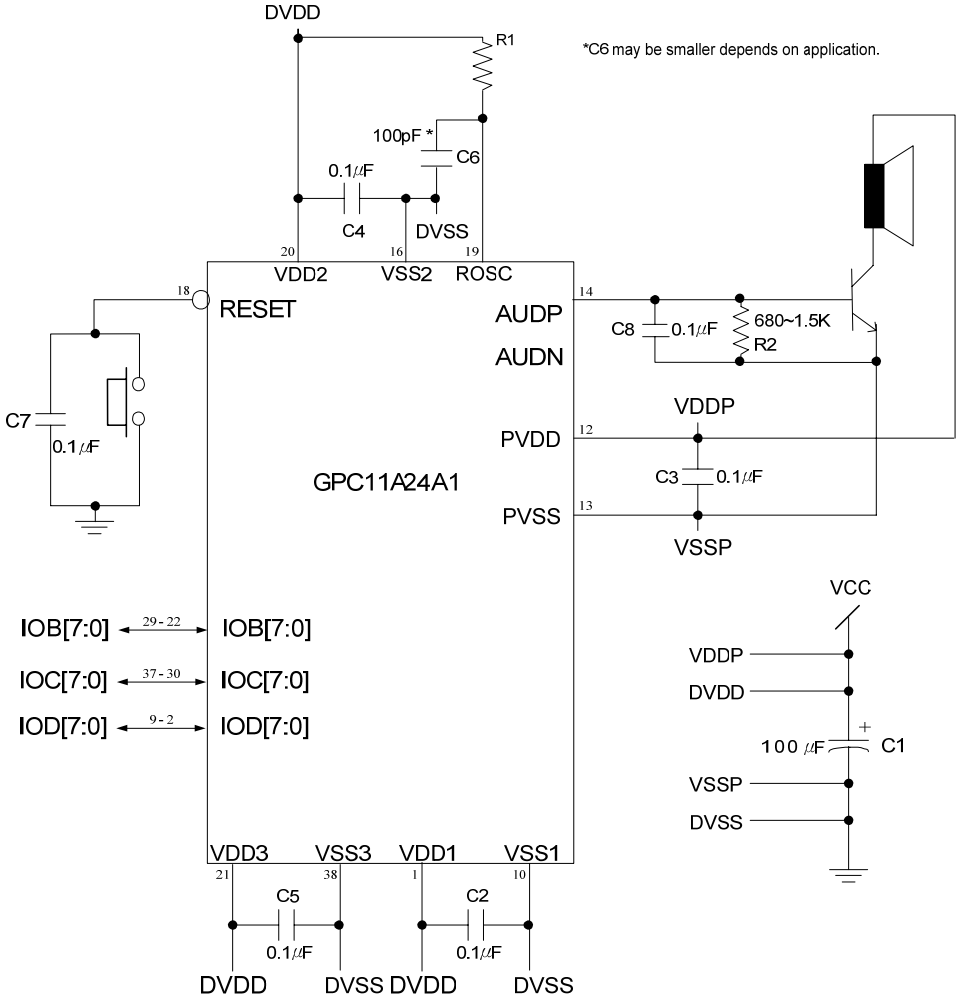
8. APPLICATION CIRCUITS

8.1. PWM Output



PCB Layout Guidelines :
1.VDD1, VDD2, VDD3, PVDD must be connected to power input port directly, not to be the branch of each other.
2.VSS1, VSS2, VSS3, PVSS must be connected to ground input port directly, not to be the branch of each other.
3.R1 and C6 should be as close as possible to ROSC pin.
4.C2 should be as close as possible to VDD1/VSS1 pin.
5.C3 should be as close as possible to PVDD/PVSS pin.
6.C4 should be as close as possible to VDD2/VSS2 pin.
7.C5 should be as close as possible to VDD3/VSS3 pin.

8.2. DAC Output



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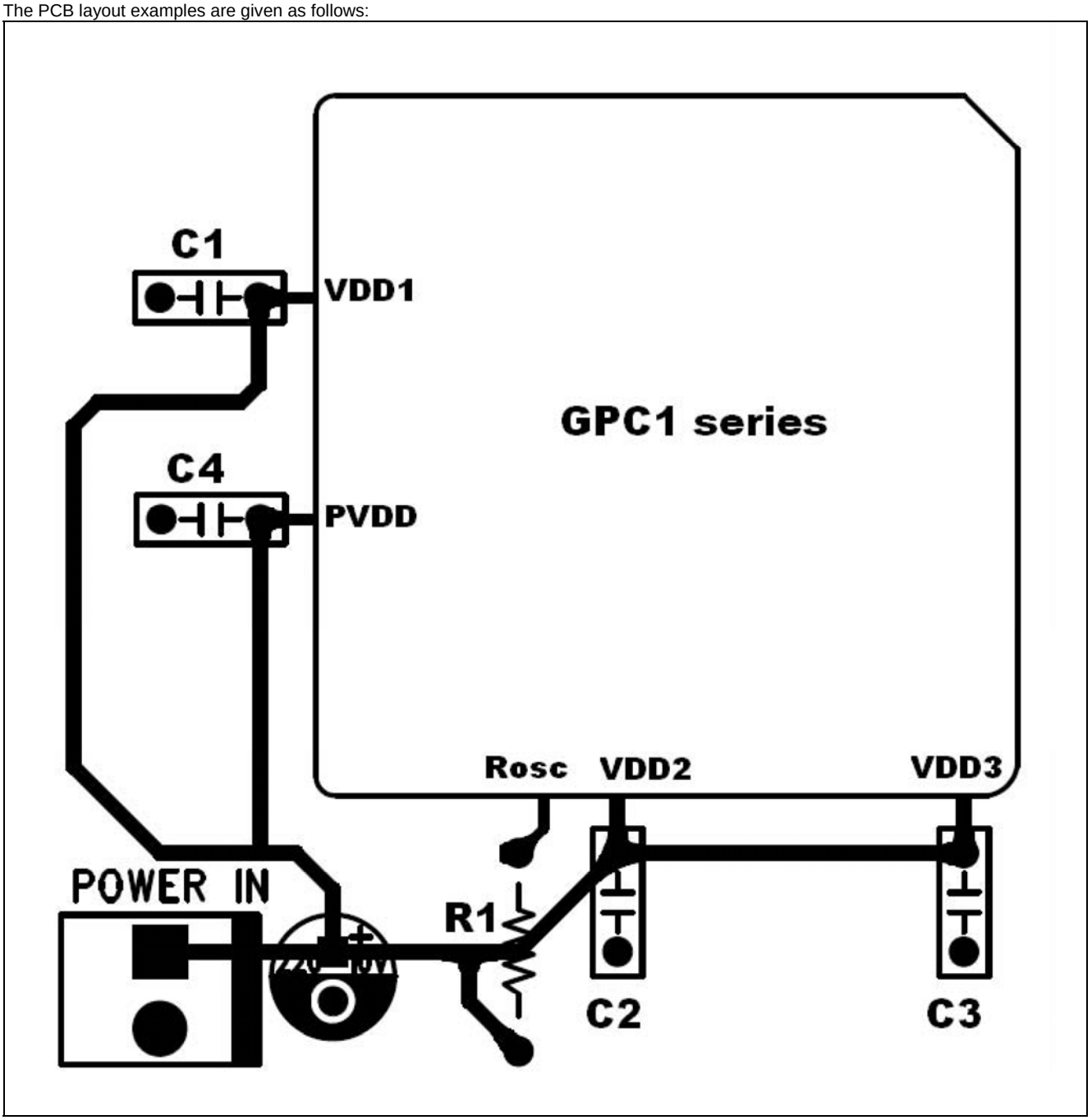
1.VDD1, VDD2, VDD3, PVDD must be connected to power input port directly, not to be the branch of each other.
2.VSS1, VSS2, VSS3, PVSS must be connected to ground input port directly, not to be the branch of each other.
3.R1 and C6 should be as close as possible to ROSC pin.
4.C2 should be as close as possible to VDD1/VSS1 pin.
5.C3 should be as close as possible to PVDD/PVSS pin.
6.C4 should be as close as possible to VDD2/VSS2 pin.
7.C5 should be as close as possible to VDD3/VSS3 pin.

9. PCB LAYOUT GUIDE

To avoid the unexpected noises to end up with abnormal CPU operations, the following cares must be exercised while doing the PCB layout:

1. Bond all VDD and VSS pins out.
2. The 0.1μF capacitor (C1-C4) placed between VDD and VSS must be as closed as possible to IC itself.
3. The ROSC resistor R1 must be as closed as possible to IC itself.

The PCB layout examples are given as follows:



10. PACKAGE/PAD LOCATIONS

10.1. Ordering Information

Product Number	Package Type
GPC11A24A1 - NnnV - C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

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12. REVISION HISTORY

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