DATA SHEET

GPC12A

12KB Sound Controller (OTP)

MAR. 23, 2006

Version 1.0

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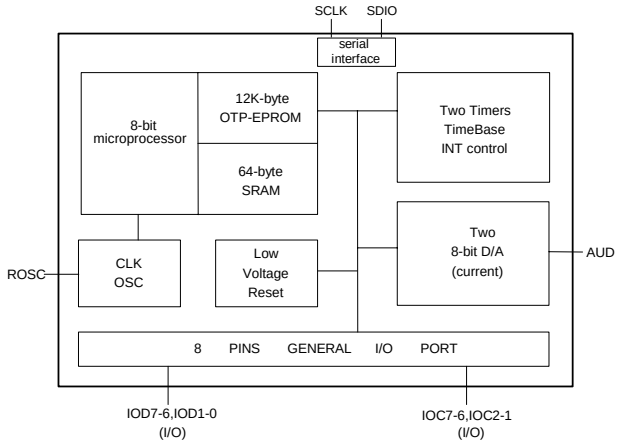
12KB SOUND CONTROLLER (OTP)

1. GENERAL DESCRIPTION

The GPC12A, a two-channel speech/melody synthesizer, equips an 8-bit CMOS microprocessor with 69 instructions, 12K-byte OTP-EPROM for speech and melody data (speech compressed by a 4-bit ADPCM with approx. three seconds speech duration @ 6.0KHz sampling rate), 64-byte working SRAM Other primary features include two Timer/Counters, 8 Software Selectable I/Os, and one 8-bit current D/A output. In audio processing, melody and speech can be mixed into one output. It operates at a wide voltage range of 2.4V - 5.5V with a Low Voltage Reset function that automatically resets CPU when operating voltage is less than 2.2V. Plus, a Clock Stop mode is built in for power savings. The unique power saving mode saves the RAM contents, but freezes the oscillator to stop executing other functions. The maximum CPU frequency can run up to 6.0MHz and the instruction cycle is two clock cycles (min.) ~ six clock cycles (max.). The GPC12A loads, not only the latest technology, but also the full commitment and technical support of Generalplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- 12K-byte OTP-EPROM for program and audio data
- 64-byte working SRAM
- Software-based audio processing
- Wide operating voltage: 2.4V - 5.5V @ 4.0MHz
  3.6V - 5.5V @ 6.0MHz
- Supports R_{OSC} only
- Max. CPU clock: 4.0MHz @ 3.0V, 6.0MHz @ 5.0V
- Standby mode (Clock Stop mode) for power savings.
  Max. 8.0μA @ 5.0V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- Eight general I/Os
- Two 12-bit timer/counters
- Six INT sources
- Key wake -up function
- Approx. 3-sec speech @ 6.0KHz sampling rate with ADPCM
- One D/A output
- Low Voltage Reset

4. APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- Advanced toy controller
- General speech synthesizer
- Industrial controller

5. SIGNAL DESCRIPTIONS*

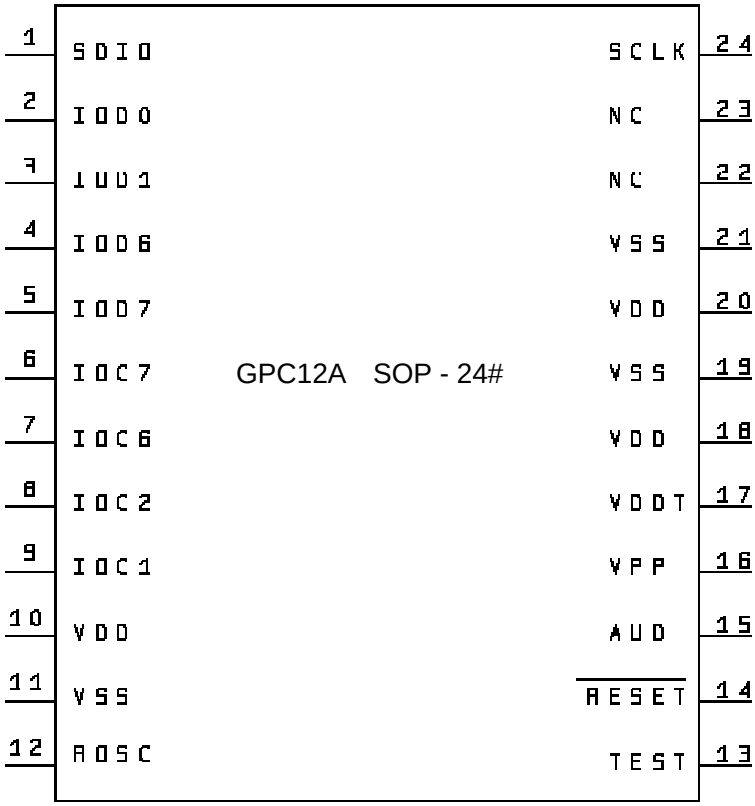
Mnemonic	PIN No.		Type	Description
	Chip	Package		
SCLK	1	24	I	Clock input of serial interface
SDIO	2	1	I/O	Data of serial interface.
IOD0 IOD1 IOD6 IOD7	3 4 5 6	2 3 4 5	I/O I/O I/O I/O	PortD is a 4-bit bi-directional programmable Input/Output port with Pull-low or Open-drain option. In input mode, PortD can be either Pure or Pull-low states. In output mode, PortD can be either Buffer or Open-drain PMOS type (source current). (Key change, Wake up I/O) **See note 1 and 2 below.
IOC7 IOC6 IOC2 IOC1	7 8 9 10	6 7 8 9	I/O I/O I/O I/O	PortC is a 4-bit bi-directional programmable Input/Output port with Pull-high or Open-drain option. In input mode, PortC can be in either Pure or Pull-high states. In output mode, IOC2, IOC1 can be a Buffer or Open-drain NMOS type (sink current). IOC7, IOC6 can be a Buffer or Open-drain PMOS type (source current). IOC1: EXT INT IN IOC2: EXT COUNT IN **See note 1 and 2 below.
VDD	11	10	I	Power input
VSS	12	11	I	Ground
ROSC	13	12	I	ROSC Resistor input (Resistor must be connected to VDD)
TEST	14	13	I	Test pin, NC
$\overline{\text{RESET}}$	15	14	I	This pin is an active low reset to the chip
AUD	16	15	O	Audio output
VPP	17	16	I	High voltage input for EPROM use
VDDT	18	17	I	Power input for EPROM use
VDD	19	18	I	Power input
VSS	20	19	I	Ground
NC	21 - 27	22 - 23		NC
VDD	28	20	I	Power input
VSS	29	21	I	Ground

* Refer to GPC Programming Guide for more information.

****Note:** 1.) Two input states can be specified: Pure Input, Pull-High or Pull Low.

2.) Three output states can be specified: Buffer output, Open Drain PMOS output (send), or Open Drain NMOS output (sink).

5.1. PIN Map


1 SDIO
2 IOD0
3 IOD1
4 IOD6
5 IOD7
6 IOC7
7 IOC6
8 IOC2
9 IOC1
10 VDD
11 VSS
12 ROSC
GPC12A SOP - 24#
24 SCLK
23 NC
22 NC
21 VSS
20 VDD
19 VSS
18 VDD
17 VDDT
16 VPP
15 AUD
14 RESET
13 TEST

6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The microprocessor in GPC12A is a high performance 8-bit processor equipped Accumulator, Program Counter, X Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure). The maximum CPU speed of 6.0MHz is capable of bringing you the cleaner speech, pleasant music as well as achieving the best performance.

6.2. OTP EPROM Area

The OTP EPROM area in GPC12A is 12K-byte that can be used for program as well as data.

6.3. RAM Area

The total RAM size is 64-bytes (including Stack) starting from address $C0 through $FF.

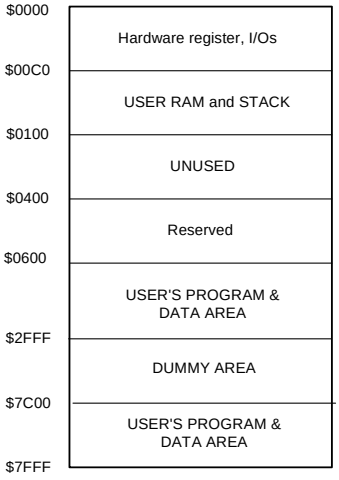
6.4. Map of Memory and I/Os

*I/O PORT:
- PORT IOC $0004
  IOD $0005
- I/O CONFIG $0000
  $0001

*NMI SOURCE:
- INTA (from TIMER A)

*INT SOURCE:
- INTA (from TIMER A)
- INTB (from TIMER B)
- CPU CLK / 1024
- CPU CLK / 8192
- CPU CLK / 65536
- EXT INT

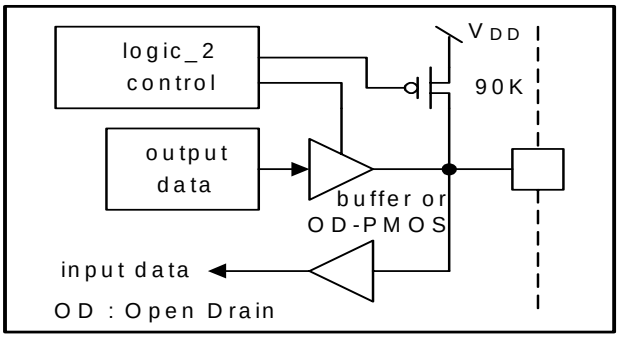
*MEMORY MAP (From ROM view)



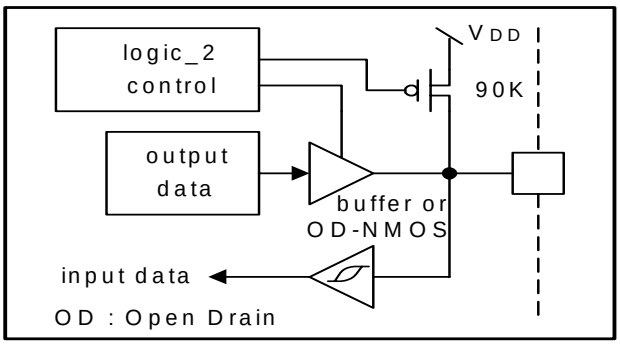
Note1: $05F0 (bit0): watchdog timer ON/OFF.
Note2: $05F6, $05F7: EPROM checksum.
Note3: $05F8 (bit7): Security bit

6.5. I/O Port Configuration*

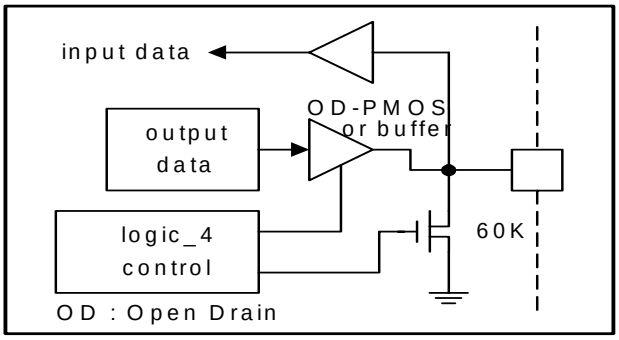
Input/Output IOC port : IOC7 - IOC6



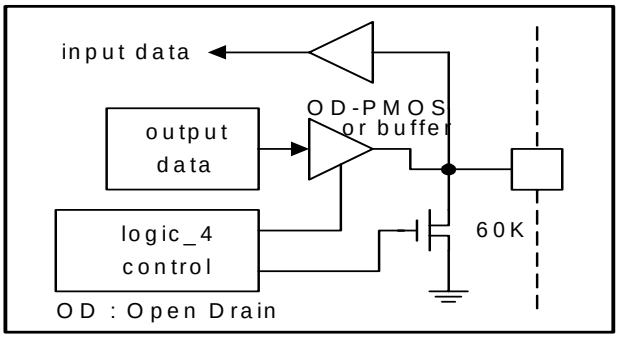
Input/Output IOC port : IOC2 - IOC1



Input/Output IOD port : IOD7 - IOD6



Input/Output IOD port : IOD1 - IOD0



Note: * Values are for VDD = 5.0V test conditions only.

6.6. Power Saving Mode

The GPC12A includes a power saving mode (Standby mode) for those applications that require very low standby current. To enter standby mode, the Wake-Up Register must be enabled and then stop the CPU clock by writing the STOP CLOCK Register to enter standby mode. In such mode, RAM and I/Os will remain in their previous states until being awaken. Port IOD (7, 6, 1, 0) is the only wake-up source in the GPC12A. After the GPC12A is awakening, the internal CPU will go to the RESET State (Tw ≧ 65536 x T1) and continue to execute program. Wakeup Reset will not affect RAM nor I/Os (FIG.1).

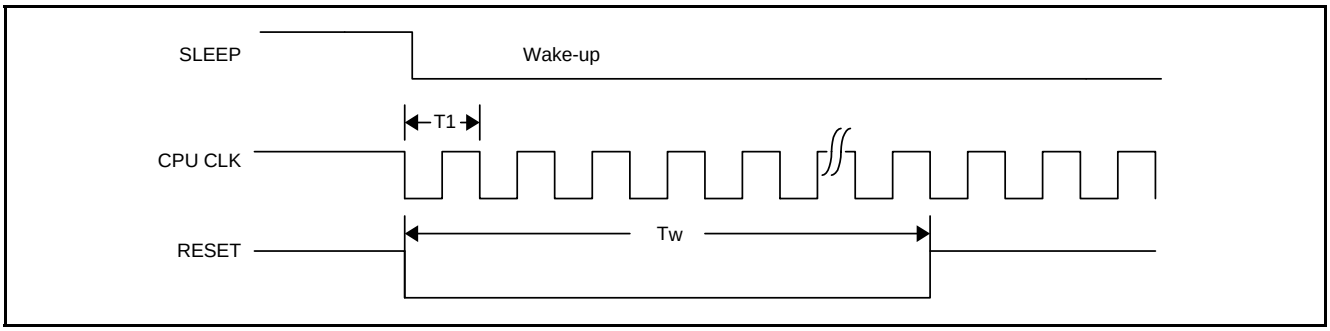
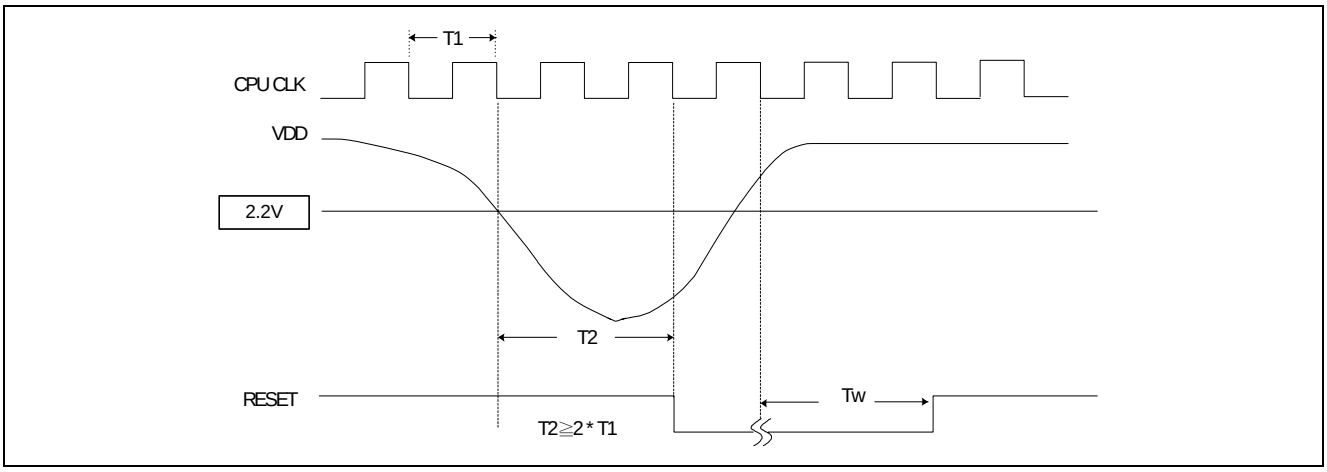


FIG. 1

T1 = 1 / (F_{CPU}), Tw ≧65536 x T1

6.7. Low Voltage Reset

The GPC12A has a Low Voltage Reset (LVR) function. In general, the CPU becomes unstable and malfunctions when the power voltage drops below certain operating voltage. With the unique design of Low Voltage Reset in GPC12A, it is able to reset all functions to the initial operational (stable) state if the VDD power-supply voltage drops around 2.2V (FIG.2).



(The LVR function is the same as Power ON Reset or External Reset.)

FIG. 2

6.8. Timer/Counter

The GPC12A has two 12-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer or a counter, but TMB can only be used as a timer. In the timer mode, TMA and TMB are re-loaded up-counters. When timer rollovers from $0FFF to $0000, the carry (overflow) signal will make the user's preset value to be loaded into timer automatically and up-count again. At the same time, the carry signal will generate an INT signal if the corresponding bit is enabled in the INT ENABLE Register. Suppose TMA is specified as a counter, users can reset it by loading #0 into the counter. After the counter has been activated, the value in the counter can also be read at the same time. The read instruction will not affect the value of the counter nor reset it.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	12-BIT TIMER	CPU CLOCK (T) or T/4
	12-BIT COUNTER	T/64, T/8192, T/65536 or EXT CLK
TMB	12-BIT TIMER	T or T/4
MODE SELECT REGISTER		TMA only, select timer or counter
TIMER CLOCK SELECTOR		Select T or T/4

6.9. Speech and Melody

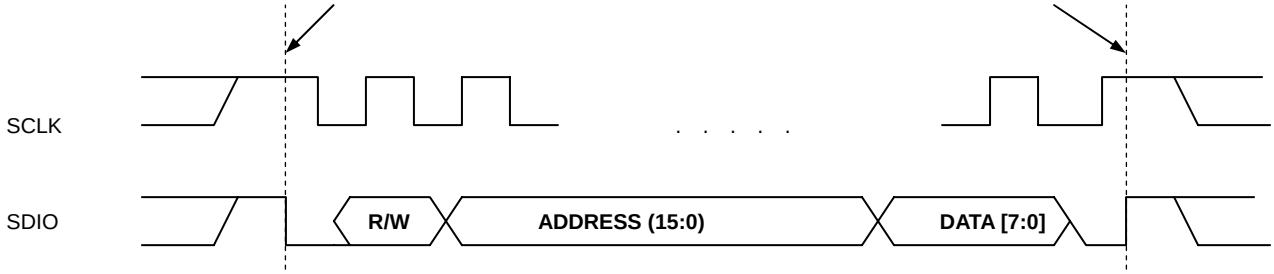
Since the GPC12A provides a large ROM and wide range of CPU operating speeds, it is the most suitable device for speech and melody synthesis.

In speech synthesis, the GPC12A can use NMI for accurate sampling frequency. The user can store the speech data in ROM and play it back with realistic sound quality. Several algorithms are recommended for high fidelity and compression of sound: PCM, LOG PCM, and ADPCM.

In melody synthesis, the GPC12A provides a dual tone mode to obtain melodious music. After selecting the dual tone mode, the user only needs to program either TMA or TMB, or both TMA and TMB to generate expected frequency for each channel. The hardware will toggle the tone wave automatically without entering into an interrupt service routine. The user can create musical instruments or sound effects by simply controlling the envelope of tone output.

6.10. Serial interface timing

1: Serial mode program condition: V_{BUREN} =13V, VDDT = 5V, VDD = 5V, VSS = 0V timing as following:



Note: R/W =1 for read mode; R/W =0 for write mode

6.11. Watchdog enable/disable

$05F0 (bit0): watchdog timer option.

'1': disable watchdog timer. Generalplus highly recommend disabling the watchdog timer.

'0': enable watchdog timer

6.12. Identify code and Security option

$05F6 and $05F7: EPROM checksum for identifying use.

Serial mode can read data of $05F6 and $05F7 even security is on.

$05F8 (bit7): security option.

'1': security OFF.

'0': security ON.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC2}	-	2.0	4.0	MHz	VDD = 2.4V - 3.6V, for 2-battery
		-	4.0	6.0	MHz	VDD = 3.6V - 5.5V, for 3-battery

7.3. DC Characteristics (VDD = 3.0V, T_A = 25°C)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	1.5	2.0	mA	F_{CPU} = 3.0MHz @ 3.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 3.0V
Audio Output Current	I_{AUD}	-	-1.5	-	mA	VDD = 3.0V,one-channel
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input High Level(IOC2-1)	V_{IH}	1.6	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Input Low Level (IOC2-1)	V_{IL}	-	-	1.1	V	VDD = 3.0V
Output High Current (IOC, IOD)	I_{OH}	-1.0	-	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Output Sink Current (IOC, IOD)	I_{OL}	2.0	-	-	mA	VDD = 3.0V, V_{OL} = 0.8V
Input Resistor (IOD)	R_{IN}	-	100	-	Kohm	Pull Low, VDD = 3.0V, V_{IN} = VDD

7.4. DC Characteristics (VDD = 5.0V, T_A = 25°C)

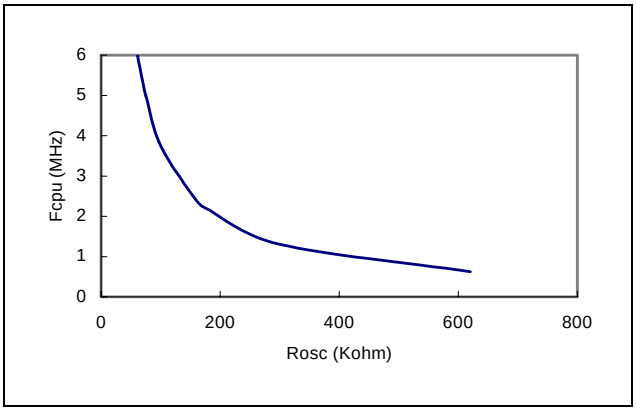
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	4.0	5.0	mA	F_{CPU} = 4.0MHz @ 5.0V, no load
Standby Current	I_{STBY}	-	-	8.0*	μA	VDD = 5.0V
Audio Output Current	I_{AUD}	-	-3.0	-	mA	VDD = 5.0V, one-channel
Input High Level	V_{IH}	3.0	-	-	V	VDD = 5.0V
Input High Level (IOC2-1)	V_{IH}	2.0	-	-	V	VDD = 5.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 5.0V
Input Low Level(IOC2-1)	V_{IL}	-	-	1.6	V	VDD = 5.0V
Output High Current (IOC, IOD)	I_{OH}	-1.0	-	-	mA	VDD = 5.0V, V_{OH} = 4.2V

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Output Sink Current (IOC, IOD)	I_{OL}	4.0	-	-	mA	VDD = 5.0V, V_{OL} = 0.8V
Input Resistor (IOD)	R_{IN}	-	60	-	Kohm	Pull Low, VDD = 5.0V, V_{IN} = VDD

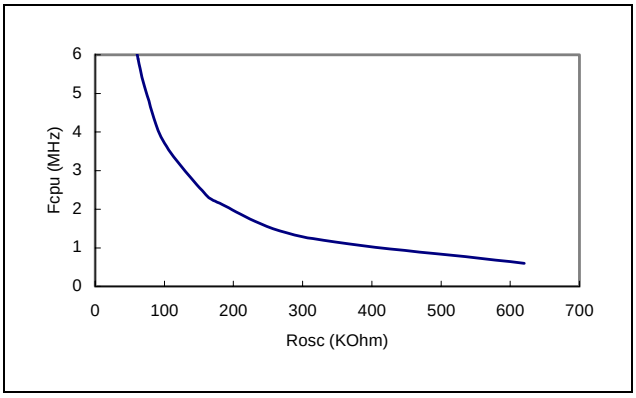
Note*: Regarding EPROM option code bias circuit design, ISTBY on VDD=5V is more than on VDD=3V

7.5. The Relationship between R_{OSC} and F_{CPU}

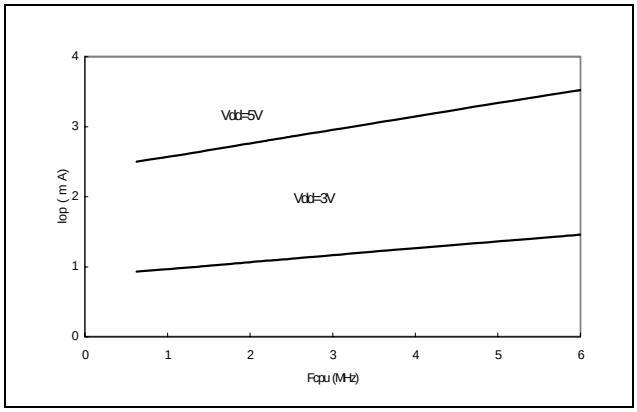
7.5.1. VDD = 3.0V



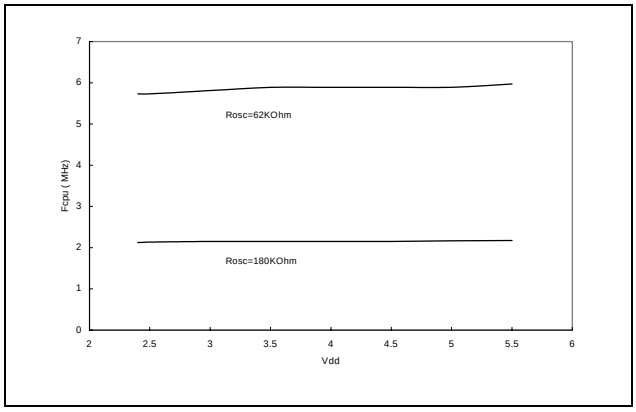
7.5.2. VDD = 5.0V



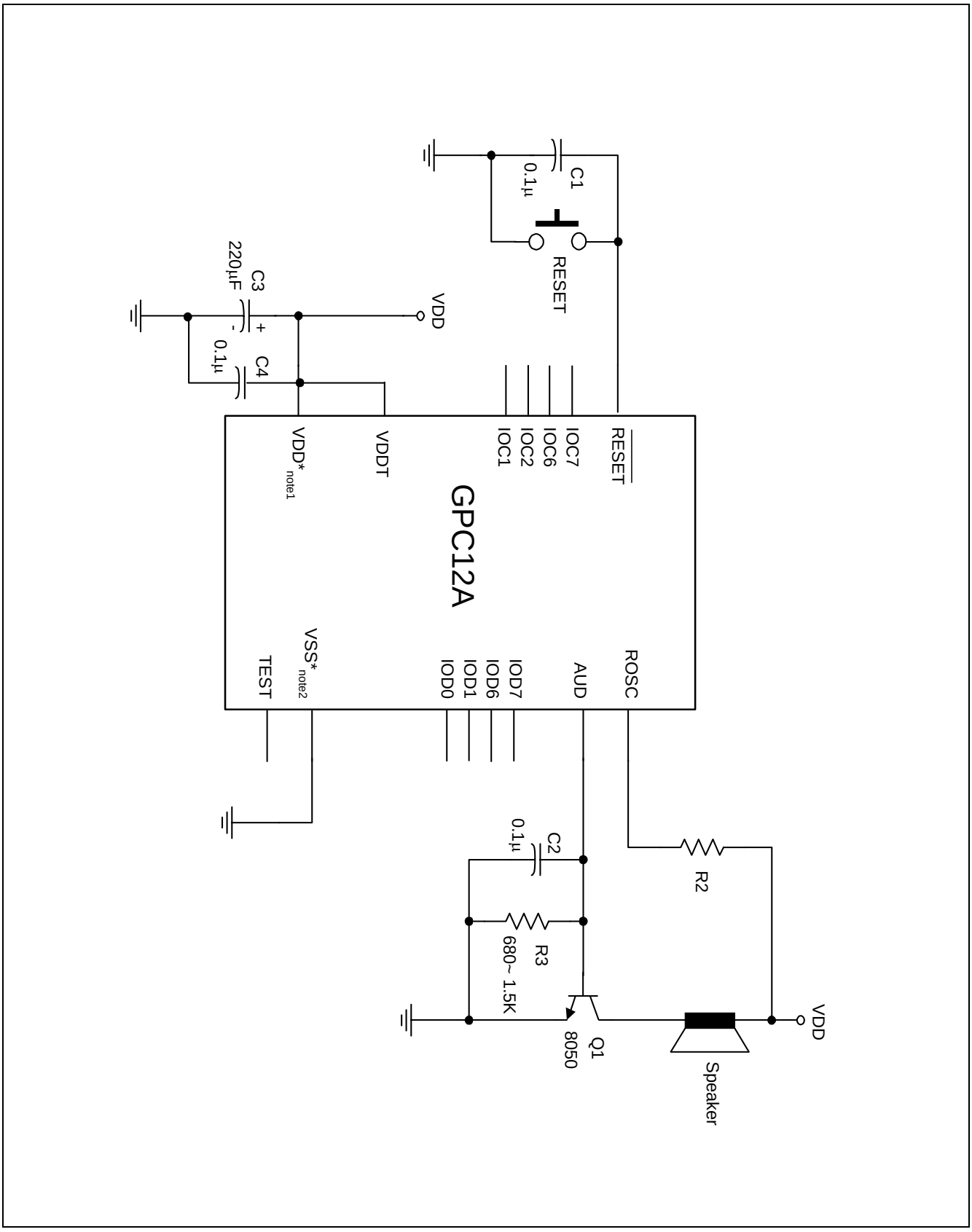
7.6. The Relationship between I_{OP} and F_{CPU}



7.7. The Relationship between F_{CPU} and VDD



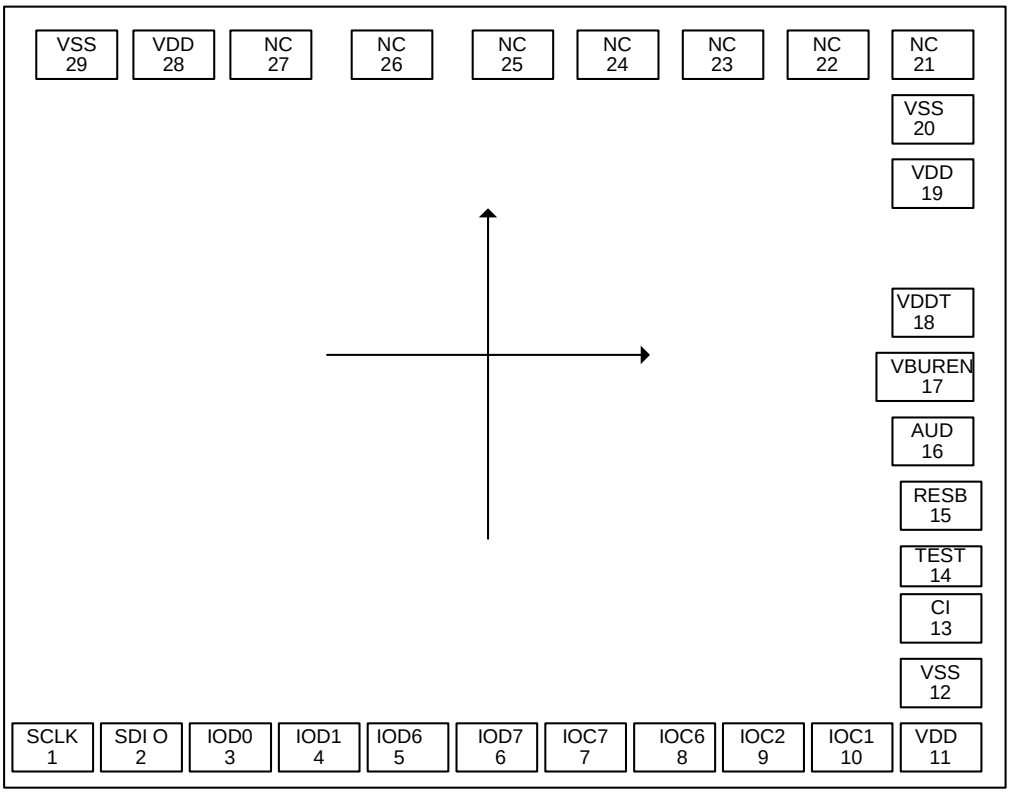
8. APPLICATION CIRCUIT



Note1: VDD pin tie together, (11, 19, 28) for chip form, (10, 18, 20) for package
Note2: VSS pin tie together, (12, 20, 29) for chip form, (11, 19, 21) for package

9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



This IC substrate should be connected to VSS

Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

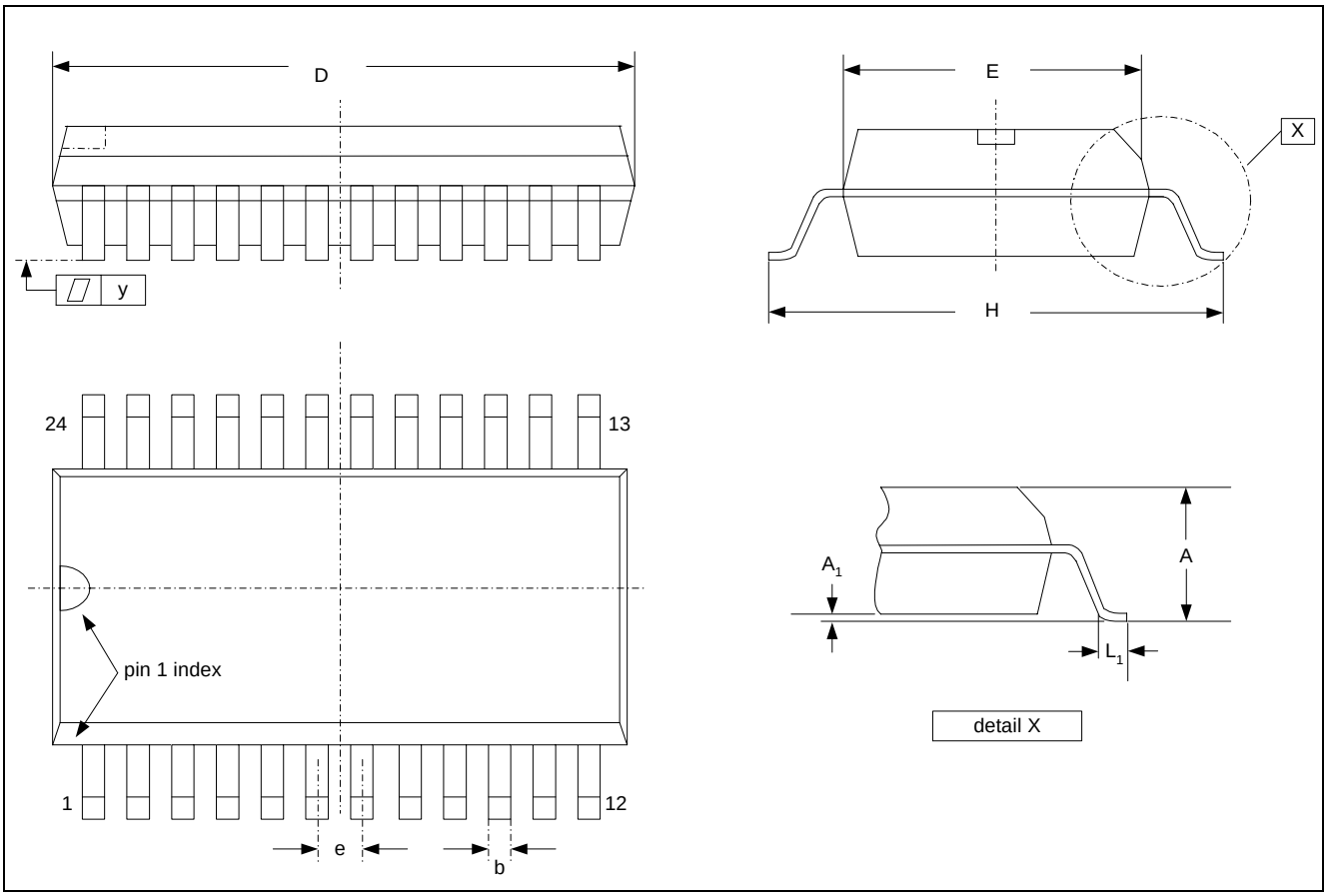
Product Number	Package Type
GPC12A-NnnV-C	Chip form
GPC12A-NnnV-PS10x	Package form - SOP 24

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 0 - 9, serial number).

9.3. Package Information



Symbol	Dimension in inch		
	Min.	Typ.	Max.
A	0.093	0.099	0.104
A1	0.004	-	0.012
b	-	0.016	-
D	0.599	0.600	0.614
E	0.291	0.295	0.299
e	-	0.050	-
H	0.394	0.406	0.419
L1	0.016	0.035	0.050
y	-	-	0.004

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
MAR. 23, 2006	1.0	Original Note: The GPC12A data sheet v1.0 is a continued version of SPC12A data sheet v0.3.	16