DATA SHEET

GPC251A1

256KB Sound Controller

FEB. 23, 2006

Version 1.0

Table of Contents

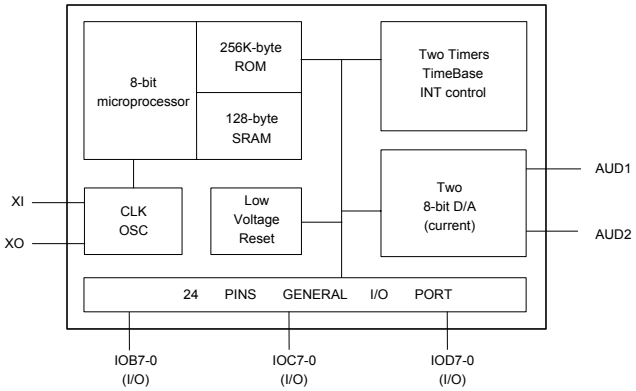
PAGE

256KB SOUND CONTROLLER

1. GENERAL DESCRIPTION

The GPC251A1 is a CPU based two-channel speech/melody synthesizer including CMOS 8-bit microprocessor with 69 instructions, 256K-byte ROM for speech and melody data (Speech is compressed by a 4-bit ADPCM with approx. 85 sec speech duration @ 6KHz sampling rate) and 128-byte working SRAM. It includes two Timer/Counters, 24 Software Selectable I/Os, and two 8-bit current outputs (D/A). For audio processing, melody and speech can be mixed into one output. It operates over a wide voltage range of 2.4V - 5.5V and includes Low Voltage Reset function. The Low Voltage Reset automatically resets when the working voltage is less than 2.2V. In addition, GPC251A1 has a Clock Stop mode for power savings. The power savings mode saves the RAM contents, but freezes the oscillator, causing all other chip functions to be inoperative. The Max. CPU clock frequency is 6.0MHz. It has an Instruction Cycle Rate of 2 clock cycles (min.) - 6 clock cycles (max.). The GPC251A1 includes not only the latest technology, but also the full commitment and technical support of Generalplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- Provides 256K-byte ROM for program and audio data
- 128-byte working SRAM
- Software-based audio processing
- Wide operating voltage: 2.4V - 3.6 V @ 4.0MHz
  3.6V - 5.5V @ 6.0MHz
- Supports Crystal Resonator or R_{OSC} (with Mask option)
- Max. CPU clock: 4.0MHz @ 2.4V - 3.6V
  6.0MHz @ 3.6V - 5.5V
- Standby mode (Clock Stop mode) for power savings. Max. 2μA @ 5.0V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- Provides 24 general I/Os
- Two 12-bit timer/counters
- 6 INT sources
- Key wake-up function
- Approx. 85 sec speech @ 6KHz sampling rate with 4-bit ADPCM
- Two DA output
- Low Voltage Reset
- Volume control function

4. APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- High end toy controller
- Talking instrument controller
- General speech synthesizer
- Industrial controller

5. SIGNAL DESCRIPTIONS*

Mnemonic	Pin No.	Type	Description
VDD	17	I	Power VDD
VSS	13, 14	I	Power VSS
XI	19	I	Oscillator crystal input or RESISTOR (Resistor should be connected to VDD)
XO	18	O	Oscillator crystal output
TEST	22	I	Test pin, NC
RESET	16	I	This pin is an active low reset for the chip.
AUD1 AUD2	20 21	O	Audio output
IOB0 IOB1 IOB2 IOB3 IOB4 IOB5 IOB6 IOB7	31 32 33 1 2 3 4 5	I/O I/O I/O I/O I/O I/O I/O I/O	Port B is an 8-bit bi-directional Input / Output port with Pull-low or Open-drain option. As inputs, Port B can be in either the Pure or Pull-low states. As outputs, Port B can be either Buffer or Open-drain NMOS types (Sink current). **See note 1 and 2 below.
IOC0 IOC1 IOC2 IOC3 IOC4 IOC5 IOC6 IOC7	15 12 11 10 9 8 7 6	I/O I/O I/O I/O I/O I/O I/O I/O	Port C is an 8-bit bi-directional Input / Output port with Pull-high or Open-drain option. As inputs, Port C can be in either the Pure or Pull-high states. As outputs Port C can be a Buffer type or Open-drain type. Port C3 - 0 are Open-drain NMOS type (Sink current) and Port C7 - 4 are Open-drain PMOS (Send current). IOC0: Serial programming Data IOC1: Also selectable as an external interrupt PIN IOC2: EXT COUNT IN **See note 1 and 2 below.
IOD0 IOD1 IOD2 IOD3 IOD4 IOD5 IOD6 IOD7	30 29 28 27 26 25 24 23	I/O I/O I/O I/O I/O I/O I/O I/O	Port D is an 8-bit bi-directional programmable Input / Output port with Pull-low or Open-drain option. As inputs, Port D can be either Pure or Pull-low states. As outputs, Port D can be either Buffer or Open-drain PMOS (send current). Also, Port D can be software programmed for wake-up I/O pins. (Key Change, Wake-up I/O). **See note 1 and 2 below.

* Refer to GPC Programming Guide for complete information.

**Note: 1.) Two input states can be specified; Pure Input, Pull-High or Pull Low.

2.) Three output states can be specified as Buffer output, Open Drain PMOS output (send), or Open Drain NMOS output <sink>.

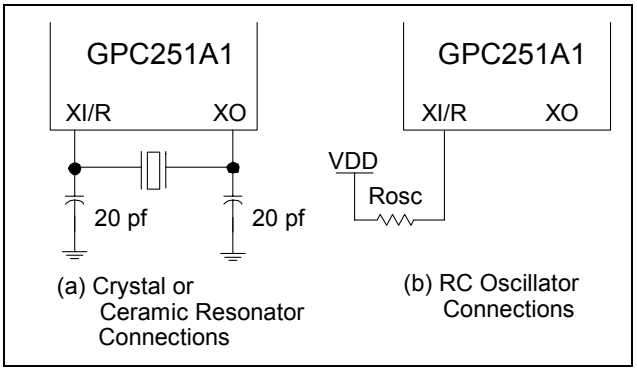
6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The 8-bit microprocessor of GPC251A1 is a high performance processor equipped with Accumulator, Program Counter, X Register, Stack pointer and Processor Status Register (this is the same as the 6502 instruction structure). GPC251A1 is able to perform with 6.0MHz (max.) depending on the application specifications.

6.2. Oscillator

The GPC251A1 supports AT-cut parallel resonant oscillated Crystal / Resonator or RC Oscillator or external clock sources by mask option (select one from those three types). The design of application circuit should follow the vendors' specifications or recommendations. The diagrams listed below are typical X'TAL/ROSC circuits for most applications:



6.3. Mask Option

The GPC251A1 has the following mask option:

- Supports Crystal Resonator or R_{OSC} (with mask option).

6.4. ROM Area

The GPC251A1 provides a 256K-byte ROM that can be defined as the program area, audio data area, or both. To access ROM, users should program the BANK SELECT Register; choose bank, and access address to fetch data.

6.5. RAM Area

The GPC251A1 total RAM consists of 128 bytes (including Stack) at locations from $80 through $FF.

6.6. Volume Control Function

The GPC251A1 contains a volume control function that provides an 8-step volume controller to control current D/A output. A volume control function selector (Enable/Disable) register and controller register is provided.

6.7. Map of Memory and I/Os

*I/O PORT:

– PORT IOA $0002
IOB $0003
IOC $0004
IOD $0005

– I/O CONFIG $0000
$0001

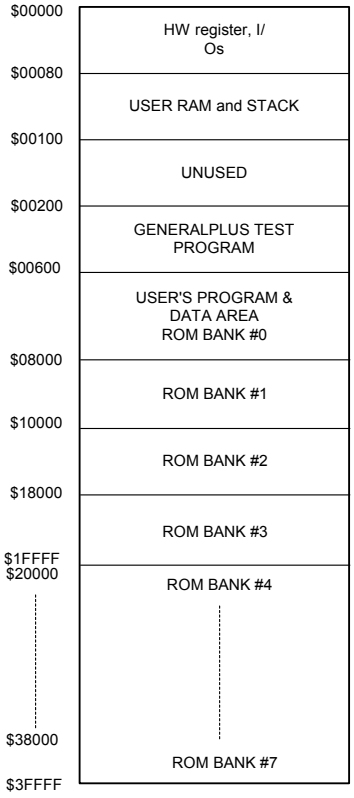
*NMI SOURCE:

– INTA (from TIMER A)

*INT SOURCE:

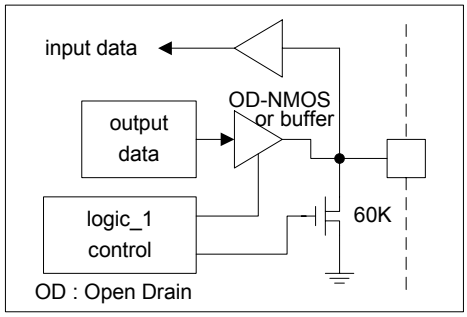
– INTA (from TIMER A)
– INTB (from TIMER B)
– CPU CLK / 1024
– CPU CLK / 8192
– CPU CLK / 65536
– EXT INT

*MEMORY MAP (From ROM view)

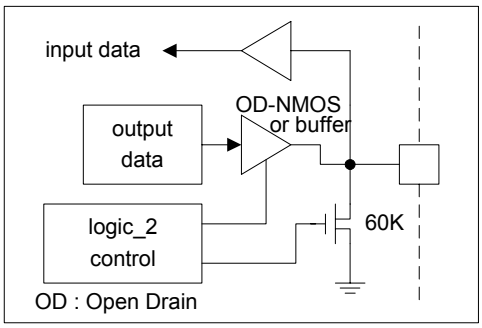


6.8. I/O Port Configurations*

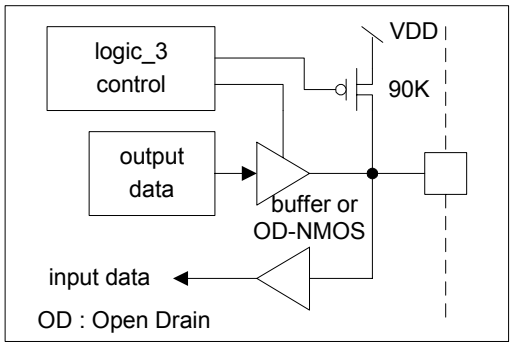
Input/Output IOB port : IOB3 - 0



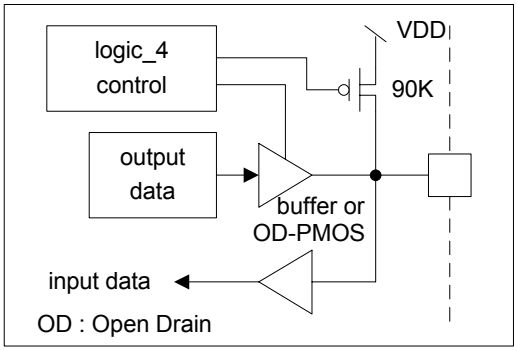
Input/Output IOB port : IOB7 - 4



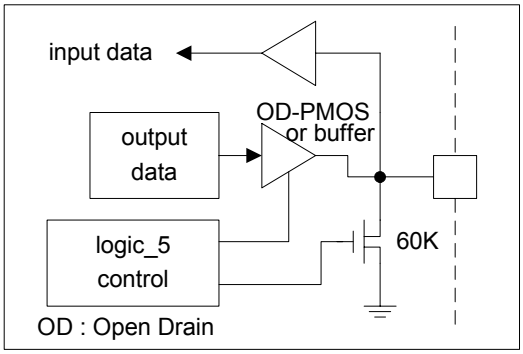
Input/Output IOC port : IOC3 - 0



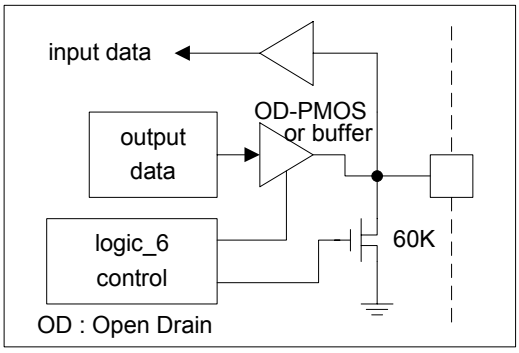
Input/Output IOC port : IOC7 - 4



Input/Output IOD port : IOD3 - 0



Input/Output IOD port : IOD7 - 4



*Values shown are for VDD = 5.0V test conditions only.

6.9. Timer/Counter

The GPC251A1 contains two 12-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer or a counter, but TMB can only be used as a timer. In the timer mode, TMA and TMB are re-loaded up-counters. When timer overflows from $0FFF to $0000, the carry signal will make the timer automatically reload to the user's pre-set value and be up-counted again. At the same time, the carry signal will generate the INT signal if the corresponding bit is enabled in the INT ENABLE Register. If TMA is specified as a counter, users can reset by loading #0 into the counter. After the counter has been activated, the value of the counter can also be read from the counters at the same time. The read instruction will not affect the value of the counter or reset it.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	12-BIT TIMER	CPU CLOCK (T) or T/4
	12-BIT COUNTER	T/64, T/8192, T/65536 or EXT CLK
TMB	12-BIT TIMER	T or T/4
MODE SELECT REGISTER		TMA only, select timer or counter
TIMER CLOCK SELECTOR		Select T or T/4

6.10. Speech and Melody

Since the GPC251A1 provides a large ROM and wide range of CPU operation speeds, it is most suitable for speech and melody synthesis.

For speech synthesis, the GPC251A1 can provide NMI for accurate sampling frequency. Users can record or synthesize the sound and digitize it into the ROM. The sound data can be played back in the sequence of the control functions as designed by the user's program. Several algorithms are recommended for high fidelity and compression of sound including PCM, LOG PCM, and ADPCM.

For melody synthesis, the GPC251A1 provides the dual tone mode. After selecting the dual tone mode, users only need to fill either TMA or TMB, or both TMA and TMB to generate expected frequency for each channel. The hardware will toggle the tone wave automatically without entering into an interrupt service routine. Users are able to simulate musical instruments or sound effects by simply controlling the envelope of tone output.

6.11. Power Savings Mode

The GPC251A1 provides a power savings mode (Standby mode) for those applications that require very low stand-by current. To enter standby mode, the Wake-Up Register should be enabled and then stop the CPU clock by writing the STOP CLOCK Register. The CPU will then go to the stand-by mode. In such a mode, RAM and I/Os will remain in their previous states until being awakened. Port IOD7-0 is the only wake-up source in the GPC251A1. After the GPC251A1 is awakened, the internal CPU will go to the RESET State (Tw ≧ 65536 x T1) and then continue processing the program. Wakeup Reset will not affect RAM or I/Os (See FIG.1).

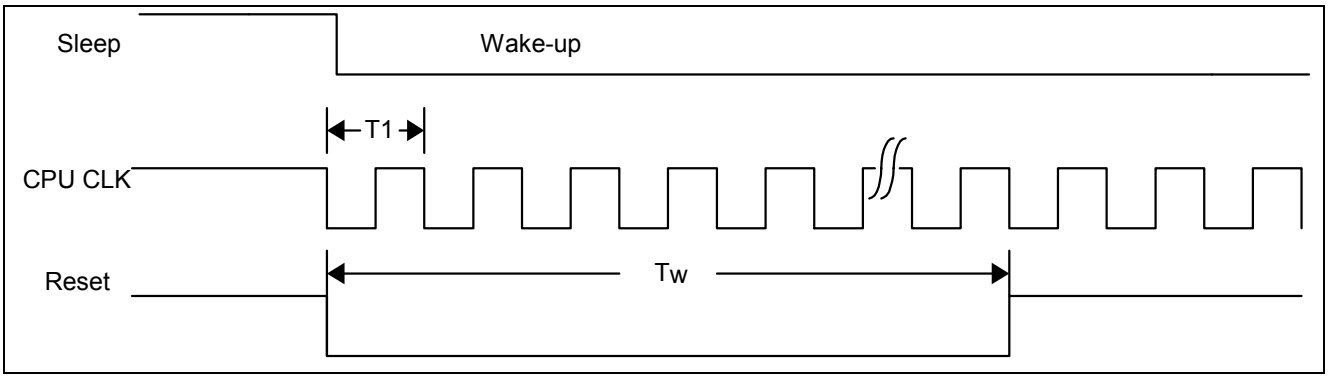
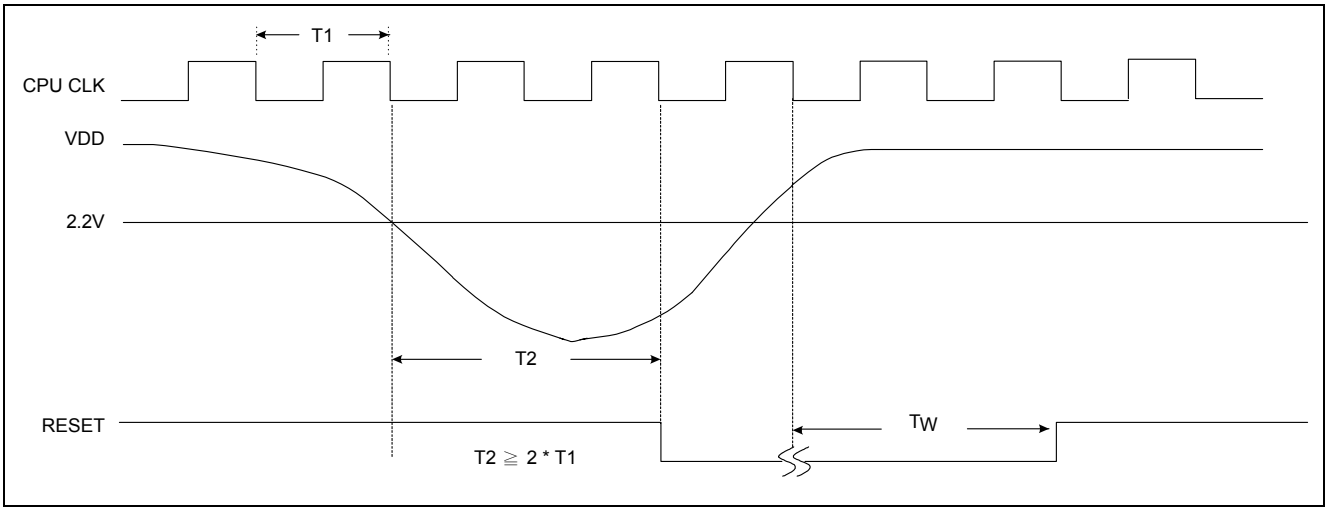


FIG. 1

T1 = 1 / (F_{CPU}), Tw ≧ 65536 x T1

6.12. Low Voltage Reset

The GPC251A1 includes a Low Voltage Reset (LVR) function. Below the minimum power-supply voltage of 2.2V, the CPU system will become unstable and malfunction. Low Voltage Reset will reset all functions into the initial operational (stable) state if the VDD power-supply voltage drops below 2.2V (FIG.2).



(The LVR function is the same as Power ON Reset or External Reset.)

FIG. 2

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
CPU Clock	F_{CPU}	-	2.0	4.0	MHz	VDD = 2.4V - 3.6V, 2-battery
		-	4.0	6.0	MHz	VDD = 3.6V - 5.5V, 3-battery

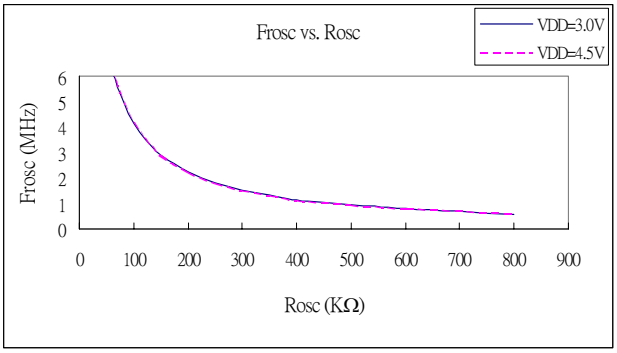
7.3. DC Characteristics (VDD = 3.0V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	1.5	2.0	mA	F_{CPU} = 3.0MHz @ 3.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 3.0V
Audio output current	I_{AUD}	-	-1.5	-	mA	VDD = 3.0V, one-channel
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High I IOB, IOC, IOD	I_{OH}	-1.0	-	-	mA	VDD = 3.0V V_{OH} = 2.0V
Output Sink I IOB, IOC, IOD	IOL	2.0	-	-	mA	VDD = 3.0V V_{OL} = 0.8V
Input Resistor IOB, IOD	R_{IN}	-	90	-	Kohm	Pull Low VDD = 3.0V

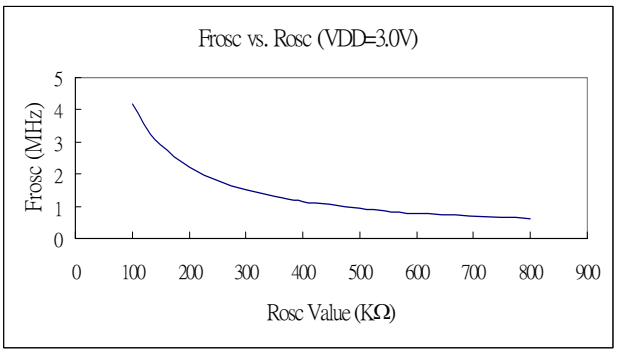
7.4. DC Characteristics (VDD = 5.0V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	4.0	5.0	mA	F_{CPU} = 4.0MHz @ 5.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 5.0V
Audio output current	I_{AUD}	-	-3.0	-	mA	VDD = 5.0V, one-channel
Input High Level	V_{IH}	3.0	-	-	V	VDD = 5.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 5.0V
Output High I IOB, IOC, IOD	I_{OH}	-1.0	-	-	mA	VDD = 5.0V V_{OH} = 4.2V
Output Sink I IOB, IOC, IOD	I_{OL}	4.0	-	-	mA	VDD = 5.0V V_{OL} = 0.8V
Input Resistor IOB, IOD	R_{IN}	-	45	-	Kohm	Pull Low VDD = 5.0V

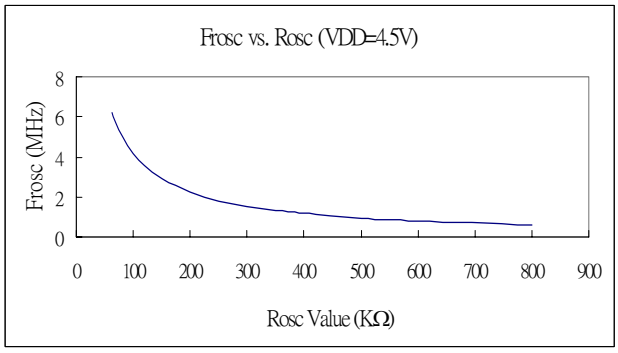
7.5. The Relationship between the R_{OSC} and the F_{CPU}



7.5.1. VDD= 3.0V, T_A = 25℃

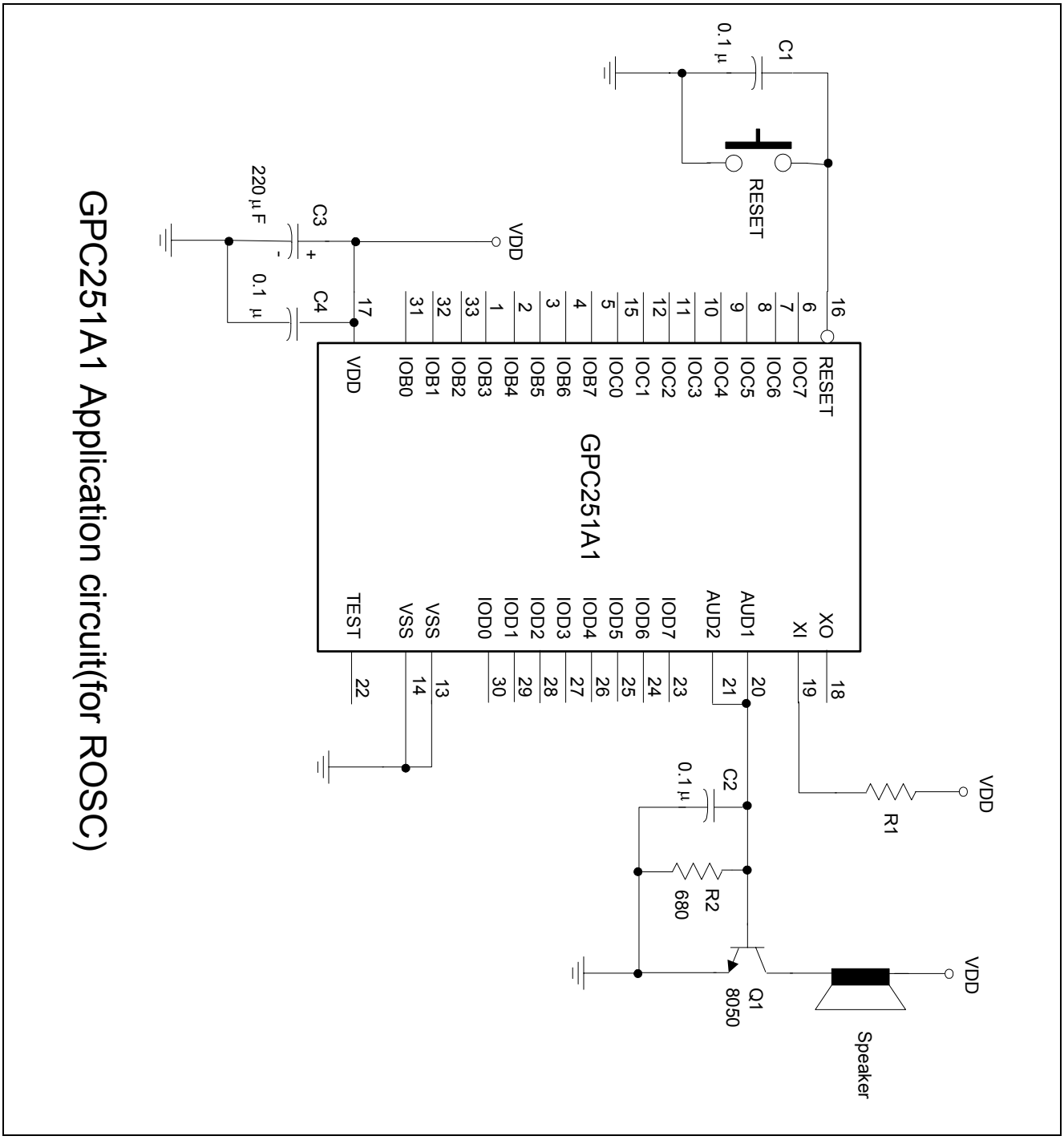


7.5.2. VDD= 4.5V, T_A = 25℃

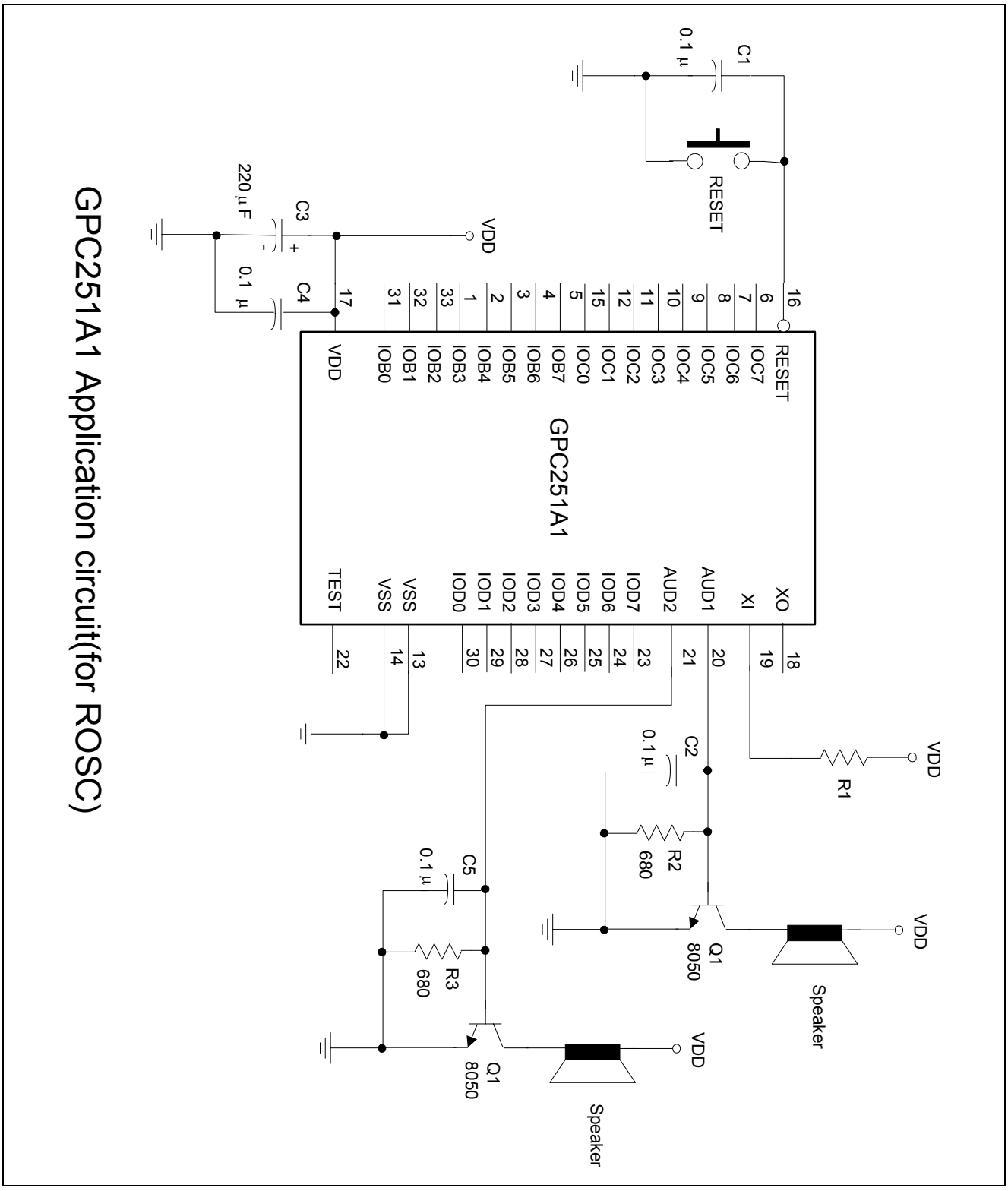


8. APPLICATION CIRCUITS

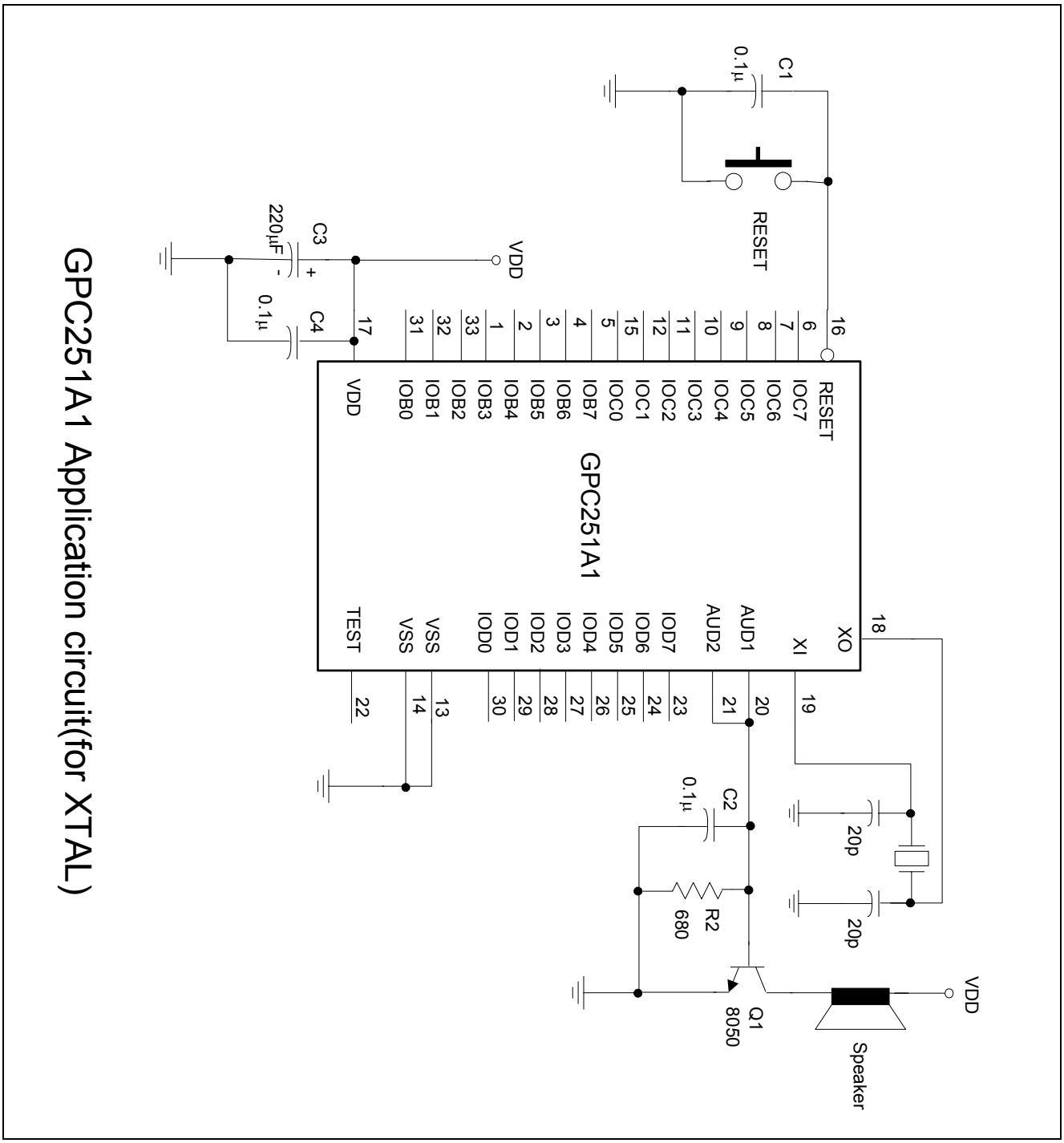
8.1. Application Circuit - (1)



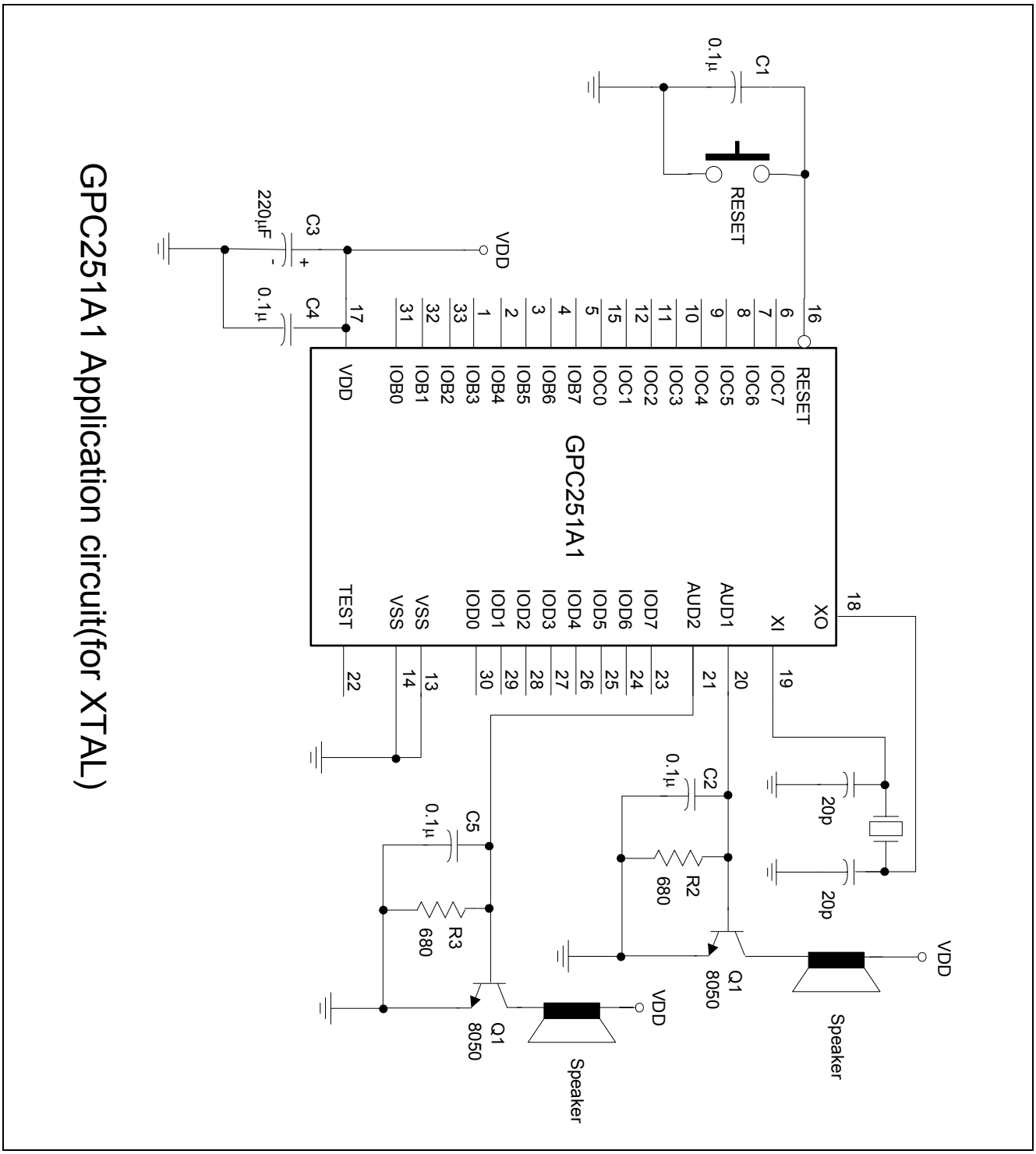
8.2. Application Circuit - (2)



8.3. Application Circuit - (3)

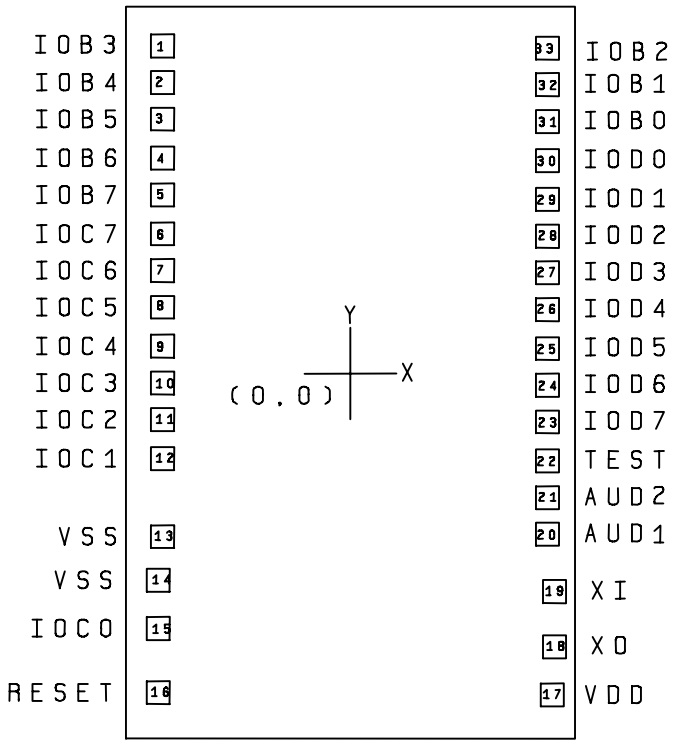


8.4. Application Circuit - (4)



9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



This IC substrate should be connected to VSS

Note1: To ensure that the IC functions properly, bond VDD and VSS pins.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
GPC251A1-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
FEB. 23, 2006	1.0	Original Note: The GPC251A1 data sheet v1.0 is a continued version of SPC251A1 data sheet v1.3.	16