DATA SHEET

GPCDXXXXA Series

Multi-Channel Sound Controller

Feb. 08, 2017

Version 1.5

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MULTI-CHANNEL SOUND CONTROLLER

1.GENERAL DESCRIPTION

The GPCDXXXXA series works with internal 128K~1M bytes ROM, 512 bytes working SRAM, three sets of 12-bit timer, 16~32 general I/Os with selectable 8+1/4+2/1+2 channels of input and one 14-bit DAC with push-pull amplifier. In audio signal processing, melody and speech can be mixed into one output. The GPCDXXXXA features up to two software channels and a high performance SPU voice engine to playback voice in ADPCM or PCM format. It is designed to operate over a wide voltage range along with low voltage reset function to assure the capability of operating at an extremely low voltage condition. In addition, GPCDXXXXA supports a sleep mode to save powers when power resource is limited such as power from ordinary battery or solar cell. While in standby mode, it can be rapidly awaked from sleep mode by interrupt sources or IO state alterations. A Serial Peripheral Interface (SPI) controller is also available in certain GPCDXXXXA series to facilitate communications with other devices and components.

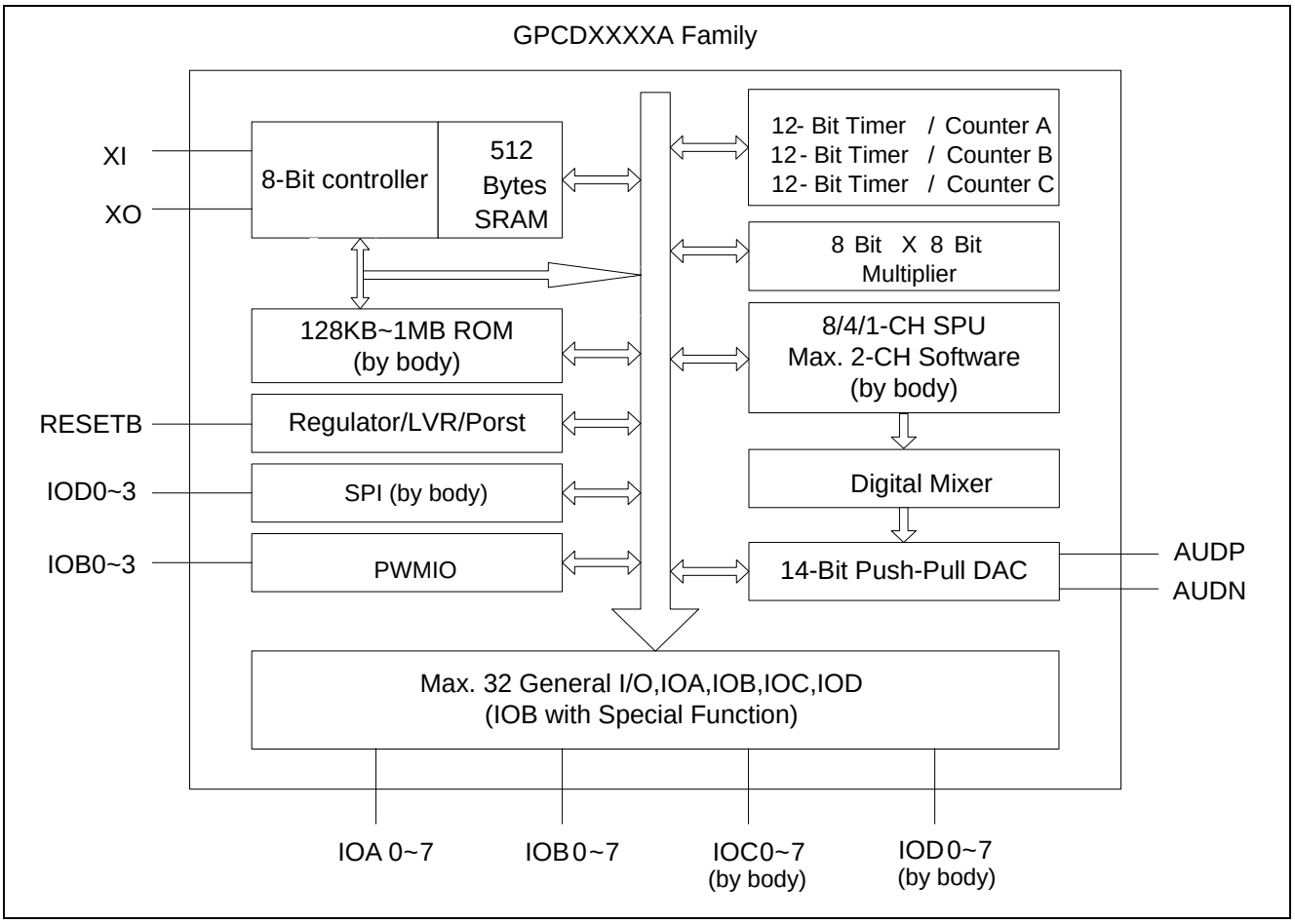
2.FEATURES

- ***Working Voltage: 2.1V/2.3V - 5.5V (by body option)***
- CPU Speed: max. 8MHz.
- F_{OSC} = max. 16MHz (2 x CPU clock)
- ROM Size: 128KB~1M bytes (by body)
- RAM Size: max. 512 bytes
- Three 12-bit timer/counter, TMA with capture and comparison function, TMB/TMC with comparison function only (Programmable and Auto Reload)
- Sleep mode to reduce power consumption
- Key change wake-up function
- IRQs & NMI Interrupts
- Clock source with ROSC or XTAL (option)
- Watchdog function (option)
- 5.5V to 3.3V regulator
- Low Voltage Reset and Low Voltage Detection
- Bit programmable 16~32 general I/Os (by body)
- Eight I/Os with high sink current for LED application
- All general IOs with 1M-Ohm pull-low function to prevent current leakage from key touch error.
- One 14-bit DAC with push-pull amplifier for direct drive speaker
- SPU(Sound Processing Unit) engine can output audio data with 14-bit resolution to perform high quality voice/melody
- IR PWM Output
- Hardware PWMIO supports four LED outputs with brightness control of 256-level
- Real-time clock
- 8/4/1-channel SPU engine with ADPCM/PCM wave table (by body option)
- Up to two sets of 14-bit software channel with noise filter to playback high quality sound
- SPI master interface (by body)

3.APPLICATION FIELD

- Talking instrument controller
- General Music synthesizer
- General purpose controller
- High end toy controller
- Intelligent education toys
- And more

4.BLOCK DIAGRAM



5.GPCDXXXXA FAMILY AND FEATURE LIST

Body	GPCD9340A	GPCD6340A	GPCD3340A	GPCD9300A	GPCD6300A	-
Voice Duration	340 Sec.	340 Sec.	340 Sec.	300 Sec.	300 Sec.	-
Working Voltage F_{osc} = Max. 16M	2.3~5.5V	2.3~5.5V	2.3~5.5V	2.3~5.5V	2.3~5.5V	-
Working Voltage F_{osc} = Max. 12M	2.1~5.5V	2.1~5.5V	2.1~5.5V	2.1~5.5V	2.1~5.5V	-
RAM Size	512B	512B	512B	512B	512B	-
ROM Size	1MB	1MB	1MB	912KB	912KB	-
IO Pin	32 (IOA/B/C/D)	32 (IOA/B/C/D)	32 (IOA/B/C/D)	32 (IOA/B/C/D)	32 (IOA/B/C/D)	-
SPU Channel	8	4	1	8	4	-
Software Channel	1	2	2	1	2	-
SPI	V	V	V	V	V	-
Body	**GPCD9270A**	**GPCD6270A**	**GPCD3270A**	**GPCD9220A**	**GPCD6220A**	**-**
Voice Duration	270 Sec.	270 Sec.	270 Sec.	220 Sec.	220 Sec.	-
Working Voltage F_{osc} = Max. 16M	2.3~5.5V	2.3~5.5V	2.3~5.5V	2.3~5.5V	2.3~5.5V	-
Working Voltage F_{osc} = Max. 12M	2.1~5.5V	2.1~5.5V	2.1~5.5V	2.1~5.5V	2.1~5.5V	-
RAM Size	512B	512B	512B	512B	512B	-
ROM Size	832KB	832KB	832KB	672KB	672KB	-
IO Pin	32 (IOA/B/C/D)	32 (IOA/B/C/D)	32 (IOA/B/C/D)	32 (IOA/B/C/D)	32 (IOA/B/C/D)	-
SPU Channel	8	4	1	8	4	-
Software Channel	1	2	2	1	2	-
SPI	V	V	V	V	V	-
Body	**GPCD9170A**	**GPCD6170A**	**GPCD3170A**	**GPCD9130A**	**GPCD6130A**	**GPCD3130A**
Voice Duration	170 Sec.	170 Sec.	170 Sec.	130 Sec.	130 Sec.	130 Sec.
Working Voltage F_{osc} = Max. 16M	2.1~5.5V	2.1~5.5V	2.1~5.5V	2.1~5.5V	2.1~5.5V	2.1~5.5V
RAM Size	512B	512B	512B	512B	512B	512B
ROM Size	512KB	512KB	512KB	416KB	416KB	416KB
IO Pin	24 (IOA/B/D)	24 (IOA/B/D)	24 (IOA/B/D)	24 (IOA/B/D)	24 (IOA/B/D)	24 (IOA/B/D)
SPU Channel	8	4	1	8	4	1
Software Channel	1	2	2	1	2	2
SPI	V	V	V	V	V	V
Body	**GPCD9080A**	**GPCD6080A**	**GPCD3080A**	**GPCD9040A**	**GPCD6040A**	**GPCD3040A**
Voice Duration	80 Sec.	80 Sec.	80 Sec.	40 Sec.	40 Sec.	40 Sec.
Working Voltage F_{osc} = Max. 16M	2.1~5.5V	2.1~5.5V	2.1~5.5V	2.1~5.5V	2.1~5.5V	2.1~5.5V
RAM Size	512B	512B	512B	512B	512B	512B
ROM Size	256KB	256KB	256KB	128KB	128KB	128KB
IO Pin	16 (IOA/B)	16 (IOA/B)	16 (IOA/B)	16 (IOA/B)	16 (IOA/B)	16 (IOA/B)
SPU Channel	8	4	1	8	4	1
Software Channel	1	2	2	1	2	2
SPI	X	X	X	X	X	X

6. Signal descriptions

6.1. Signal Description for GPCDXXXXA

Name	Type	Description	Note
IO PORT			
IOA0~IOA7	I/O	Bi-directional IO ports, can be wakeup pins	IOA0~3 high sink, available for GPCDXXXXA series
IOB0~IOB7	I/O	Bi-directional IO ports, can be wakeup pins	IOB0~3 high sink, available for GPCDXXXXA series
IOC0~IOC7	I/O	Bi-directional IO ports, can be wakeup pins	Available for GPCDX340A/300A/270A/220A
IOD0~IOD7	I/O	Bi-directional IO ports, can be wakeup pins	Available for GPCDX340A/300A/270A/220A/170A/130A
Clock related			
XO	O	Oscillator crystal output	
XI	I	Oscillator crystal input/R_{OSC} input	
POWER PAD			
VDD_REG	P	Positive supply for regulator (2.1/2.3~5.5V)	Working voltage refers to “GPCDXXXXA Family and Feature List” in page-5
VDD_DAC1	P	Positive supply for amplifier (2.1/2.3~5.5V)	Working voltage refers to “GPCDXXXXA Family and Feature List” in page-5
VDD_DAC2	P	Positive supply for DAC (2.1/2.3~5.5V)	Working voltage refers to “GPCDXXXXA Family and Feature List” in page-5
VDD_IO1	P	Positive supply for IOB,IOC (2.1/2.3~5.5V)	Working voltage refers to “GPCDXXXXA Family and Feature List” in page-5
VDD_IO2	P	Positive supply for IOA,IOD (2.1/2.3~5.5V)	Working voltage refers to “GPCDXXXXA Family and Feature List” in page-5
VDD	P	Core power from regulator and recommended connect it to VDD33 via PCB	It is not allowed for external components power source. Short to VDD33 internally.
VDD33	P	Core power output from regulator	It is not allowed for external components power source. Short to VDD internally.
VSS_REG	G	Ground reference for regulator	
VSS	G	Ground reference for GPIO and core circuit	
VSS_DAC1~2	G	Ground reference for amplifier	X2
VSS_DAC3	G	Ground reference for DAC	
Others			
RESETB	I	External reset pin(active low)	Internal pull-high
TEST	I	For test mode, NC for normal application	Internal pull-low
AUDP	O	Audio output of push-pull DAC	
AUDN	O	Audio output of push-pull DAC	

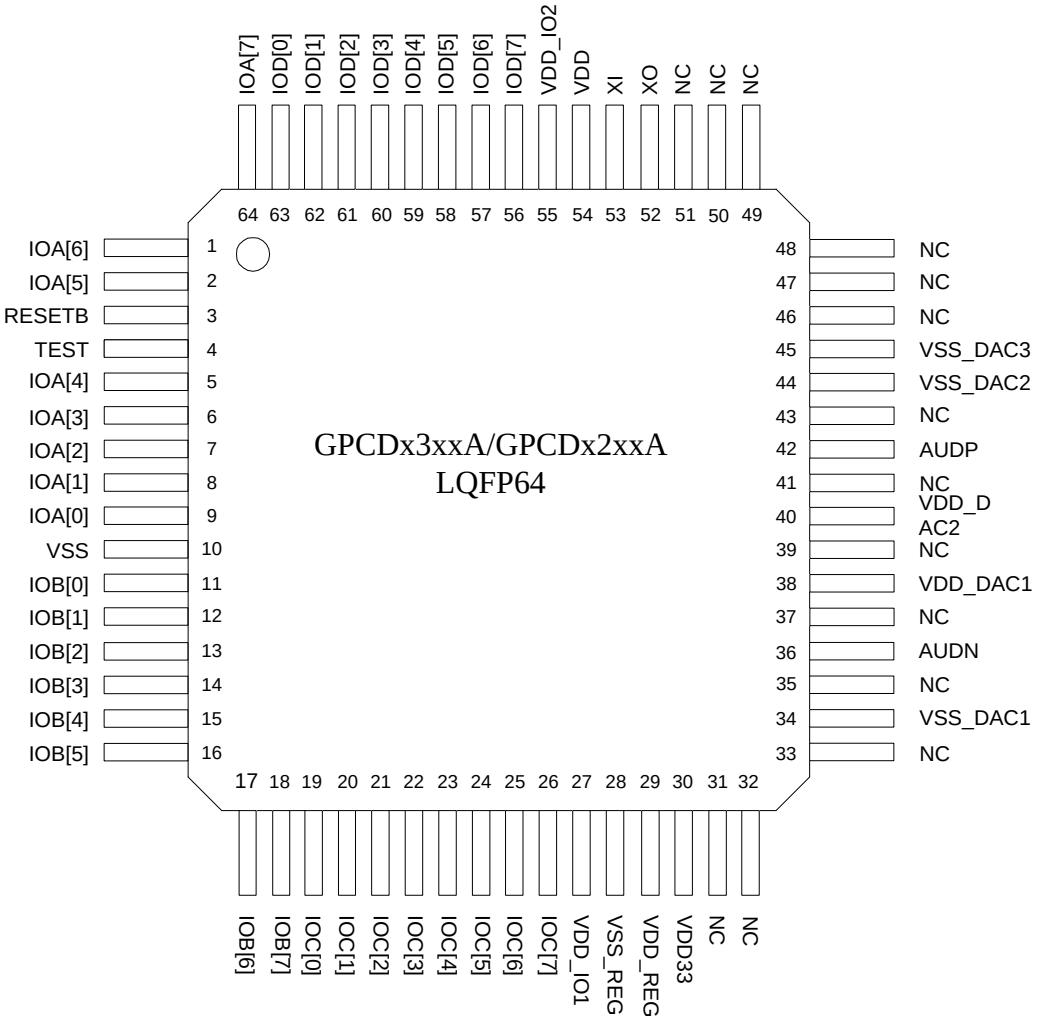
***Note: (1) VDD pad is recommended to be bonded for stability issue even VDD33 is shorted to VDD internally.**

(2) IO special function and allocation please refer to 7.6.1 IO configuration.

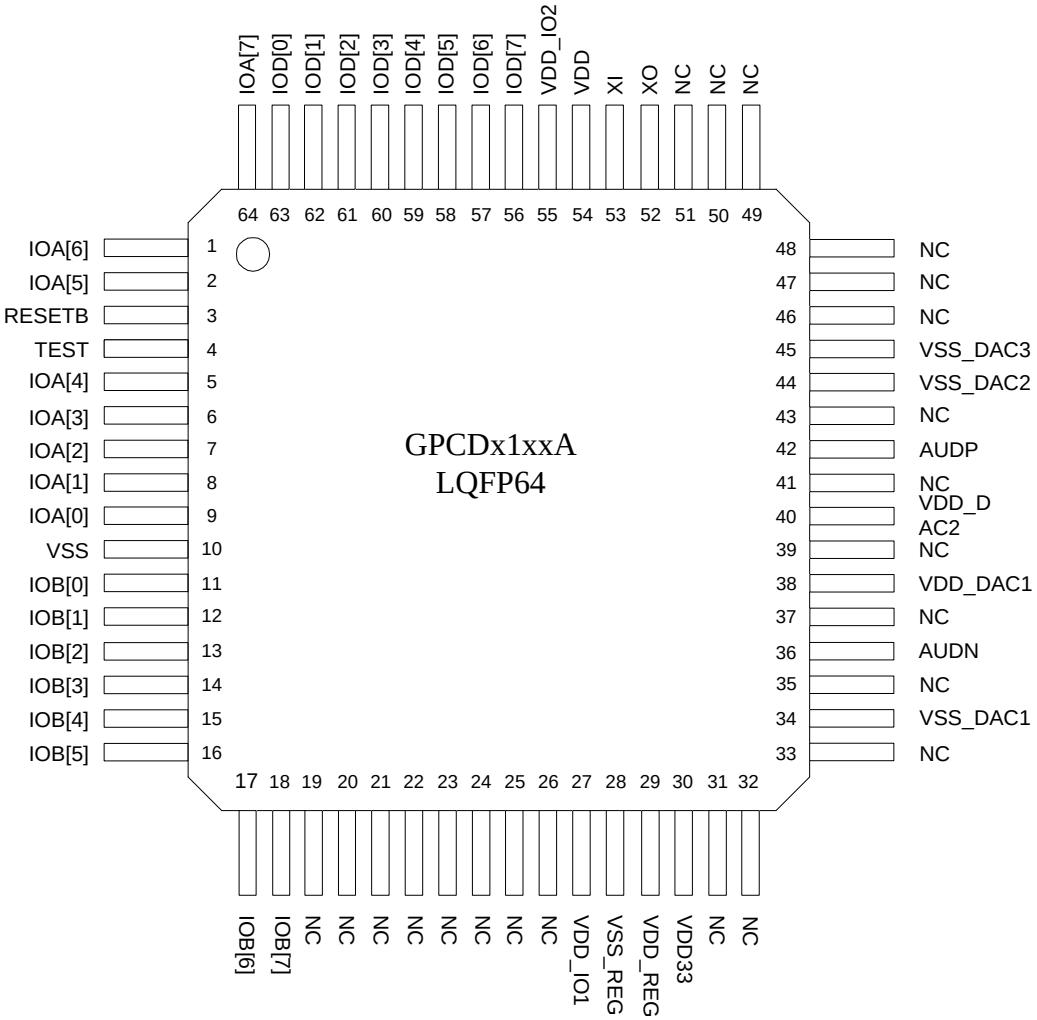
(3) For more details about pad information, please refer to respective “Pad Assignment and Locations” document of GPCDXXXXA series.

(4) VDD33 and VDD are dedicated to GPCDXXXXA internal circuits, external component power source not allowed.

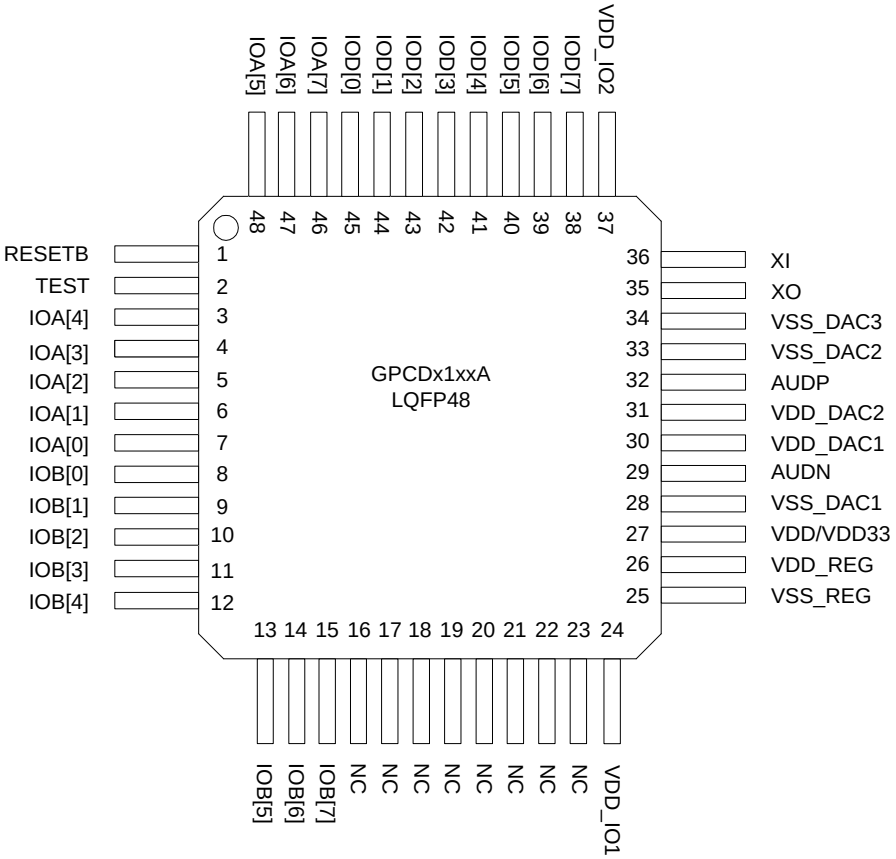
6.2. LQFP64 Package Pin Assignment for GPCDX3XXA & GPCDX2XXA



6.3. LQFP64 Package Pin Assignment for GPCDX1XXA



6.4. LQFP48 Package Pin Assignment for GPCDX1XXA



7. FUNCTIONAL DESCRIPTIONS

7.1. SRAM

The 512-byte SRAM (including Stack) area is located in $000000~$0002FF.

7.2. ROM

GPCDXXXXA is capable of accessing internal ROM. The ROM size for various bodies are indicated in following table:

Body	ROM Size	ROM Address
GPCD9/6/3340A	1MB	0x00840~0xFFFFF
GPCD9/6300A	912KB	0x00840~0xE3FFF
GPCD9/6/3270A	832KB	0x00840~0xCFFFF
GPCD9/6220A	672KB	0x00840~0xA7FFF
GPCD9/6/3170A	512KB	0x00840~0x7FFFF
GPCD9/6/3130A	416KB	0x00840~0x67FFF
GPCD9/6/3080A	256KB	0x00840~0x3FFFF
GPCD9/6/3040A	128KB	0x00840~0x1FFFF

7.3. Low Voltage Reset

The GPCDXXXXA provides another important feature - Low Voltage Reset (LVR). With the LVR function, a reset signal is generated to reset system when the operating voltage drops below LVR. Without LVR, the CPU becomes unstable and malfunction when working voltage is extremely low.

7.4. Interrupt

The GPCDXXXXA has two interrupt (INT) modes: IRQ (interrupt Request) and NMI (Non-Mask Interrupt Request). The interrupt controller controls fifteen IRQs and seven NMIs. A NMI cannot be interrupted by any other IRQs.

Interrupt Source	Interrupt Name	Priority
Timer A	NMI_TIMER_A	NMI
Timer B	NMI_TIMER_B	NMI
Timer C	NMI_TIMER_C	NMI
CPU_CLOCK/1024	NMI_D1024	NMI
CPU_CLOCK/4096	NMI_D4096	NMI
KEY	NMI_KEY	NMI
EXT	NMI_EXT	NMI
TIMER A	IRQ_TIMER_A	IRQ1
TIMER B	IRQ_TIMER_B	IRQ2
TIMER C	IRQ_TIMER_C	IRQ3
CPU_CLOCK/1024	IRQ_D1024	IRQ4
CPU_CLOCK/4096	IRQ_D4096	IRQ5
16 Hz	IRQ_16Hz	IRQ6
2 Hz	IRQ_2 Hz	IRQ7
KEY	IRQ_KEY	IRQ8
EXT	IRQ_EXT	IRQ9
SPU	IRQ_SPU	IRQ10
SPI *	IRQ_SPI	IRQ11
QD1_F	IRQ_QD1_F	IRQ12
QD1_B	IRQ_QD1_B	IRQ13
QD2_F	IRQ_QD2_F	IRQ14
QD2_B	IRQ_QD2_B	IRQ15

***Note:** SPI interrupt is not available for GPCDX080A/040A series.

7.5. Hardware PWMIO

Hardware PWMIO supports four LED outputs from IOB0~3 with brightness control of 256 levels. The clock source of PWMIO can be selected by user's request.

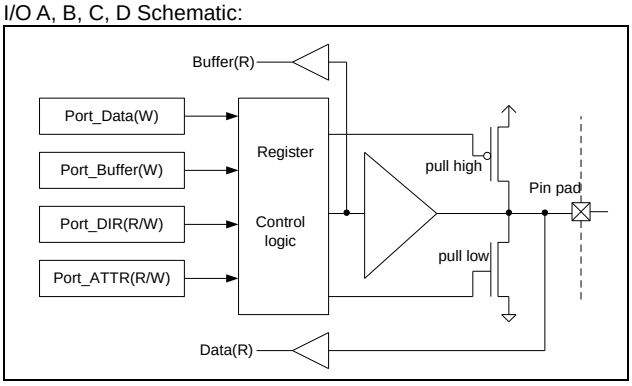
7.6. I/O

The purpose of input and output port is mainly to communicate with other devices or components. Maximum 32 programmable I/O ports are built in GPCDXXXXA series, including Port A, Port B, Port C, and Port D (by body option). All ports are general I/Os with programmable wake-up capability and 1M-Ohm pull-low function. In addition, these ports also provide some special functions in certain pins. PortA0~3 and PortB0~3 supports large sink current for LED application. The Port D0~3 is sharing with SPI function (by body option). Please refer to following figure for **IO Sharing**.

7.6.1. I/O Configuration

The following diagram is the I/O schematic.

I/O A, B, C, D Schematic:



Port_Data and Port_Buffer are written into the same register but reading from different node. To activate key wakeup function, user should latch data on IOX_Data and enable the key wakeup function. Wakeup is triggered when the state of port is different from that of latched data.

A summary of IO sharing is listed as following.

IO Sharing

	IOA								IOB							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Wake up	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
High sink					V	V	V	V					V	V	V	V
PWMIO													V	V	V	V
IR(Output)									V							
External INT										V						
External Clock		V(TMC)	V(TMB)	V(TMA)												
RTC											V	V				
IIS out/in	V(in)	V(in)	V(in)			V(out)	V(out)	V(out)								
QD					V(qd2)	V(qd2)	V(qd1)	V(qd1)								
CC		TMC	TMB	TMA						TMC	TMB	TMA				
1M pull low	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V

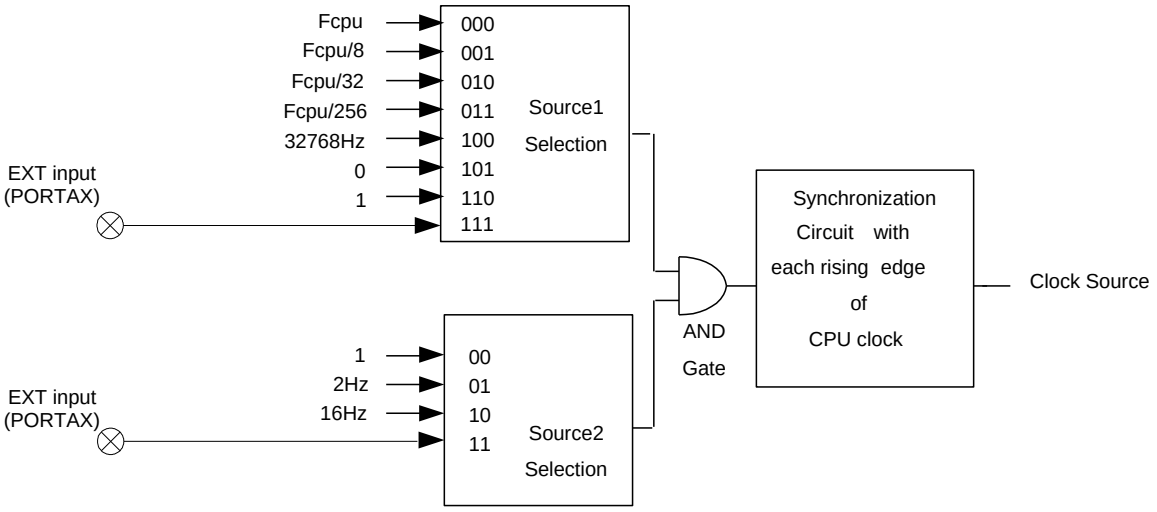
	IOC								IOD							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Wake up	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
SPI													V(rx)	V(tx)	V(ck)	V(cs)
1M pull low	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V

***Note: (1) QD means quadrature decoder; CC means Capture/Comparison.**

(2) IOC is available for GPCDX340A/300A/270A/220A. IOD is available for GPCDX340A/300A/270A/220A/170A/130A.

7.7. Timer/Counter (Timer A/Timer B/Timer C)

Three 12-bit timers are embedded in GPCDXXXXA: Timer A, Timer B and Timer C. These timers all have a 12-bit up counter, a preloaded register, and variety of programmable clock sources. Timer A/B can also be the clock source of the software channel 1/2 respectively. The clock source of each timer can be set individually. Two clock sources including CPU clock and external clock can be selected respectively or combination to be timer's clock source. Furthermore, capture and comparison functions are supported by TMA and in contrast, only comparison is supported by TMB and TMC.



7.8. Sleep, Wakeup and Watchdog

7.8.1. Sleep and Wakeup

Sleep mode saves power by stopping clock while device is not in operating. When entering into sleep mode, the device runs from operating mode to standby mode. Wake-up from sleep mode returns system back to operating mode.

1). Sleep: After power-on reset, CPU starts operating until a sleep command is given. When a sleep signal is accepted, CPU will turn off system clock and enter into sleep mode.

2). Wake-up: while an IRQ/NMI interrupt signal is generated, GPCDXXXXA awakes from sleep mode. While wake-up is completed, program counter will continue to execute the following commands.

7.8.2. Watchdog

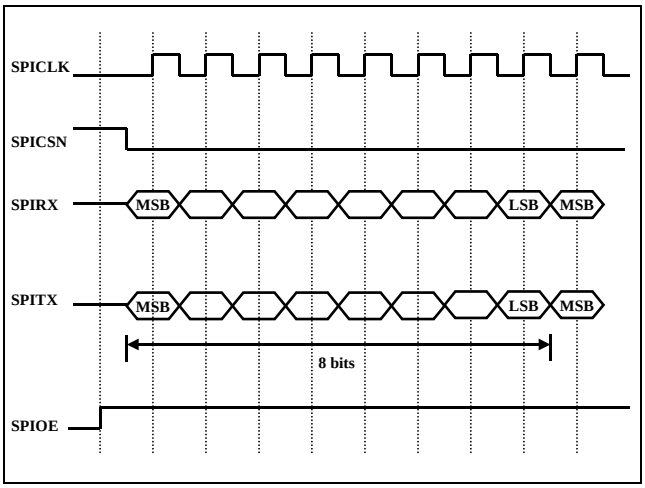
The purpose of watchdog is to monitor whether a system is operating normally. Within a certain period of time, watchdog must routinely be cleared. It prevents system from incorrect code execution by generating a system reset signal when software is failed to clear watchdog flag within 0.75 seconds. Watchdog function can be removed by option.

7.9. Speech and DAC

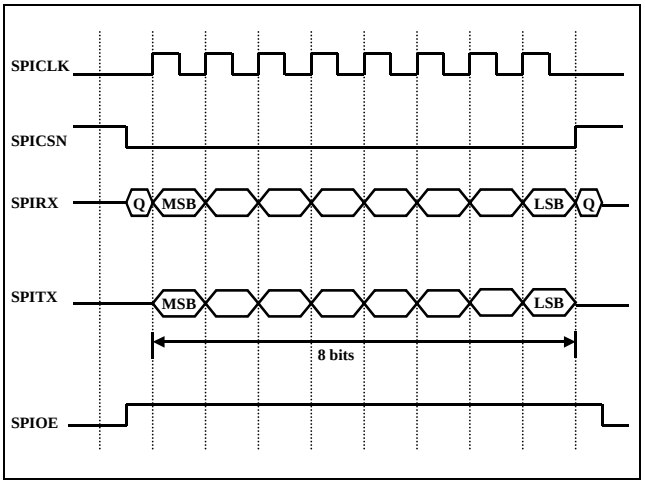
The GPCDXXXXA uses a high performance SPU voice engine to achieve 8/4/1-channel voice with ADPCM/PCM (by body). The SPU also supports automatic zero-crossing concatenate function. A hardware multiplier is also embedded in this SPU for software usage. The fixed address of RAM area $0000 - $007F/3F/0F is designed as address pointers and a data buffer for the 8/4/1-channel speech/melody generation. Moreover, up to two sets of 14-bit software channel with noise filter are equipped. There is one 14-bit DAC with push-pull amplifier for direct audio output.

7.10. SPI Controller

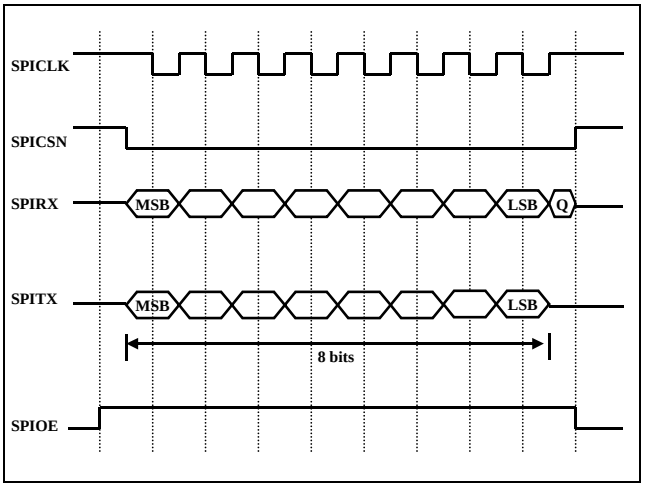
A Serial Peripheral Interface (SPI) controller is a significant feature to facilitate communication tasks with other devices and components. The SPI requires four control signals which includes SPICSN, SPICLK (SCK), SPITX (SDO), and SPIRX (SDI); these four signals are shared with IO ports: PortD0, PortD1, PortD2 and PortD3. While SPI module is enabled by respective control bits. These four pins cannot be GPIOs and any setting on corresponding GPIO control register will have no effect. Four types of timing are presented as follows:



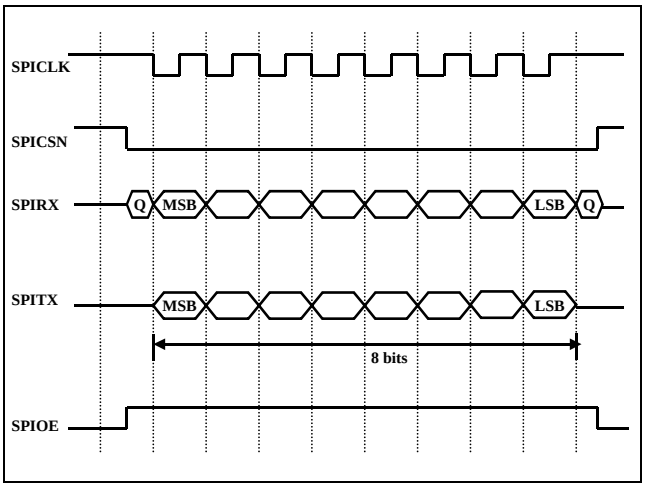
Master Mode, SPO = 0, SPH=0



Master Mode, SPO = 0, SPH=1



Master Mode, SPO = 1, SPH=0

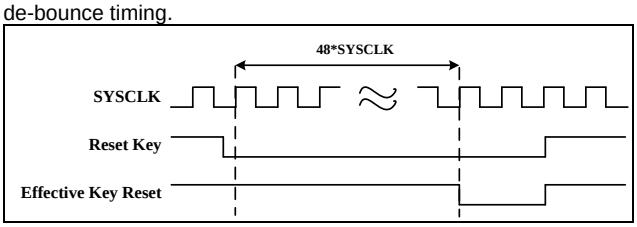


Master Mode, SPO = 1, SPH=1

***Note:** SPI is not available for GPCDX080A/040A series.

7.11. Reset Key De-bounce

For system stability, reset key de-bounce time for GPCDXXXXA is 48 system clocks. Please refer to the following diagram for de-bounce timing.



8. ELECTRICAL SPECIFICATIONS

8.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions, see DC Electrical Characteristics.

8.2. DC Characteristics (VDD_IO/VDD_REG=3.0V, TA=25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	***2.1 / 2.3****	-	3.6	V	For 2-battery
Operating Current-1	I_{OP1}	-	9	-	mA	VDD_IO/VDD_ADC/VDD_REG=3.0V F_{CPU} = 8MHz , DAC on, no load
Operating Current-2	I_{OP2}	-	6	-	mA	VDD_IO/VDD_ADC/VDD_REG=3.0V F_{CPU} = 8MHz , DAC off, no load
Standby Current	I_{STBY}	-	-	3	μA	VDD_IO/VDD_ADC/VDD_REG=3.0V
OSC Frequency	F_{OSC}	-	-	16	MHz	VDD_IO/VDD_ADC/VDD_REG=3.0V
Input High Level	V_{IH}	0.7*VDD	-	-	V	-
Input Low Level	V_{IL}	-	-	0.3*VDD	V	-
Output High Current (IOA/B/C/D[7:0])	I_{OH}	-	5	-	mA	VDD_IO/VDD_ADC/VDD_REG=3.0V, V_{OH} =2.1V
Output Low Sink Current (IOA/B[7:4], IOC/D[7:0])	I_{OL1}	-	10	-	mA	VDD_IO/VDD_ADC/VDD_REG=3.0V, V_{OL} =0.9V
Output Low Sink Current (IOA/B[3:0])	I_{OL2}	-	19	-	mA	VDD_IO/VDD_ADC/VDD_REG=3.0V, V_{OL} =0.9V
Input Pull-Low Resistor (IOA/B/C/D[7:0])	R_{PL}	-	1400	-	Kohm	VDD_IO/VDD_ADC/VDD_REG=3.0V, Vin=3.0V
Input Pull-High Resistor (IOA/B/C/D[7:0])	R_{PH}	-	155	-	Kohm	VDD_IO/VDD_ADC/VDD_REG=3.0V, Vin=VSS

***Note:** (1) VDD min. for GPCDX340A/300A/270A/220A is 2.3V, VDD min. for GPCDX170A/130A/080A/040A is 2.1V.

8.3. DC Characteristics (VDD_IO/VDD_REG=4.5V, TA=25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current-1	I_{OP1}	-	11	-	mA	VDD_IO/VDD_ADC/VDD_REG=4.5V F_{CPU} = 8MHz , DAC on, no load
Operating Current-2	I_{OP2}	-	7	-	mA	VDD_IO/VDD_ADC/VDD_REG=4.5V F_{CPU} = 8MHz , DAC off, no load
Standby Current	I_{STBY}	-	-	4	μA	VDD_IO/VDD_ADC/VDD_REG=4.5V
OSC Frequency	F_{OSC}	-	-	16	MHz	VDD_IO/VDD_ADC/VDD_REG=4.5V
Input High Level	V_{IH}	0.7*VDD	-	-	V	-
Input Low Level	V_{IL}	-	-	0.3*VDD	V	-

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Output High Current (IOA/B/C/D[7:0])	I_{OH}	-	11	-	mA	VDD_IO/VDD_ADC/VDD_REG=4.5V, V_{OH} =3.15V
Output Low Sink Current (IOA/B[7:4], IOC/D[7:0])	I_{OL1}	-	18	-	mA	VDD_IO/VDD_ADC/VDD_REG=4.5V, V_{OL} =1.35V
Output Low Sink Current (IOA/B[3:0])	I_{OL2}	-	35	-	mA	VDD_IO/VDD_ADC/VDD_REG=4.5V, V_{OL} =1.35V
Input Pull-Low Resistor (IOA/B/C/D[7:0])	R_{PL}	-	865	-	Kohm	VDD_IO/VDD_ADC/VDD_REG=4.5V, Vin=4.5V
Input Pull-High Resistor (IOA/B/C/D[7:0])	R_{PH}	-	97	-	Kohm	VDD_IO/VDD_ADC/VDD_REG=4.5V, Vin=VSS

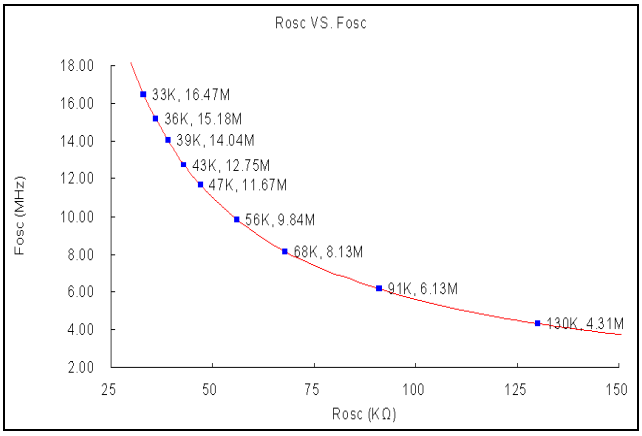
8.4. DAC Characteristics (VDD_IO/VDD_REG/VDD_DAC=4.5V, R_L=8Ω, f=1KHz, TA=25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
DAC Resolution	RESO	-	-	14	bit
THD+n (4.5V@0.45W)	-	-	0.4	-	%
Noise at No Signal	-	-	-97	-	dBr A
Dynamic Range (-60dB)	-	-	-80	-	dBr A

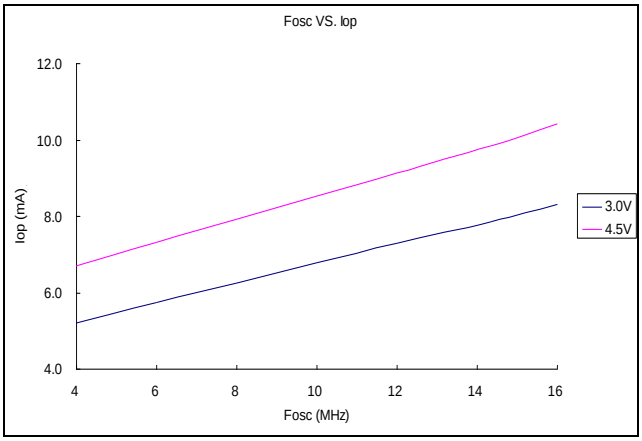
8.5. Regulator Characteristics (TA=25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	2.1	4.5	5.5	V
Maximum Current Output	IREGO	-	-	30	mA
Output Voltage	VREGO	2.1	3.3	3.6	V
Standby Current	IREGS	-	-	2.0	uA

8.6. The Relationship between R_{OSC} and F_{OSC} (TA=25℃)

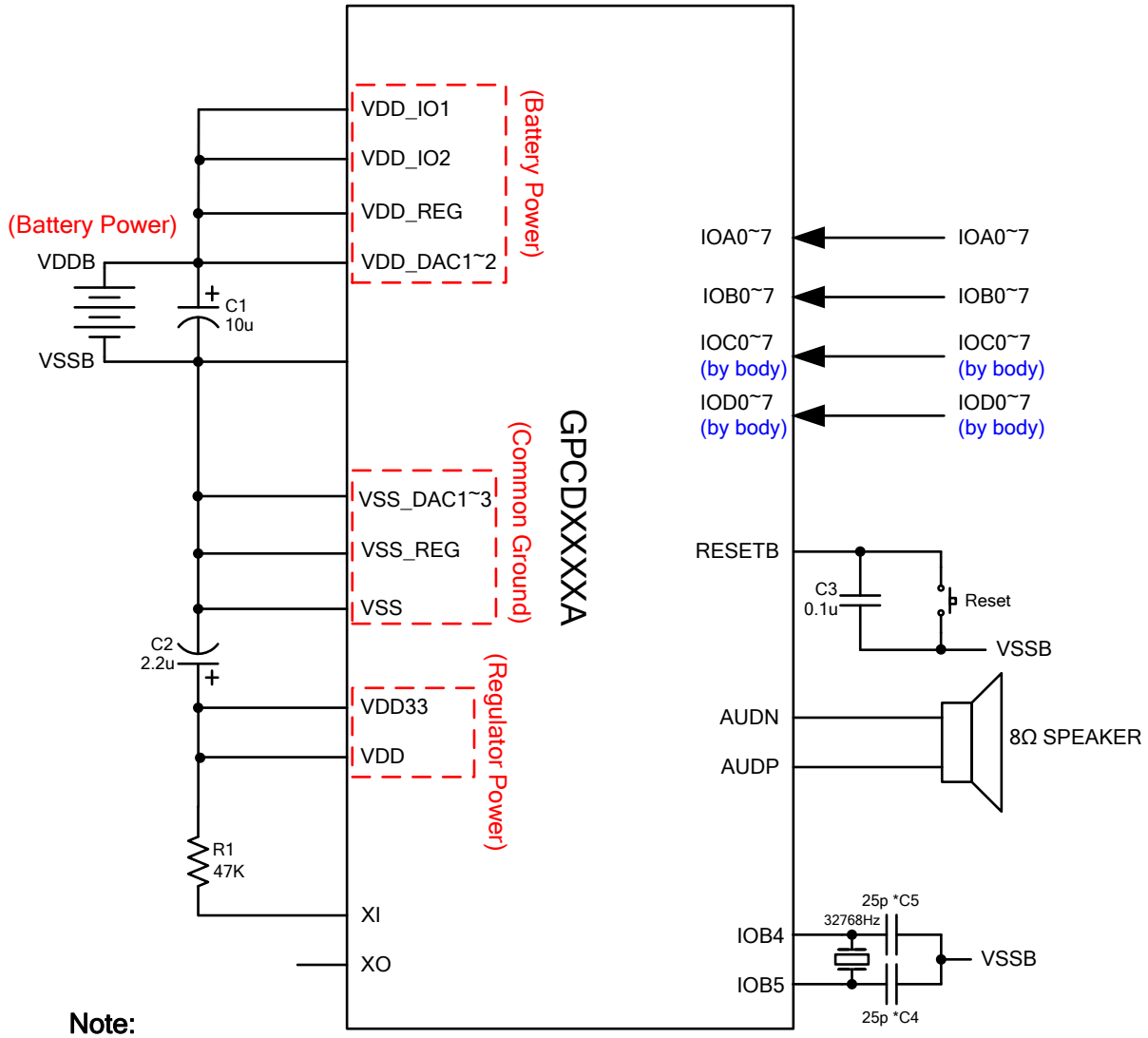


8.7. The Relationship between F_{OSC} and I_{OP} (TA=25℃)



9.APPLICATION CIRCUITS

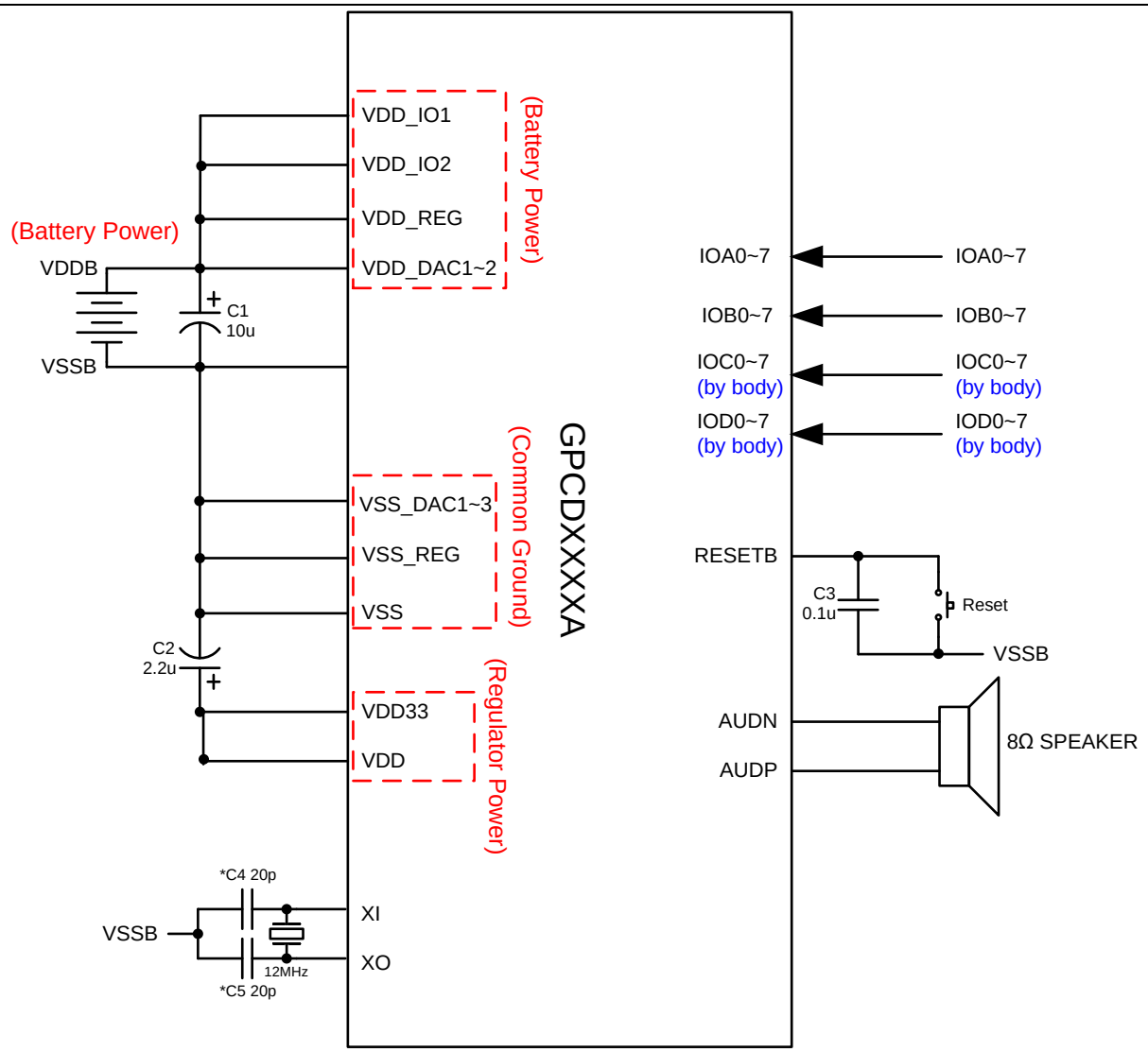
9.1. GPCDXXXXA Application Circuit with 32K Crystal Mode and without IO Output Driving Application(R_{OSC}-mode)



Note:

1. 4Ω speaker application is not allowed in GPCDXXXXA.
2. Above illustration only suggested for no IO heavy driving output, such as only key input trigger and no LED or motor driver output.
3. C1/C2 value may vary with system application.
4. If system is not stable, it is suggested to refer to following 9.3~9.6 circuits.
5. C4/C5 values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~60K and CL1=CL2 =26~36pF (including PCB parasitic loading, for example, user should apply additional 20~30pF on X32I and X32O if PCB parasitic loading is 6pF)

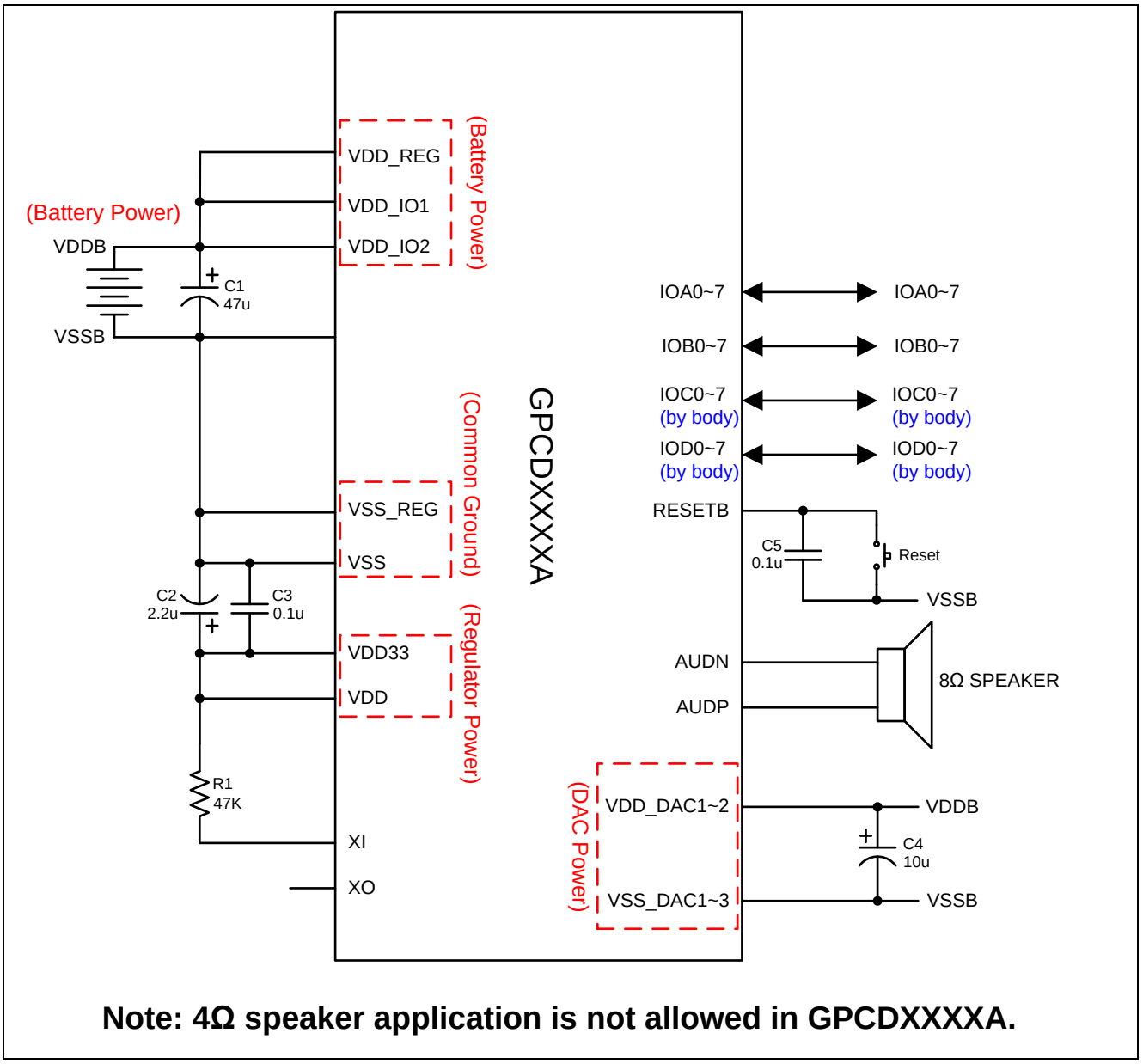
9.2. GPCDXXXXA Application Circuit without IO Output Driving Application(XTAL-mode)



Note:

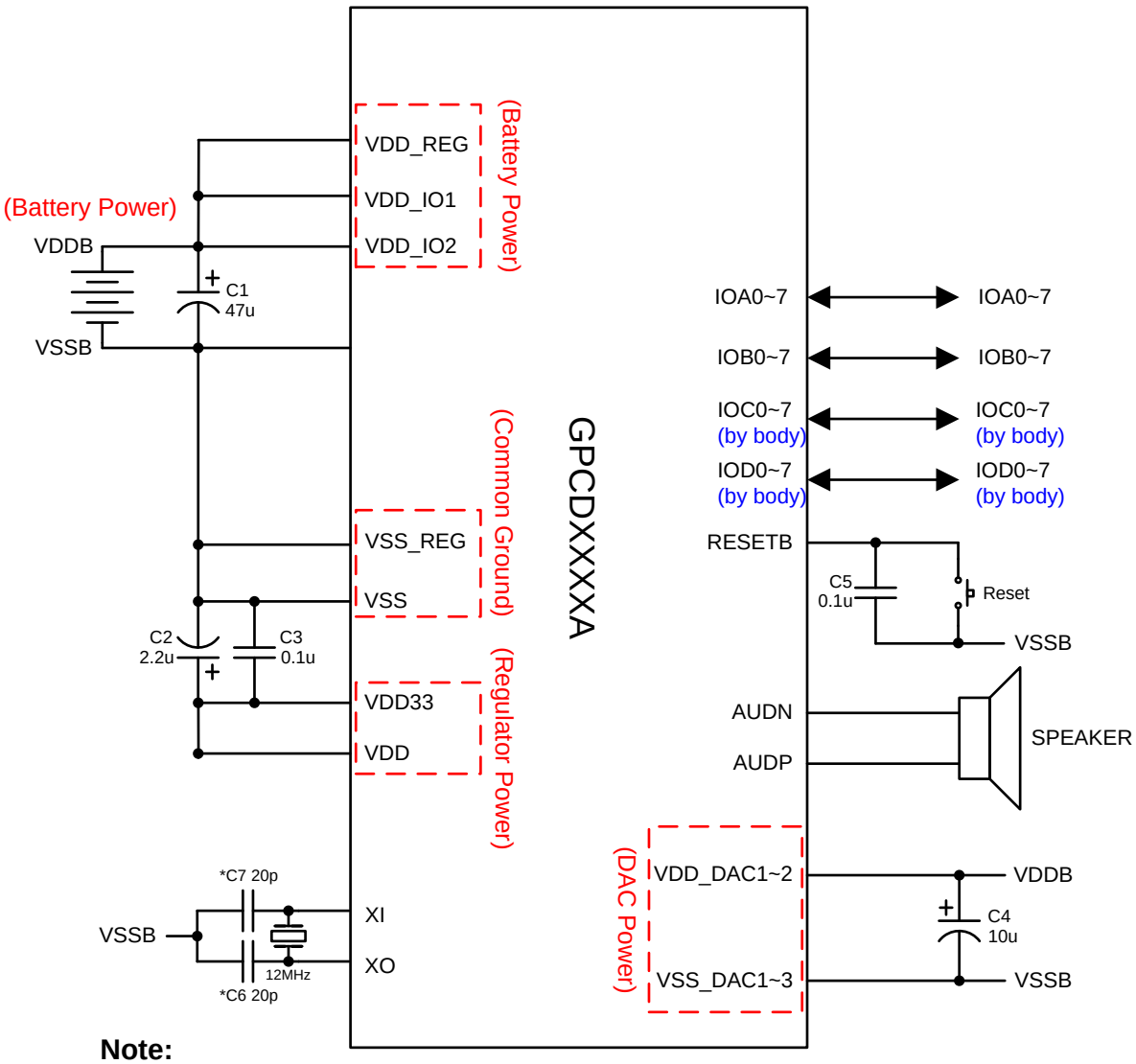
1. **4Ω speaker application is not allowed in GPCDXXXXA.**
2. **Above illustration only suggested for no IO heavy driving output, such as only key input trigger and no LED or motor driver output.**
3. **C1/C2 value may vary with system application.**
4. **If system is not stable, it is suggested to refer to following 9.3~9.6 circuits.**
5. **The values of C4/C5 are for design guidance only, different values may be needed for different crystal/resonator used.**

9.3. GPCDXXXXA Application Circuit with R_{osc} Option



Note: 4Ω speaker application is not allowed in GPCDXXXXA.

9.4. GPCDXXXXA Application Circuit with Crystal Option

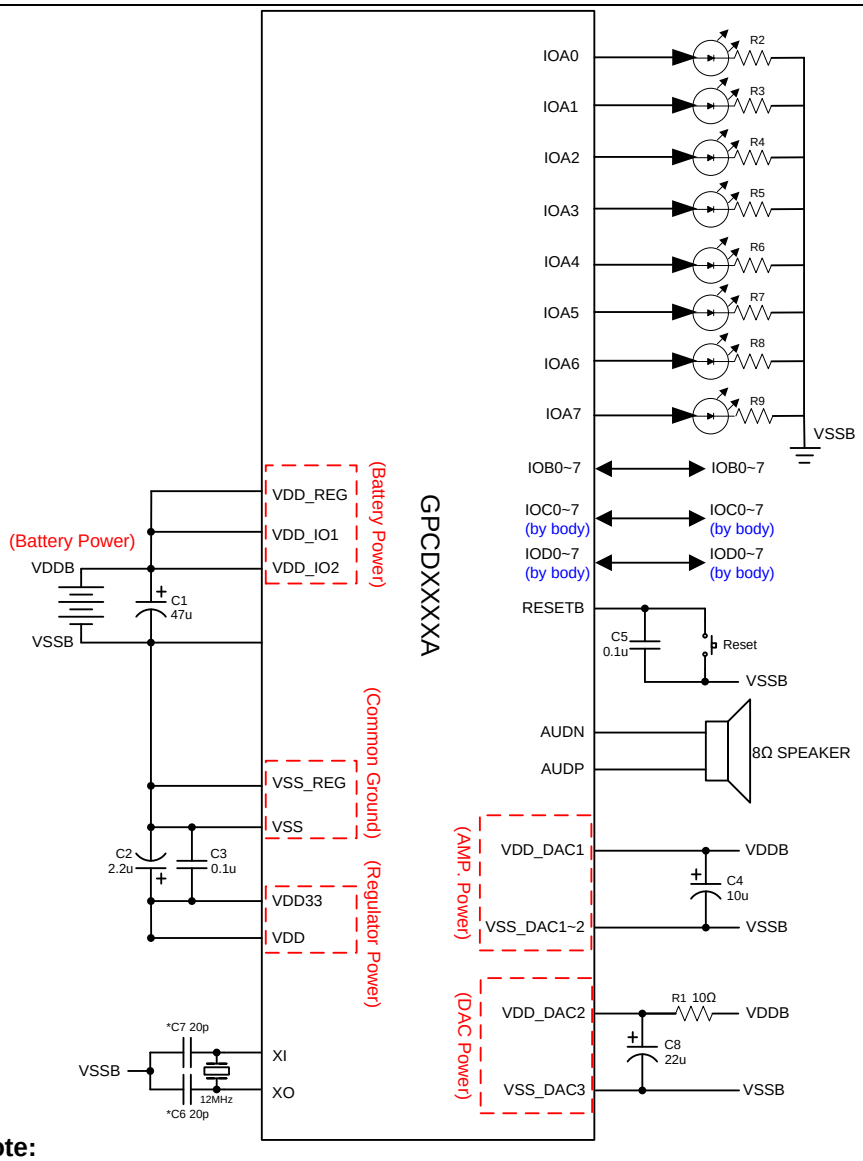


Note:

1. 4Ω speaker application is not allowed in GPCDXXXXA.

2. The values of C6/C7 are for design guidance only, different values may be needed for different crystal/resonator used.

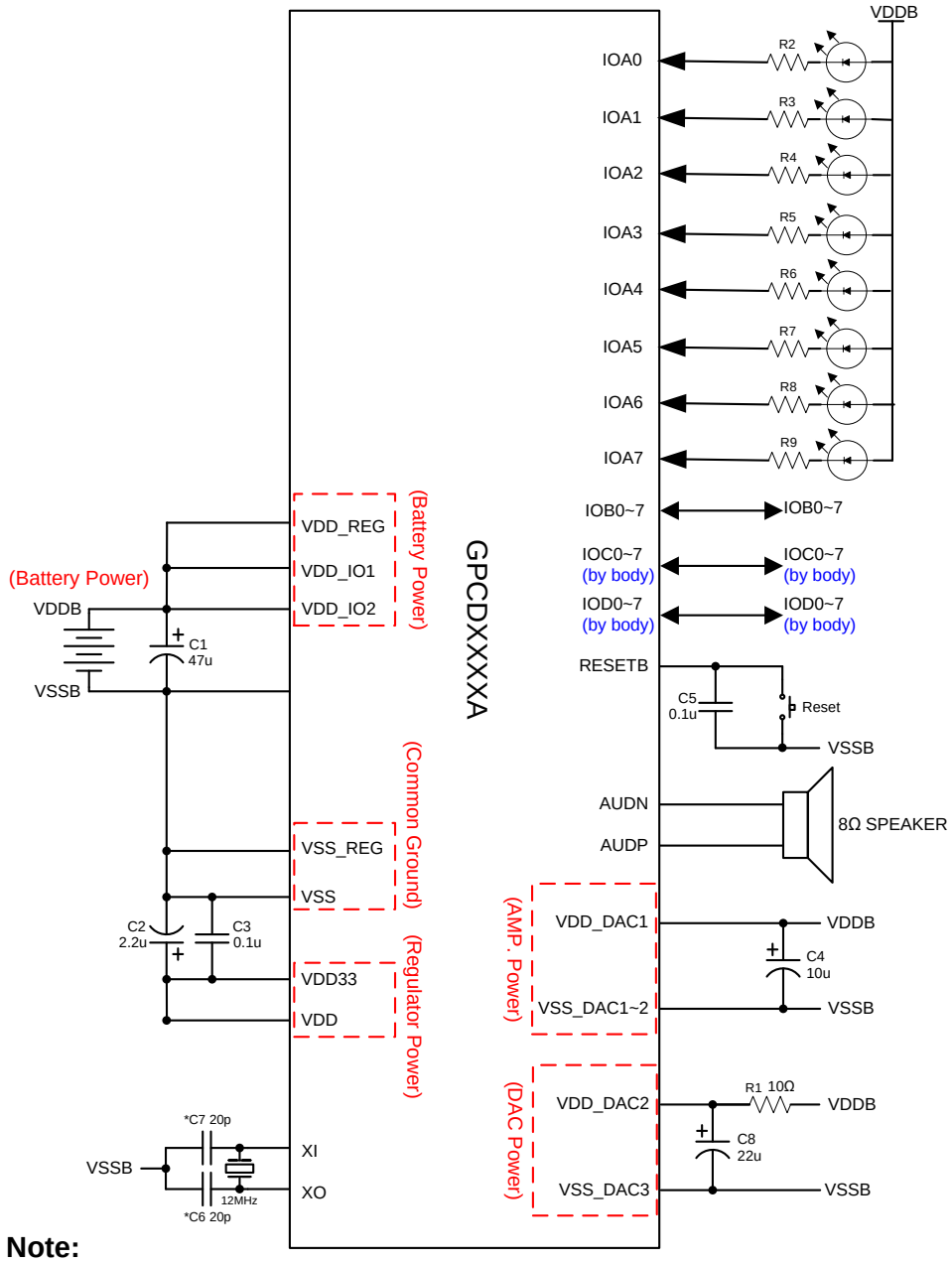
9.5. GPCDXXXXA Application Circuit with IO Heavy Loading(1):High Sourcing



Note:

1. **4Ω speaker application is not allowed in GPCDXXXXA.**
2. **For system stability and performance, it is recommended to add R1/C8 for the applications that IOs toggle with high current sourcing, such as LEDs or motor drivers.**
3. **The value of R2~R9/C8 depends on applications. Basically, the more IO toggles, the larger C8 is suggested.**
4. **The values of C6/C7 are for design guidance only, different values may be needed for different crystal/resonator used.**

9.6. GPCDXXXXA Application Circuit with IO Heavy Loading(2):High Sinking



Note:

1. **4Ω speaker application is not allowed in GPCDXXXXA.**
2. **For system stability and performance, it is recommended to add R1~R9/C8 for the applications that IOs toggle with high current sinking, such as LEDs or motor drivers.**
3. **The value of R2~R9/C8 depends on the system application.**
4. **Basically, the more IO toggles, the larger C8 is suggested.**
5. **The values of C6/C7 are for design guidance only, different values may be needed for different crystal/resonator used.**

10. PACKAGE

10.1. Ordering Information

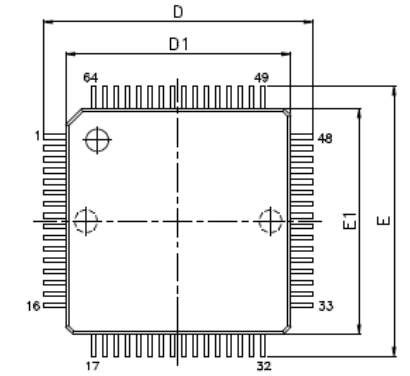
Product Number	Package Type
GPCD3040A-NnnV-C	Chip form
GPCD3080A-NnnV-C	Chip form
GPCD3130A-NnnV- QL02x	Green Package – LQFP64
GPCD3130A-NnnV- QL01x	Green Package – LQFP48
GPCD3170A-NnnV- QL02x	Green Package – LQFP64
GPCD3170A-NnnV- QL01x	Green Package – LQFP48
GPCD3270A-NnnV- QL02x	Green Package – LQFP64
GPCD3340A-NnnV- QL02x	Green Package – LQFP64
GPCD6040A-NnnV-C	Chip form
GPCD6080A-NnnV-C	Chip form
GPCD6130A-NnnV- QL02x	Green Package – LQFP64
GPCD6130A-NnnV- QL01x	Green Package – LQFP48
GPCD6220A-NnnV- QL02x	Green Package – LQFP64
GPCD6300A-NnnV- QL02x	Green Package – LQFP64
GPCD6170A-NnnV- QL02x	Green Package – LQFP64
GPCD6170A-NnnV- QL01x	Green Package – LQFP48
GPCD6270A-NnnV- QL02x	Green Package – LQFP64
GPCD6340A-NnnV- QL02x	Green Package – LQFP64
GPCD9040A-NnnV-C	Chip form
GPCD9080A-NnnV-C	Chip form
GPCD9130A-NnnV- QL02x	Green Package – LQFP64
GPCD9130A-NnnV- QL01x	Green Package – LQFP48
GPCD9220A-NnnV- QL02x	Green Package – LQFP64
GPCD9300A-NnnV- QL02x	Green Package – LQFP64
GPCD9170A-NnnV-QL02x	Green Package – LQFP64
GPCD9170A-NnnV-QL01x	Green Package – LQFP48
GPCD9270A-NnnV-QL02x	Green Package – LQFP64
GPCD9340A-NnnV-QL02x	Green Package – LQFP64

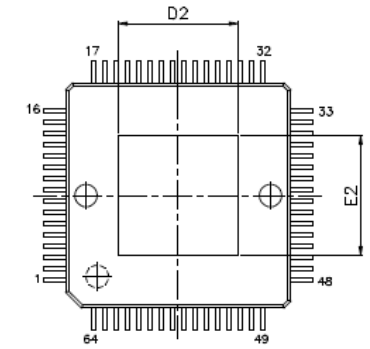
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

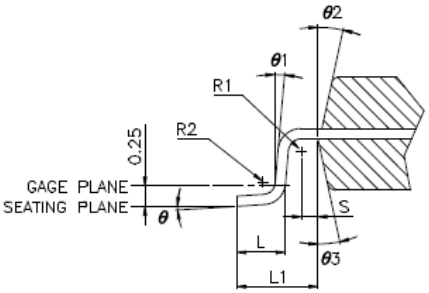
10.2. Package Information

10.2.1. LQFP 64 Outline Dimensions





(THERMALLY ENHANCED VARIATIONS ONLY)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

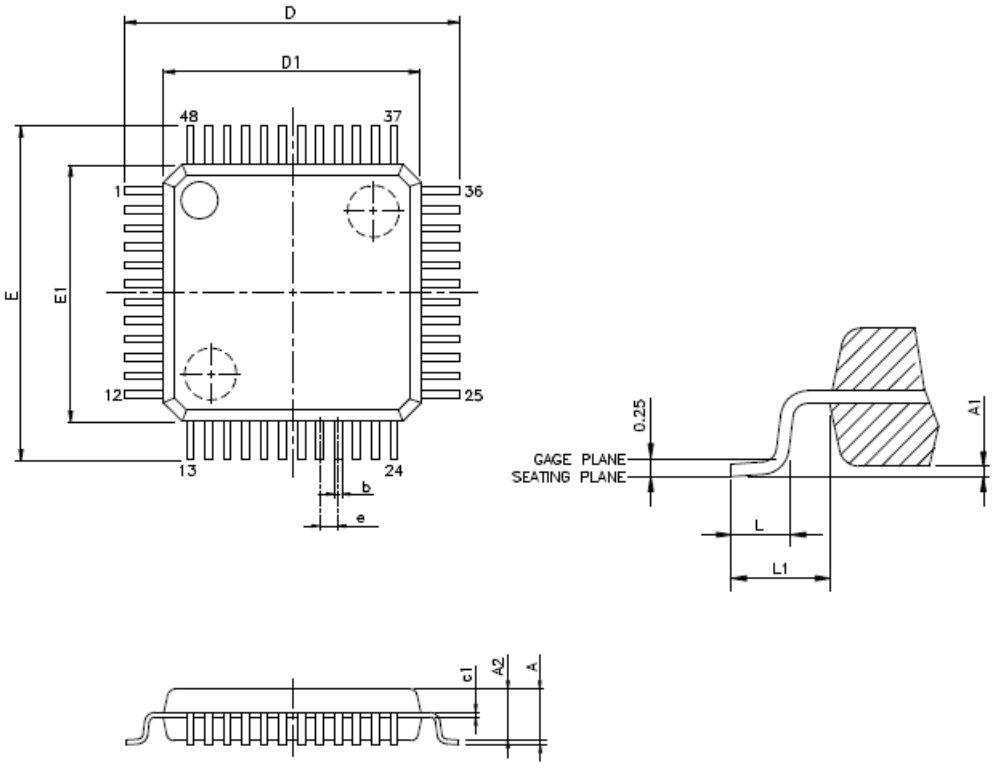
SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c1	0.09	–	0.16
D	11.75	12.00	12.25
D1	9.90	10.00	10.10
E	11.75	12.00	12.25
E1	9.90	10.00	10.10
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20 REF		
θ	3.5° REF		
θ1	5.0° REF		
θ2	12° REF		
θ3	12° REF		
R1	0.16 REF		
R2	0.15 REF		

5 THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2		D2	
	MIN.	MAX.	MIN.	MAX.
210X21E	4.27	5.33	4.27	5.33
260X26E	5.28	6.60	5.28	6.60

NOTES:
1. JEDEC OUTLINE :
   MS-026 BCD
   MS-026 BCD-HD(THERMALLY ENHANCED VARIATIONS ONLY)
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

10.2.2. LQFP 48 Outline Dimensions



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:

1. JEDEC OUTLINE:MS-026 BBC
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

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12. REVISION HISTORY

Date	Revision #	Description	Page
Jan. 18, 2017	1.5	Add LQFP64 pin assignment	7,8,9 22,23,24
OCT. 07, 2013	1.4	Modify 9.1 Application circuit	13
JUL. 26, 2013	1.3	Add LVD description and content update	
NOV. 10, 2011	1.2	Application circuit modify	13-14
SEP. 13, 2011	1.1	1. Modify working voltage in “GPCDXXXXA Family and Feature list” 2. Remove IOA0 auto-wakeup function in “IO configuration” 3. Add “Reset Key De-bounce” 4. Update “The Relationship between R_{OSC} and F_{OSC}”	4,6,7,12,13 9 11 13
FEB. 14, 2011	1.0	Original	21