

DATA SHEET



GPCE064A

16-bit Sound Controller With 32K X 16 ROM

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Version 1.3

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Table of Contents

PAGE

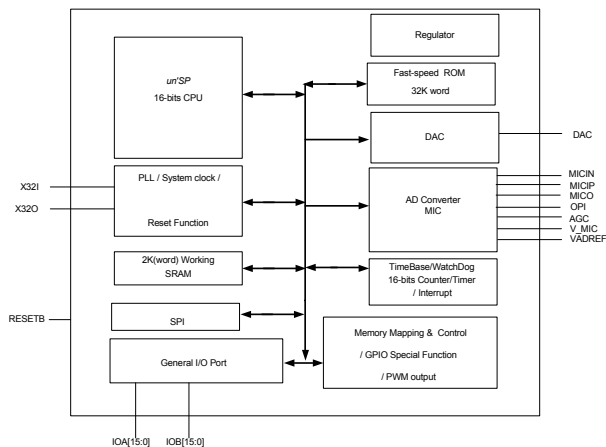
1. GENERAL DESCRIPTION	3
2. BLOCK DIAGRAM	3
3. FEATURES	3
4. APPLICATION FIELD	3
5. SIGNAL DESCRIPTIONS	4
5.1. PAD ASSIGNMENT	5
5.2. PIN MAP	6
6. FUNCTIONAL DESCRIPTIONS	7
6.1. CPU	7
6.2. MEMORY	7
6.3. PLL, CLOCK, POWER MODE	7
6.4. STANDBY MODE	7
6.5. LOW VOLTAGE DETECTION AND LOW VOLTAGE RESET	8
6.6. INTERRUPT	8
6.7. I/O	8
6.8. SPECIAL FUNCTION IN PORT	9
6.9. TIMER / COUNTER	10
6.10. SLEEP MODE, WAKEUP, HALT MODE, AND WATCHDOG	11
6.11. SOFT RESET PROTECTION	12
6.12. ADC (ANALOG TO DIGITAL CONVERTER) / DAC	12
6.13. SPI	12
6.14. AUDIO ALGORITHM	12
7. ELECTRICAL SPECIFICATIONS	13
7.1. ABSOLUTE MAXIMUM RATINGS	13
7.2. DC CHARACTERISTICS (VDD_REG = 3.3V, VDDIO = 4.5V (PORTA & B), T _A = 25°C)	13
7.3. DC CHARACTERISTICS (VDD_REG = 3.3V, VDDIO = 3.3V (PORTA & B), T _A = 25°C)	13
7.4. ADC CHARACTERISTICS (AVDD = 3.3V, T _A = 25°C)	14
7.5. DAC CHARACTERISTICS (AVDD = 3.3V, T _A = 25°C)	14
7.6. REGULATOR CHARACTERISTICS (T _A = 25°C)	15
7.7. PULL HIGH RESISTER AND VDDIO	15
7.8. PULL LOW RESISTER AND VDDIO(NORMAL PAD)	15
7.9. PULL LOW RESISTER AND VDDIO(IOB[7:0] PAD WITH INPUT HIGH)	15
7.10. I/O OUTPUT HIGH CURRENT I _{OH} AND VDDIO	15
7.11. I/O OUTPUT LOW CURRENT I _{OL} AND VDDIO(NORMAL PAD)	16
7.12. I/O OUTPUT LOW CURRENT I _{OL} AND VDDIO(HIGH DRIVING PAD)	16
7.13. DAC OUTPUT CURRENT I _{OL} AND AVDD	16
8. APPLICATION CIRCUITS	17
8.1. APPLICATION CIRCUIT-(1)	17
8.2. APPLICATION CIRCUIT-(2)	19
8.3. APPLICATION CIRCUIT-(3)	21
9. PACKAGE/PAD LOCATIONS	23
9.1. ORDERING INFORMATION	23
9.2. PACKAGE INFORMATION	23
10. DISCLAIMER	24
11. REVISION HISTORY	25

16-BIT SOUND CONTROLLER WITH 32K X 16 ROM

1. GENERAL DESCRIPTION

GPCE064A, a 16-bit architecture sound controller, features the newest 16-bit microprocessor, $\mu'nSP^{\text{TM}}$ (pronounced as *micro-n-SP*), developed by Sunplus Technology. This high processing speed assures the $\mu'nSP^{\text{TM}}$ is capable of handling complex digital signal processes easily and rapidly. Therefore, the GPCE064A is applicable to the areas of digital sound process and voice recognition. The operating voltage of 2.4V through 5.5V and speed of 0.16MHz through 49.152MHz yield the GPCE064A to be easily used in varieties of applications. The memory capacity includes 32K-word ROM plus a 2K-word working SRAM. Other features include 32 programmable multi-functional I/Os, three 16-bit timers/counters, 32768Hz Real Time Clock, Low Voltage Reset/Detection, eight channels 12-bit ADC (one channel built-in MIC amplifier with auto gain controller), 14-bit DAC output and many others.

2. BLOCK DIAGRAM



3. FEATURES

- 16-bit $\mu'nSP^{\text{TM}}$ microprocessor
- CPU Clock: 0.16MHz - 49.152MHz
- Operating Voltage: 2.4V - 5.5V
- Power regulator build-in with input voltage: 2.4~5.5V, output voltage: 2.4~3.3V
- Mask ROM Operating Voltage: 2.4V - 3.6V
- IO PortA & B Operating Voltage: 2.4V - 5.5V
- 32K-word fast speed ROM
- 2K-word working SRAM
- Software-based audio processing
- Standby mode for power saving
- Three 16-bit timers/counters
- One 14-bit DAC output
- 32 general I/Os (bit programmable)
- Key wakeup function (IOA0 - 15)
- PLL feature for system clock
- 32768Hz Real Time Clock (RTC)
- Eight channels 12-bit AD converter
- ADC external top reference voltage
- Built-in microphone amplifier and AGC function
- Low voltage reset and low voltage detection
- Watchdog Enable (option)
- One SPI serial interface I/O

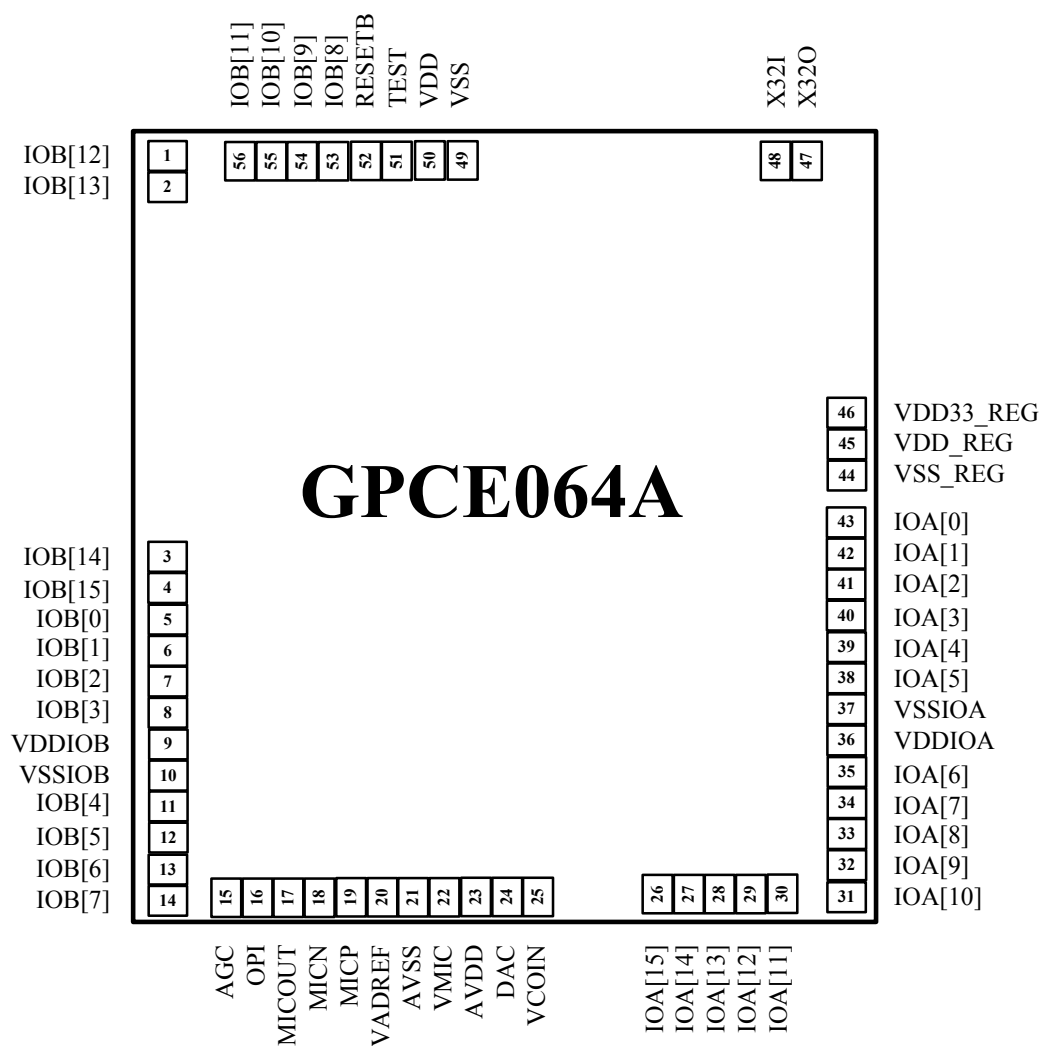
4. APPLICATION FIELD

- Voice Recognition Products
- Intelligent Interactive Talking Toys
- Advanced Educational Toys
- Kids Learning Products
- Kids Storybook
- General Speech Synthesizer
- Long Duration Audio Products
- Recording / Playback Products

5. SIGNAL DESCRIPTIONS

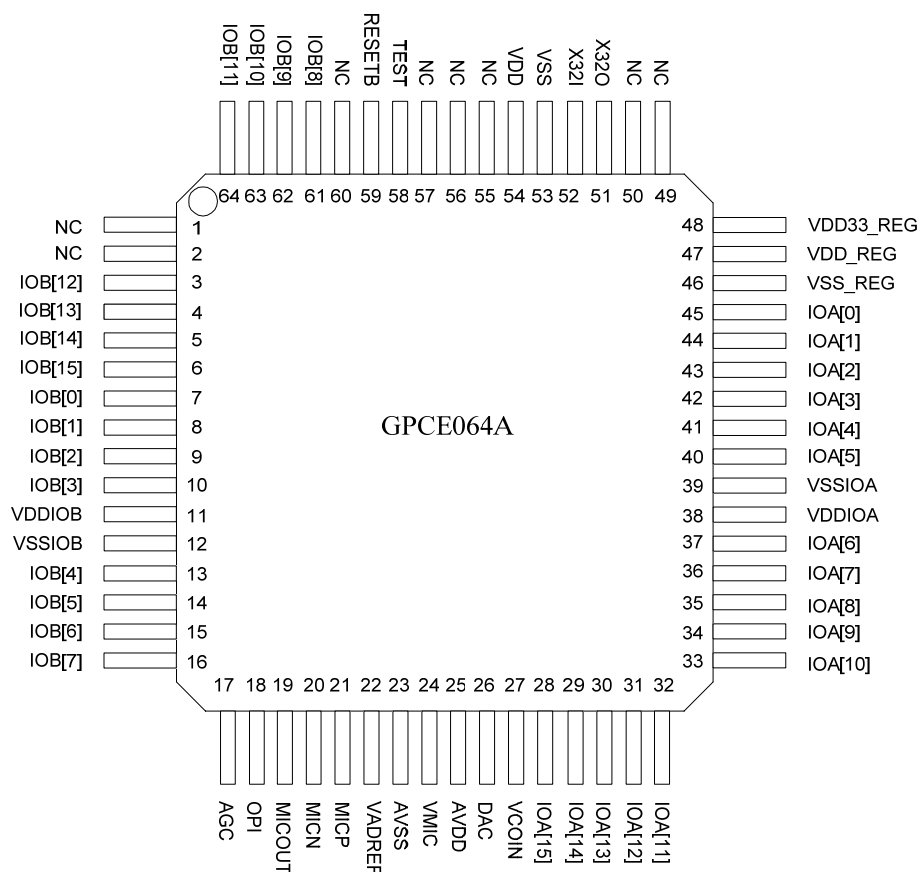
Mnemonic	PIN No.	LQFP 64 PIN No.	Type	Description
PORT A, Port B				
IOA[15:0]	26-35, 38-43	28-37, 40-45	I/O	IOA[15:0]: bi-directional I/O ports It can be programmed as wakeup I/O pins
IOB [15:0]	4-1, 56-53, 14-11, 8-5	6-3, 64-61, 16-13, 10-7	I/O	IOB [15:0]: bi-directional I/O ports
Power & GND				
VDDIOA	36	38	P	Power VDD for Port A
VSSIOA	37	39	G	Power GND for Port A
VDDIOB	9	11	P	Power VDD for Port B
VSSIOB	10	12	G	Power GND for Port B
AVDD	23	25	P	Power VDD for AD,DA + PLL(3.3V)
AVSS	21	23	G	Power GND for AD,DA + PLL
VDD	50	54	P	Power VDD for Core (3.3V)
VSS	49	53	G	Power GND for Core
CLK SYSTEM/ ICE INTERFACE				
X32I	48	52	I	32K Oscillator crystal input
X32O	47	51	O	32K Oscillator crystal output
OPTION				
TEST	51	58	I	TEST Mode selection pin, high is test mode and low is normal mode (Pad internal pull low)
DAC				
DAC	24	26	O	Audio DAC output
ADC				
MICP	19	21	I	MIC amplifier input positive (Internal Floating)
MICN	18	20	I	MIC amplifier input negative (refer to application circuit)
MICOUT	17	19	O	MIC amplifier output (refer to application circuit)
OPI	16	18	I	Audio amplifier negative input (refer to application circuit)
AGC	15	17	IO	AGC by pass filter (refer to application circuit)
VMIC	22	24	O	Microphone power supply
VADREF	20	22	O	AVREF_DA reference pin
PLL				
VCOIN	25	27	I	PLL low pass filter input
Other Signal				
RESETB	52	59	I	System reset pin (active low) (internal 47Kohm pull high resistor)
VDD_REG	45	47	I	Positive supply for regulator(2.4V~5.5V)
VSS_REG	44	46	I	Ground reference for regulator
VDD33_REG	46	48	I/O	3V power output from regulator
Total: 56 pads				

5.1. PAD Assignment



5.2. PIN Map

LQFP64



6. FUNCTIONAL DESCRIPTIONS

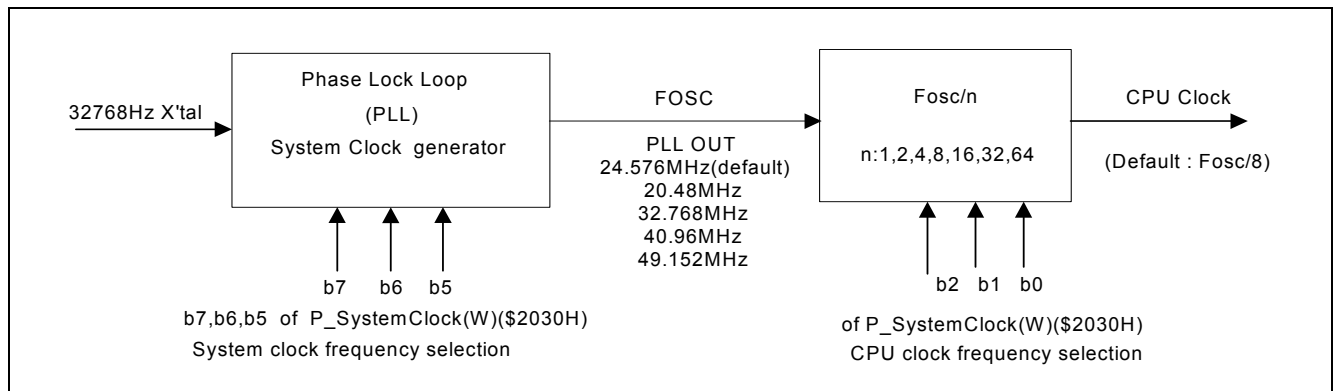
6.1. CPU

The GPCE064A is equipped with a 16-bit $\mu'nSP^{\text{TM}}$, the newest 16-bit microprocessor by Sunplus (pronounced as micro-n-SP). Eight registers are involved in $\mu'nSP^{\text{TM}}$: R1 - R4 (General-purpose registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP) and SR (Segment Register). The interrupts include three FIQs (Fast Interrupt Request) and eight IRQs (Interrupt Request), plus one software-interrupt, BREAK.

6.2. Memory

6.2.1. SRAM

The amount of SRAM is 2K-word (including Stack), ranged from \$0000 through \$07FF with access speed of two CPU clock cycles.



6.2.2. ROM

GPCE064A features a 32K-word high-speed memory with access speed of two CPU clock cycles.

6.3. PLL, Clock, Power Mode

6.3.1. PLL (Phase Lock Loop)

The purpose of PLL is to provide a base frequency (32768Hz) and to pump the frequency from 20.48MHz to 49.152MHz for system clock (F_{OSC}). The default PLL frequency is 24.576MHz.

6.3.1.1. System clock

Basically, the system clock is provided by PLL and programmed by the Port_SystemClock (W) to determine the clock frequency for system. The default system clock $F_{OSC} = 24.576\text{MHz}$ and CPU clock is $F_{OSC}/8$ if not specified. The initial CPU clock is $F_{OSC}/8$ after system wakes up and adjusts to desired CPU clock via programming the Port_SystemClock (W). This avoids ROM reading failure when system awakens.

6.3.1.2. 32768Hz RTC

The Real Time Clock (RTC) is normally used in watch, clock or other time related products. A 2Hz-RTC (0.5 seconds) function is loaded in GPCE064A. The RTC counts the time as well as to wake CPU up whenever RTC occurs. Since the RTC is generated each 0.5 seconds, time can be traced by the number of RTC occurrences. In addition, GPCE064A supports 32768Hz

oscillator in normal mode and auto-power-saving mode. In normal mode, 32768Hz OSC always runs at the highest power consumption. In auto-power-saving mode, however, it runs at normal mode for the first 7.5 seconds and switches back to power-saving mode automatically to save powers.

6.4. Standby Mode

The GPCE064A features a power savings mode (or called standby mode) for low power applications. To enter standby mode, the desired key wakeup port (IOA[15:0]) must be configured to input first. And read the Port_IOA_Data to latch the IOA state before entering the standby mode. Also remember to enable the corresponding interrupt source(s) for wakeup. After that, stop the CPU clock by writing \$5555 into Port_System_Sleep(W) to enter standby mode. In such mode, SRAM and I/Os remain in the previous states until CPU being awakened. The wakeup sources in GPCE064A include KEY wake up (IOA[15:0]), RTC wakeup, and IRQ1 - IRQ7. After GPCE064A is awakened, CPU will continue to execute the program from the location it slept. Programmer can also enable or disable the 32768Hz RTC when CPU is in standby mode.

6.5. Low Voltage Detection and Low Voltage Reset

6.5.1. Low voltage detection (LVD)

The Low Voltage Detection (LVD) reports the circumstance of present voltage. There are four LVD levels to be selected: 2.6V, 2.8V, 3.0V and 3.2V. Those levels can be programmed via P_LVD_Ctrl. As an example, suppose LVD is given to 2.8V. When the voltage drops below 2.8V, the b12 of P_LVD_Ctrl is read as HIGH. In such state, program can be designed to react this condition.

6.5.2. Low voltage reset

In addition to the LVD, the GPCE064A has another important function, Low Voltage Reset (LVR). With the LVR function, a reset signal is generated to reset system when the operating voltage drops below LVR level. Without LVR, the CPU becomes unstable and malfunctions when the operating voltage drops below LVR level. The LVR will reset all functions to the initial operational (stable) states when the voltage drops below LVR level.

6.6. Interrupt

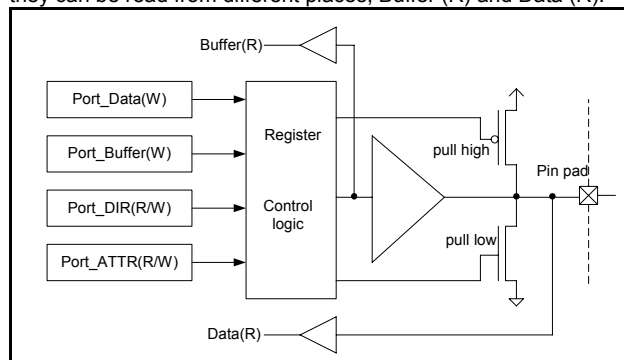
The GPCE064A has 13 interrupt sources, grouped into two types, FIQ (Fast Interrupt Request) and IRQ (Interrupt request). The priority of FIQ is higher than IRQ. FIQ is the high-priority interrupt while IRQ is the low-priority one. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt sources.

Interrupt Source	Interrupt Name / FIQ Name	IRQ Priority
Timer A	IRQ0_TMA/FIQ_TMA	1(High)
Timer B	IRQ1_TMB/FIQ_TMB	2
Timer C	IRQ2_TMC/FIQ_TMC	3
SPI	IRQ3_SPI/FIQ_SPI	4
Key wakeup	IRQ5_KEY/FIQ_KEY	5
EXT1	IRQ5_EXT1/FIQ_EXT1	6
EXT2	IRQ5_EXT2/FIQ_EXT2	7

Interrupt Source	Interrupt Name / FIQ Name	IRQ Priority
4096Hz	IRQ6_4KHz/FIQ_4KHz	8
2048Hz	IRQ6_2KHz/FIQ_2KHz	9
512Hz	IRQ6_512Hz/FIQ_512Hz	10
64Hz	IRQ7_64Hz/FIQ_64Hz	11
16Hz	IRQ7_16Hz FIQ_16Hz	12
2Hz	IRQ7_2Hz/FIQ_2Hz	13(Low)

6.7. I/O

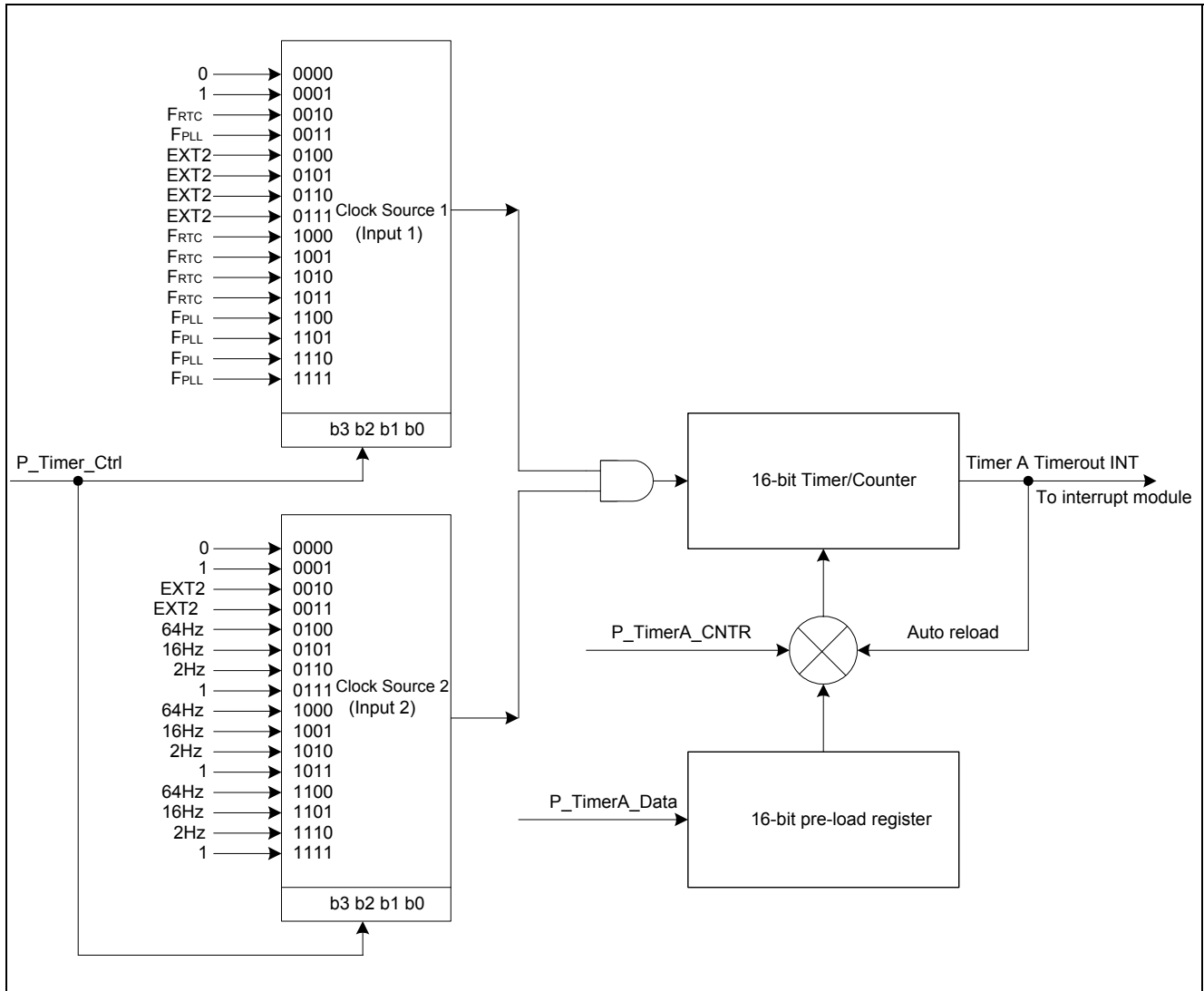
Two I/O ports are built in GPCE064A - PortA and PortB, total has 32 bit-programmable I/Os. The PortA is a general purpose I/O with programmable wakeup capability, i.e. IOA [15:0] is the key wakeup port. To activate key wakeup function, latch data on Port_IOA_Data and enable the key wakeup function. Wakeup is triggered when the PortA state is different from at the time latched. Furthermore, the I/O ports can be operated at 5V level, higher than the CPU core which is a 3V level system. Suppose system operating voltage is running at 3.3V, and VDDIO (power for I/O) operates from 3.3V to 5.5V. In such condition, the I/O pad is capable of operating from 0V through VDDIO. The following diagram is an I/O schematic. Although data can be written into the same register through Port_Data and Port_Buffer, they can be read from different places, Buffer (R) and Data (R).



In addition to a general purpose I/O port function, PortA/B also shares/carries some special functions. A summary of PortA/B special functions is listed as follows:

6.8. Special Function in Port

Port	Special Function	Function Description	Note
IOA0	IO_PWM	IO_PWM Output	Refer to Timer section
IOA1	IROUT	IR Output	-
IOA2	-	-	-
IOA3	-	-	-
IOA4	High driving I/O	-	-
IOA5	High driving I/O	-	-
IOA6	High driving I/O	-	-
IOA7	High driving I/O	-	-
IOA8	Feedback Input1	-	Refer to below Example 1
	EXT1	External interrupt source 1 (negative edge triggered)	Set IOA8 as floating input mode
IOA9	Feedback Output1	Work with IOA8 by adding a RC circuit between them to get an OSC to EXT1 interrupt	Set IOA9 as inverted output
IOA10	Feedback Input2	-	Refer to below Example 1
	EXT2	External interrupt source 2 (negative edge triggered)	Set IOA10 as floating input mode
IOA11	Feedback Output2	Work with IOA10 by adding a RC circuit between them to get an OSC to EXT2 interrupts	Set IOA11 as inverted output
IOA12	SPI CS	SPI chip select	Refer to SPI section
IOA13	SPI CK	SPI clock	Refer to SPI section
IOA14	SPI TX	SPI data output	Refer to SPI section
IOA15	SPI RX	SPI data input	Refer to SPI section
IOB0	AN0	ADC Channel 0	Refer to ADC section
IOB1	AN1	ADC Channel 1	Refer to ADC section
IOB2	AN2	ADC Channel 2	Refer to ADC section
IOB3	AN3	ADC Channel 3	Refer to ADC section
IOB4	AN4	ADC Channel 4	Refer to ADC section
IOB5	AN5	ADC Channel 5	Refer to ADC section
IOB6	AN6	ADC Channel 6	Refer to ADC section
IOB7	AN7	ADC Channel 7	Refer to ADC section



Refer to the above table, the configuration of IOA9, IOA10, IOA11, and IOA12 involves feedback function in which an OSC frequency can be obtained from EXT1 (EXT2) by simply adding a RC circuit between IOA8 (IOA10) and IOA9 (IOA11).

6.9. Timer / Counter

GPCE064A provides three 16-bit timers/counters - TimerA, TimerB and TimerC or so called universal counters. The clock source of Timer A/B/C are from clock source Input 1 and clock source Input 2 (see below table) which perform AND operation to form the varieties of combinations. When timer overflows, a timeout signal (TAOUT) is sent to CPU interrupt module to generate a timer interrupt signal. In addition, Timer A/B/C hardware interrupt events can be used to latch the DAC audio output and trigger ADC conversion.

Example to Timer A, sending a write signal into TMA_CNT, the value of TMA_DATA (value=N) will reload into TMA_CNT and set an appropriated clock source. Timer will up-count from N, N+1,

N+2... 0xFFFF. An INT signal is generated at the moment of timer rolling over from "0xFFFF" to "0x0000", and an INT signal is processed by INT controller immediately. At the same time, N will be reloaded into TMA_CNT and start counting again.

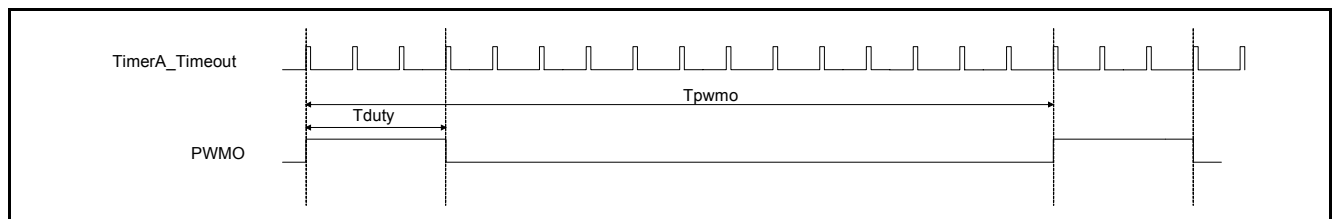
In Timer A, the clock Input 1 is a high frequency source and clock Input 2 is a low frequency clock source. The combination of clock Input 1 and 2 provides varieties of speeds to TimerA/CounterA - "1" representing pass signal (not gating), and "0" meaning timer deactivated. For instance, if Input 1="1", the clock is depending on Input 2. If Input 1="0", the TimerA is deactivated. The EXT1/ETX2 is the external clock source 1 and external clock source 2.

TMXSEL	Input 1	Input 2
0000	'0'	'0'
0001	'1'	'1'
0010	F _{RTC}	EXT2
0011	F _{PLL}	EXT2
0100	EXT2	64Hz
0101	EXT2	16Hz
0110	EXT2	2Hz
0111	EXT2	'1'
1000	F _{RTC}	64Hz
1001	F _{RTC}	16Hz
1010	F _{RTC}	2Hz
1011	F _{RTC}	'1'
1100	F _{PLL}	64Hz
1101	F _{PLL}	16Hz
1110	F _{PLL}	2Hz
1111	F _{PLL}	'1'

The following clock source A/B/C means clock source for Timer A/B/C respectively. Generally speaking, the clock source A and C are fast clock sources and source B comes from RTC system (32768Hz). Therefore, clock source B can be utilized as a precise counter for time counting, e.g., the 2Hz clock can be used for real time counting.

6.9.1. IO PWM

One IO PWMs which duty is selected from 1/16 to 14/16. Example the below figure is a 3/16-duration cycle. The PWMO waveform is made by selecting a pulse width through Port_PWM_Ctrl. As a result, each 16 cycles will generate a pulse width defined in control port. These PWM signals can be applied for controlling the speed of motor or other devices.



6.9.2. Timebase

Timebase, generated by 32768Hz crystal oscillator, is a combination of frequency selection. Furthermore, timebase generates 4KHz, 2KHz, 512Hz, 64Hz, 16Hz and 2Hz interrupt sources (FIQ6/IRQ6, FIQ7/IRQ7) for Real-Time-Clock

6.10. Sleep Mode, Wakeup, Halt Mode, and Watchdog

6.10.1. Sleep and wakeup modes

- 1) Sleep: After power-on reset, IC starts running until a sleep command is issued. When a sleep command is accepted, IC will turn the system clock (PLL) off. After all, it enters sleep mode.
- 2) Wakeup: CPU awaking from sleep mode requires a wakeup signal to turn the system clock (PLL) on. The FIQ/IRQ signal makes CPU to complete the wakeup process and initialization. The CPU wakeup source is given in the following table.

Wakeup Source
FIQ source
Timer A interrupt
Timer B interrupt
Timer C interrupt
SPI interrupt
EXT1/EXT2/KEY
RTC

6.10.2. Watchdog Reset

The GPCE064A provides another important feature, watchdog reset. If the watchdog function is enabled, a reset signal is generated to reset system when watchdog counter is overflow.

The purpose of watchdog is to monitor whether the system operates normally. Within a certain period, watchdog register must be cleared. If it is not cleared, CPU assumes the program has been running in an abnormal condition. As a result, the CPU will reset the system to the initial state and start running the program all over again.

6.11. Soft Reset Protection

Software reset. Writes \$5555 into P_System_Reset will reset the whole system like hardware reset (pull low RESETB pin), except a flag will set on in P_System_LVD_Ctrl(R/W).

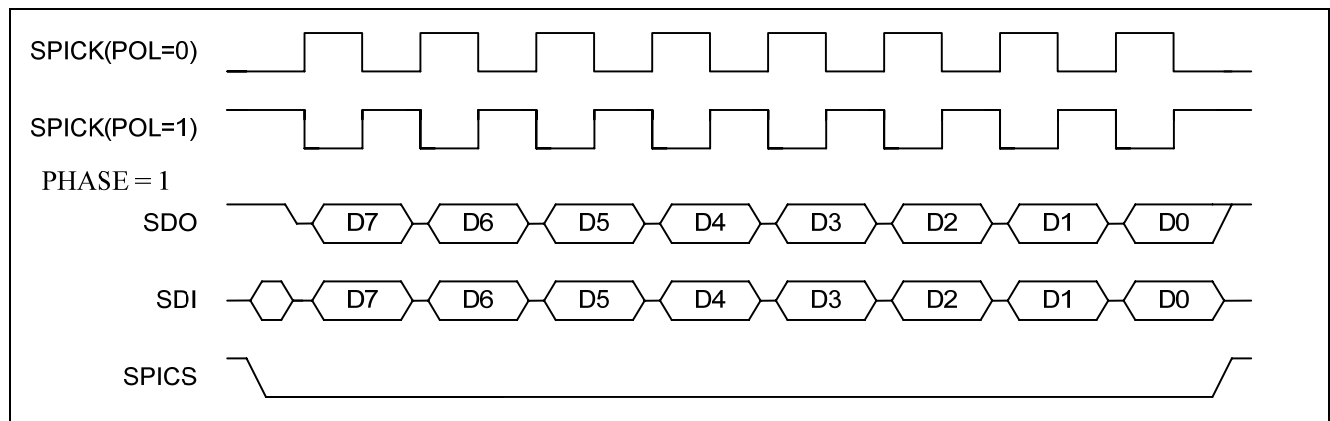
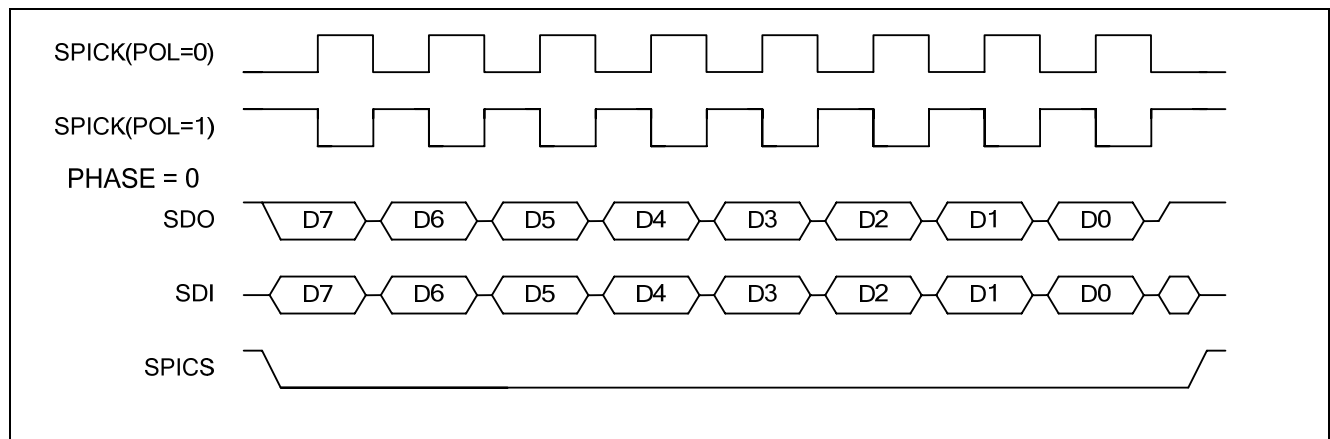
6.12. ADC (Analog to Digital Converter) / DAC

The GPCE064A has eight channels 12-bit ADC (Analog to Digital Converter). The function of an ADC is to convert analog signal to digital signal, e.g. a voltage level into a digital word. The eight channels of ADC can be seven channels of line-in from IOB [7:0] or one channel microphone (MIC) input through amplifier and AGC controller. The MIC amplifier circuit is capable of reducing

common mode noise by transmitting signals through differential MIC Inputs (MICN, MICP). Moreover, an external resistor can be applied to adjust microphone gain and time of AGC operating. The AD needs to select source of line-in before conversion. The ADC take pad(AVDD) as voltage reference.

6.13. SPI

A Serial Peripheral Interface (SPI) controller is built in GPCE064A to facilitate communicating with other devices and components. There are four control signals on SPI - SPICKS (IOA12), SPICK (IOA13), SDO (IOA14), and SDI (IOA15).



6.14. Audio Algorithm

The following speech types can be used in GPCE064A: PCM, SACM_S200, SACM_S480, SACM_S530, SACM_S720, SACM_A1600, SACM_A1601, SACM_A3600, SACM_DVR520,

SACM_DVR1600, SACM_DVR3200, and SACM_DVR4800. For melody synthesis, the GPCE064A supports SACM_MS01 (FM) and SACM_MS02 (wave-table) synthesizers.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 4.0V
PortA/B Pad Supply Voltage	V_{IO}	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0°C to +60°C
Storage Temperature	T_{STO}	-50°C to +150°C

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see DC Electrical Characteristics.

7.2. DC Characteristics (VDD_REG = 3.3V, VDDIO = 4.5V (PortA & B), $T_A = 25^\circ\text{C}$)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD_REG	2.4	-	5.5	V	-
Operating Current	I_{OP}	-	18	-	mA	$F_{OSC} = 49.152\text{MHz}$, AD, DAC disable, no load
Standby Current	I_{STB}	-	-	4	μA	Disable 32KHz crystal
				9	μA	Enable 32KHz, Disable PLL(F_{OSC})
Input High Level	V_{IH}	0.7VDD _{IO}	-	-	V	-
Input Low Level	V_{IL}	-	-	0.3VDD _{IO}	V	-
Output DAC Current (AUD1, AUD2)	I_{AUD}	-	-4.8	-	mA	For one channel DAC
Output High Current	I_{OH}	-	-11	-	mA	$V_{OH} = 0.9VDDIO$
Output Low Current (PA[3:0], PB[7:0])	I_{OL}	-	11	-	mA	$V_{OL} = 0.1VDDIO$
Output Low Current (PA[7:4])	I_{OL}	-	25	-	mA	-
Input Pull-Low Resister (PA15 :0, PB15 :8)	R_{PL}	-	120	-	K Ω	$V_{IN} = VDDIO$
Input Pull-Low Resister (PB[7:0])	R_{PL}	-	1000	-	K Ω	$V_{IN} = VDDIO$
Input Pull-High Resister (PA15 :0, PB15 :0)	R_{PH}	-	110	-	K Ω	$V_{IN} = VSS$

7.3. DC Characteristics (VDD_REG = 3.3V, VDDIO = 3.3V (PortA & B), $T_A = 25^\circ\text{C}$)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD_REG	2.4	-	5.5	V	-
Operating Current	I_{OP}	-	17	-	mA	$F_{OSC} = 49.152\text{MHz}$, AD, DAC disable, no load
Standby Current	I_{STB}	-	-	3	μA	Disable 32KHz crystal
				6	μA	Enable 32KHz, Disable PLL(F_{OSC})
Input High Level	V_{IH}	0.7VDD _{IO}	-	-	V	-
Input Low Level	V_{IL}	-	-	0.3VDD _{IO}	V	-

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Output DAC Current (AUD1, AUD2)	I _{AUD}	-	-3.5	-	mA	For one channel DAC
Output High Current	I _{OH}	-	-7	-	mA	V _{OH} = 0.9VDDIO
Output Low Current (PA[3:0], PB[7:0])	I _{OL}	-	6	-	mA	V _{OL} = 0.1VDDIO
Output Low Current (PA[7:4])	I _{OL}	-	15	-	mA	-
Input Pull-Low Resister (PA15 :0, PB15 :8)	R _{PL}	-	180	-	KΩ	V _{IN} = VDDIO
Input Pull-Low Resister (PB[7:0])	R _{PL}	-	1400	-	KΩ	V _{IN} = VDDIO
Input Pull-High Resister (PA15 :0, PB15 :0)	R _{PH}	-	160	-	KΩ	V _{IN} = VSS

7.4. ADC Characteristics (AVDD = 3.3V, T_A = 25°C)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
ADC LINE_IN Input Voltage Range from IOB[7:0]	VINL (Note 1)	VSS-0.3	-	AVDD+0.3	V
ADC Microphone Input Voltage Range	VINM	VSS-0.3	-	AVDD+0.3	V
Resolution of ADC	RESO	-	-	12	bits
Signal-to-Noise Plus Distortion of ADC from Line in	SINAD (Note 3)	-	60	-	dB
Effective Number of Bit	ENOB (Note 4)	8.0	9.0	-	bits
Integral Non-Linearity of ADC	INL	-	±3.0	-	LSB (Note 2)
Differential Non-Linearity of ADC	DNL (Note 6)	-	±1	-	LSB
AD Conversion Rate	F _{CONV}	-	-	F _{CPU} /256	Hz
Microphone Amplifier Gain	A _{MIC}	-	-	42	dB

Note1: Internal protection diodes clamp the analog input to AVDD and VSS. These diodes allow the analog input to swing from (VSS-0.3V) to (AVDD+0.3V) without causing damage to the devices.

Note2: LSB means Least Significant Bit. With VINL = 2.6V, 1LSB = 2.6V/2¹² = 0.635mV.

Note3: The SINAD testing condition at VINLp-p = 0.8*AVDD, F_{CONV} = F_{cpu}/512 = 49MHz/256 = 192KHz, Fin=1.0KHz Sine waves at AVDD = 3.0V from the IOB [7:0] input.

Note4: ENOB = (SINAD-1.76)/6.02.

Note5: The ADC of GPCE064A can guarantee 12 bits no missing code.

Note6: The microphone amplifier maximum gain = 15 * (60K/(1.5K+REXT)) V/V. The REXT is external resistor between OPI and MICOUT. The gain is 132V/V (=42dB) when REXT is 5.1K.

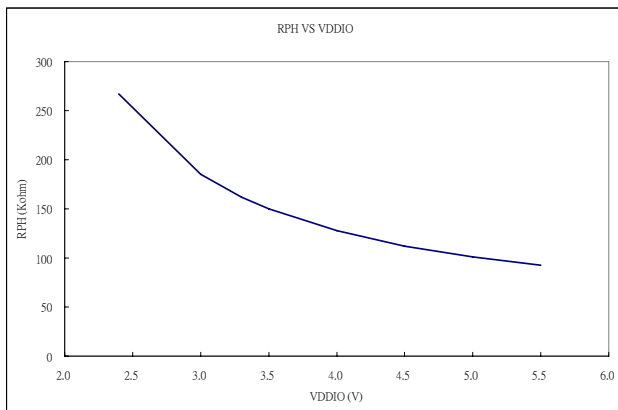
7.5. DAC Characteristics (AVDD = 3.3V, T_A = 25°C)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Resolution of DAC	RESO	-	-	14	bit
Signal to Noise Ratio of DAC	SNR	-	82	-	dB
Sample Rate	F _S	-	-	400K	Hz
THD+N at FS	F _{OUT} = 1K Hz	-	0.2	-	%

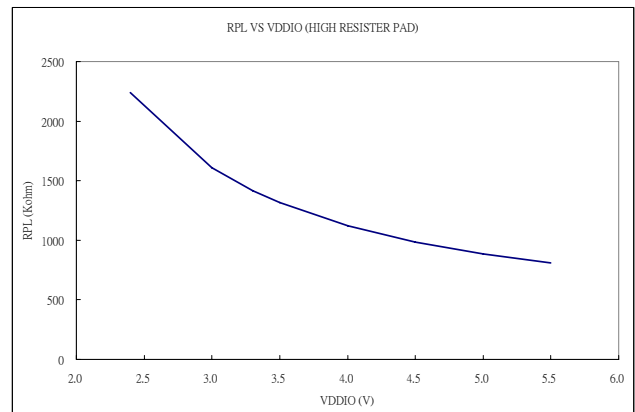
7.6. Regulator Characteristics ($T_A = 25^\circ\text{C}$)

Characteristics	Symbol	Unit			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	2.4	-	5.5	V
Maximum Current Output	IREGO	-	-	60	mA
Output Voltage	VREGO	3.14	3.3	3.46	V
Standby Current	IRGES	-	2.5	-	μA

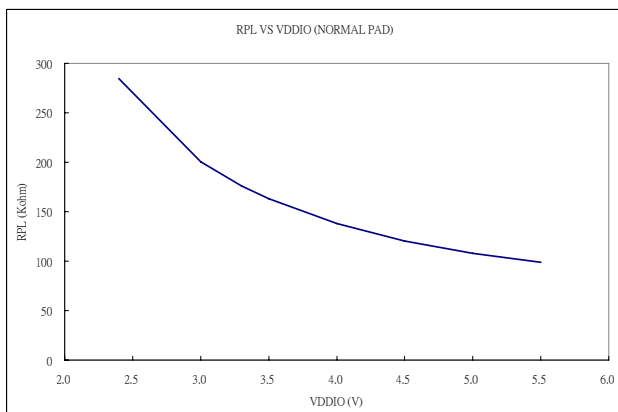
7.7. Pull High Resister and VDDIO



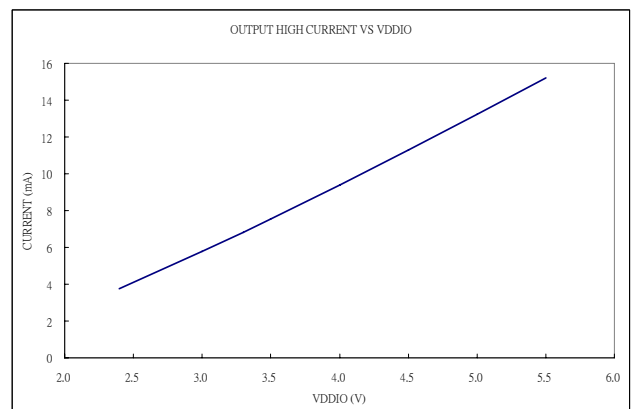
7.9. Pull Low Resister and VDDIO(IOB[7:0] PAD with input high)



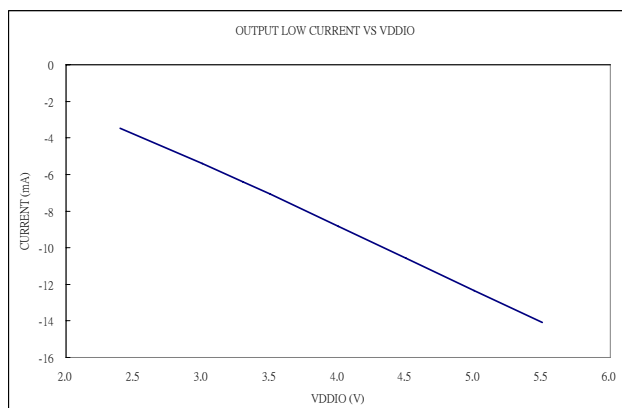
7.8. Pull Low Resister and VDDIO(Normal PAD)



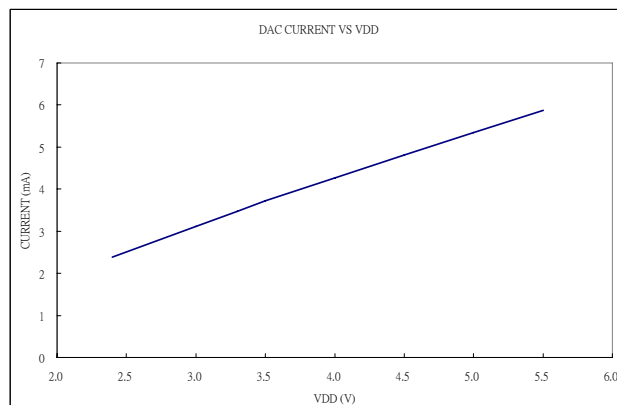
7.10. I/O Output High Current I_{OH} and VDDIO



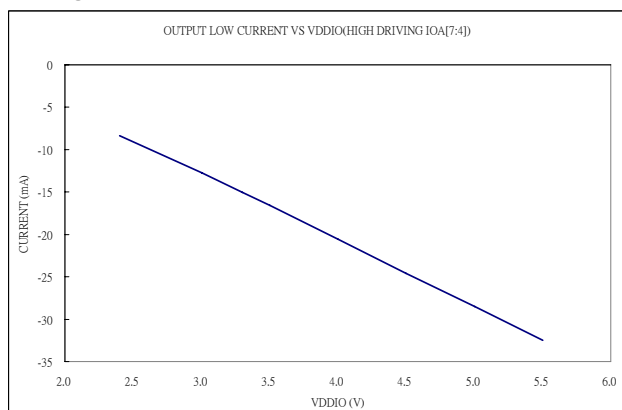
7.11. I/O Output Low Current I_{OL} and VDDIO(Normal Pad)



7.13. DAC Output Current I_{OL} and AVDD



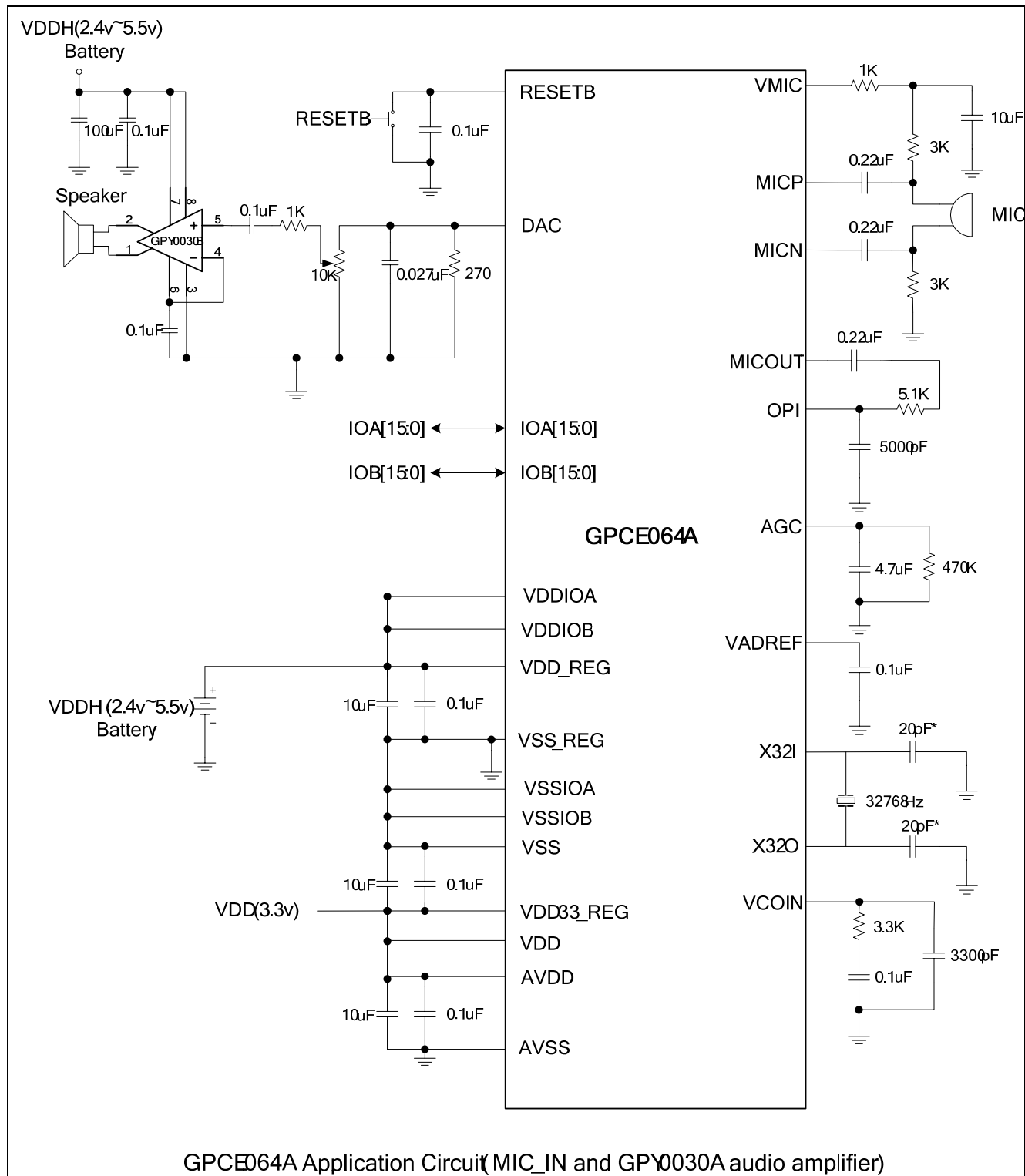
7.12. I/O Output Low Current I_{OL} and VDDIO(High driving pad)



8. APPLICATION CIRCUITS

8.1. Application Circuit-(1)

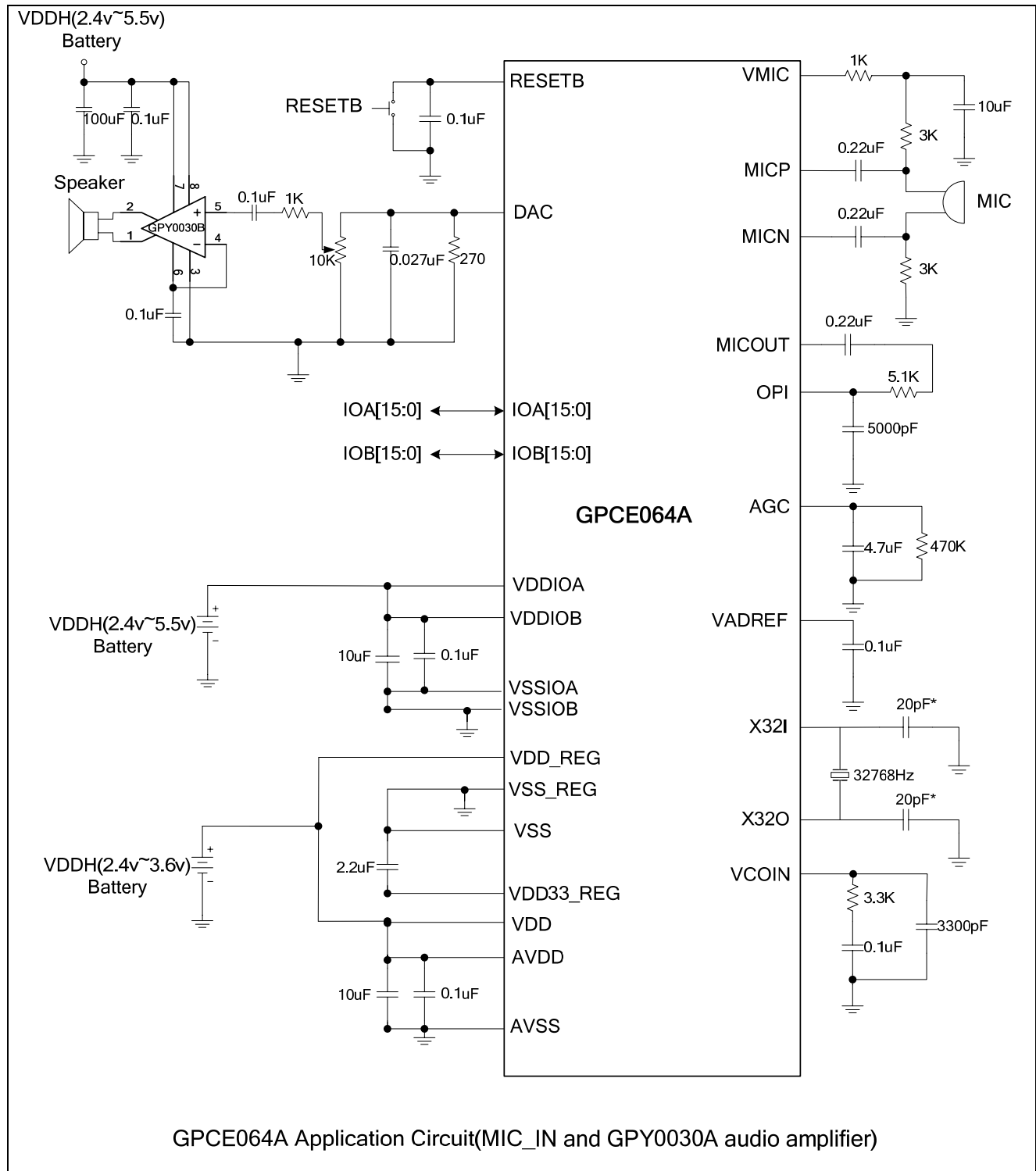
8.1.1. Application circuit (1) with regulator



Note*: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~35K and CL1=CL2=20~30pF (including PCB parasitic loading, for example, user should apply additional 14~24pF on X32I and X32O if PCB parasitic loading is 6pF)

Note: VDD33_REG is output of built-in regulator with maximum current 60 mA. It is recommended that only use it for internal power pad.

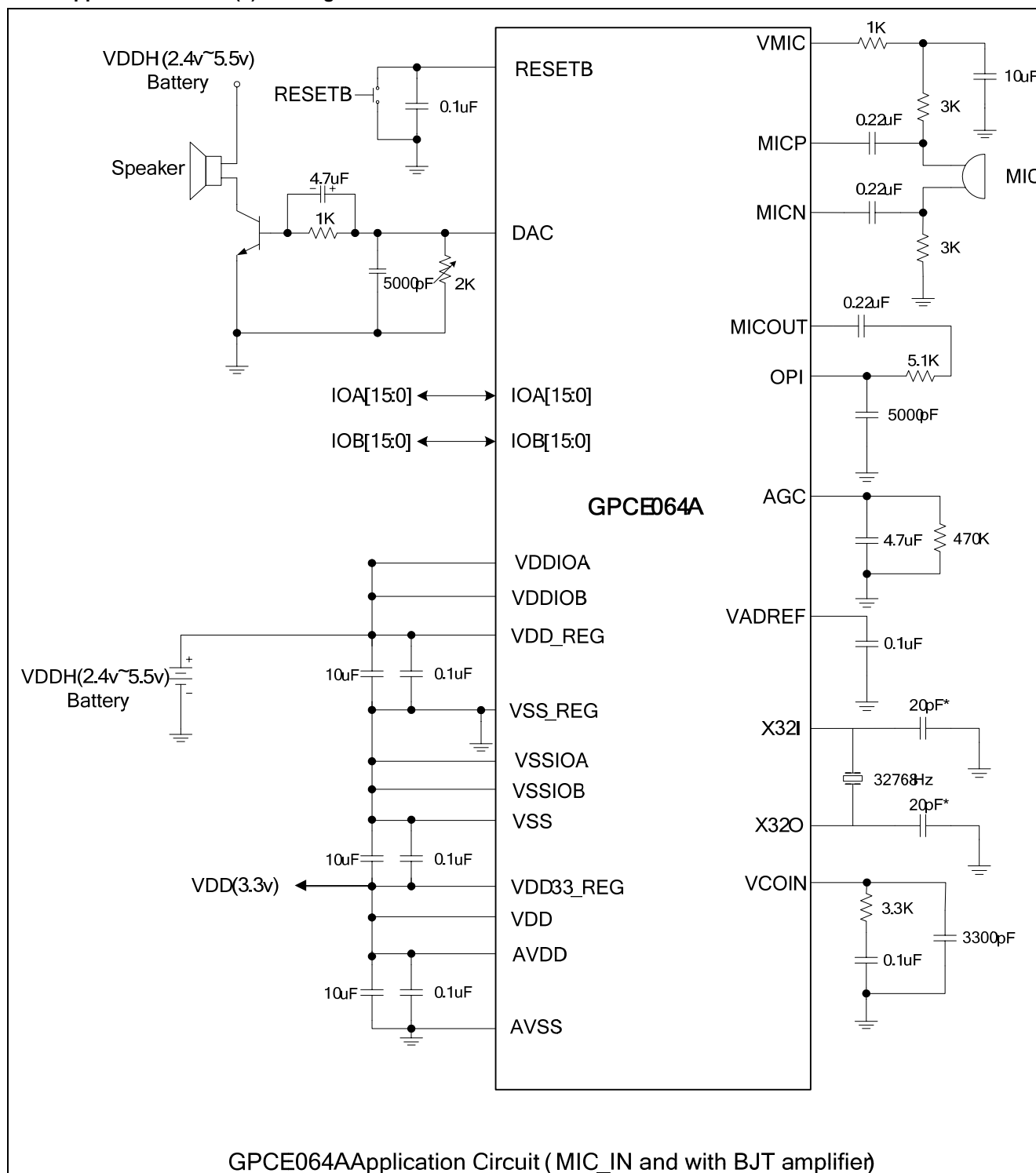
8.1.2. Application circuit (1) without regulator



Note*: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~35K and CL1=CL2 =20~30pF (including PCB parasitic loading, for example, user should apply additional 14~24pF on X32I and X32O if PCB parasitic loading is 6pF)

8.2. Application Circuit-(2)

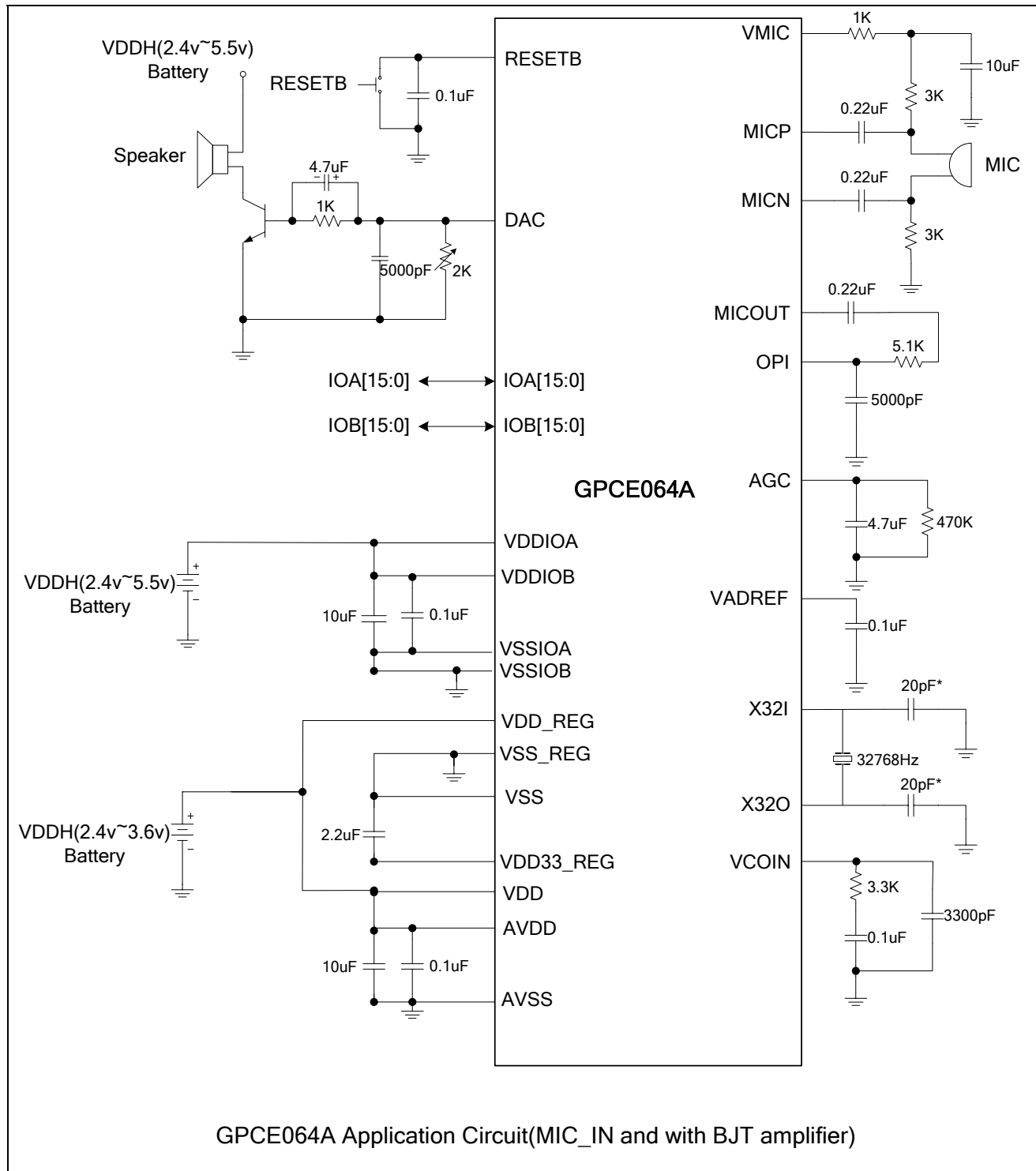
8.2.1. Application Circuit-(2) with regulator



Note*: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~35K and CL1=CL2 =20~30pF (including PCB parasitic loading, for example, user should apply additional 14~24pF on X32I and X32O if PCB parasitic loading is 6pF)

Note: VDD33_REG is output of built-in regulator with maximum current 60 mA. It is recommended that only use it for internal power pad.

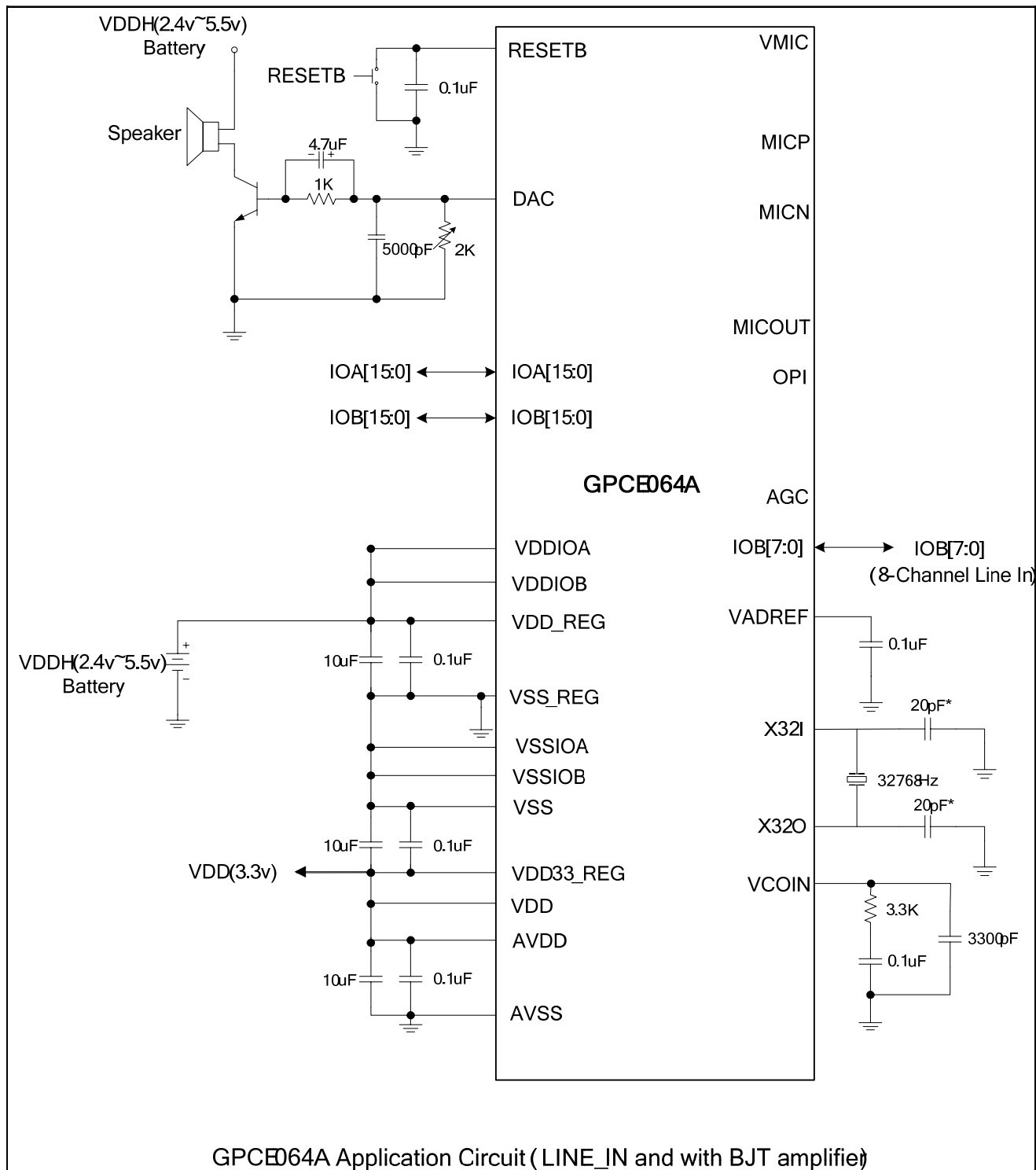
8.2.2. Application Circuit-(2) without regulator



Note*: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~35K and CL1=CL2 =20~30pF (including PCB parasitic loading, for example, user should apply additional 14~24pF on X32I and X32O if PCB parasitic loading is 6pF)

8.3. Application Circuit-(3)

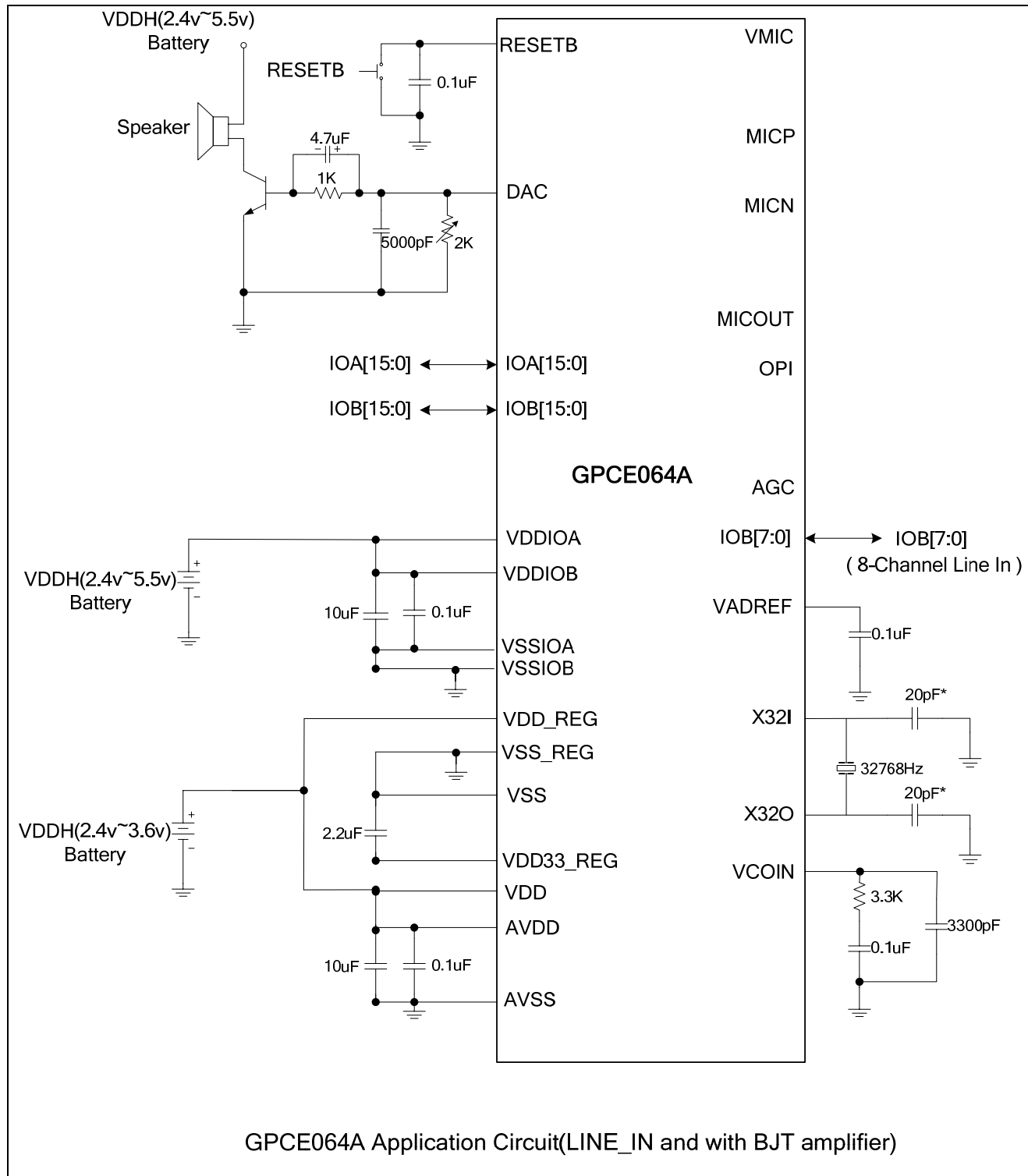
8.3.1. Application Circuit-(3) with regulator



Note*: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~35K and CL1=CL2 =20~30pF (including PCB parasitic loading, for example, user should apply additional 14~24pF on X32I and X32O if PCB parasitic loading is 6pF)

Note: VDD33_REG is output of built-in regulator with maximum current 60 mA. It is recommended that only use it for internal power pad.

8.3.2. Application Circuit-(3) without regulator



Note*: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~35K and CL1=CL2 =20~30pF (including PCB parasitic loading, for example, user should apply additional 14~24pF on X32I and X32O if PCB parasitic loading is 6pF)

9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPCE064A-NnnV-C	Chip form
GPCE064A-NnnV-QL02x	Halogen Free Package

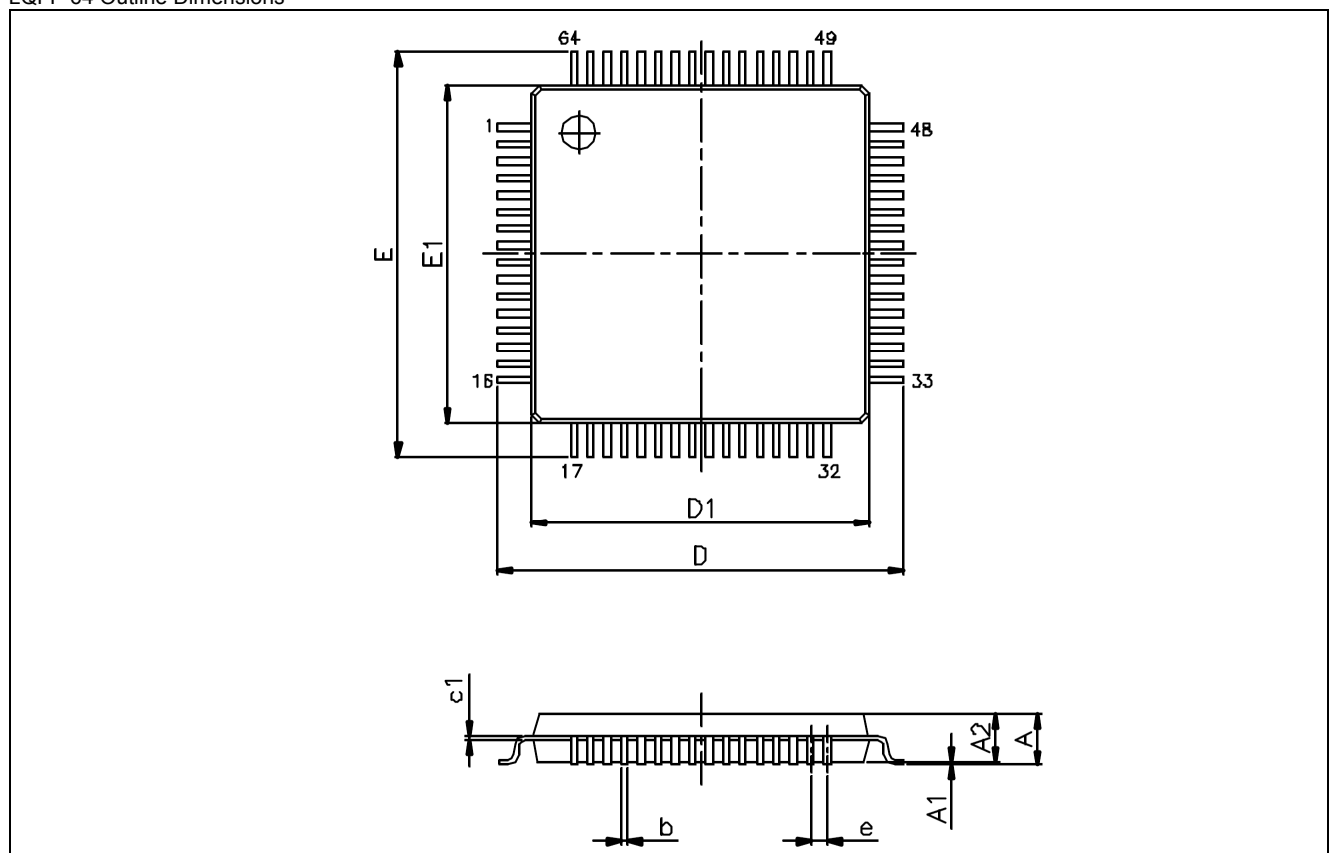
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

9.2. Package Information

LQFP 64 Outline Dimensions



Symbol	Dimension in mm		
	Min.	Typ.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c1	0.09	-	0.16
D	12.00		
D1	10.00		
E	12.00		
E1	10.00		
e	0.50 BSC.		

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11. REVISION HISTORY

Date	Revision #	Description	Page
Oct. 04, 2013	1.3	1. Add COMAIR logo to the cover page 2. Update X32K crystal's capacitance note in application circuit	
Oct. 13, 2010	1.2	Modify 3.FEATURES.	4
Dec. 10, 2008	1.1	1. Modify section 6.9.1 I/O PWM. 2. Modify section 6.12 ADC (Analog to Digital Converter) / DAC. 3. Add Application circuits to section 8.	12 13 19,21,23
Mar. 16, 2009	1.0	Released edition	
Dec. 18, 2008	0.2	Modify the Package Information in section 9.2.	18
Nov. 11, 2008	0.1	Original	20