DATA SHEET

GPCE2064C

16-bit Sound Controller With

32K X 16 ROM

Jun 12, 2017

Version 1.2

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16-BIT SOUND CONTROLLER WITH 32K X 16 ROM

1 GENERAL DESCRIPTION

GPCE2064C, a 16-bit architecture sound controller, features a 16-bit microprocessor *μ'nSP*™ (pronounced as *micro-n-SP*) to handle complex digital signal processes efficiently. The operating voltage from 2.4V to 5.5V and clock speed from 0.140625MHz through 48MHz allows GPCE2064C to be adopted in variety of applications. Furthermore, it also features a 32K-word ROM with a 2K-word working SRAM memory, 20 programmable multi-functional I/Os, three 16-bit timers/counters, 32KHz clock, Low Voltage Reset/Detection, one 14-bit DAC with push-pull amplifier, and many others.

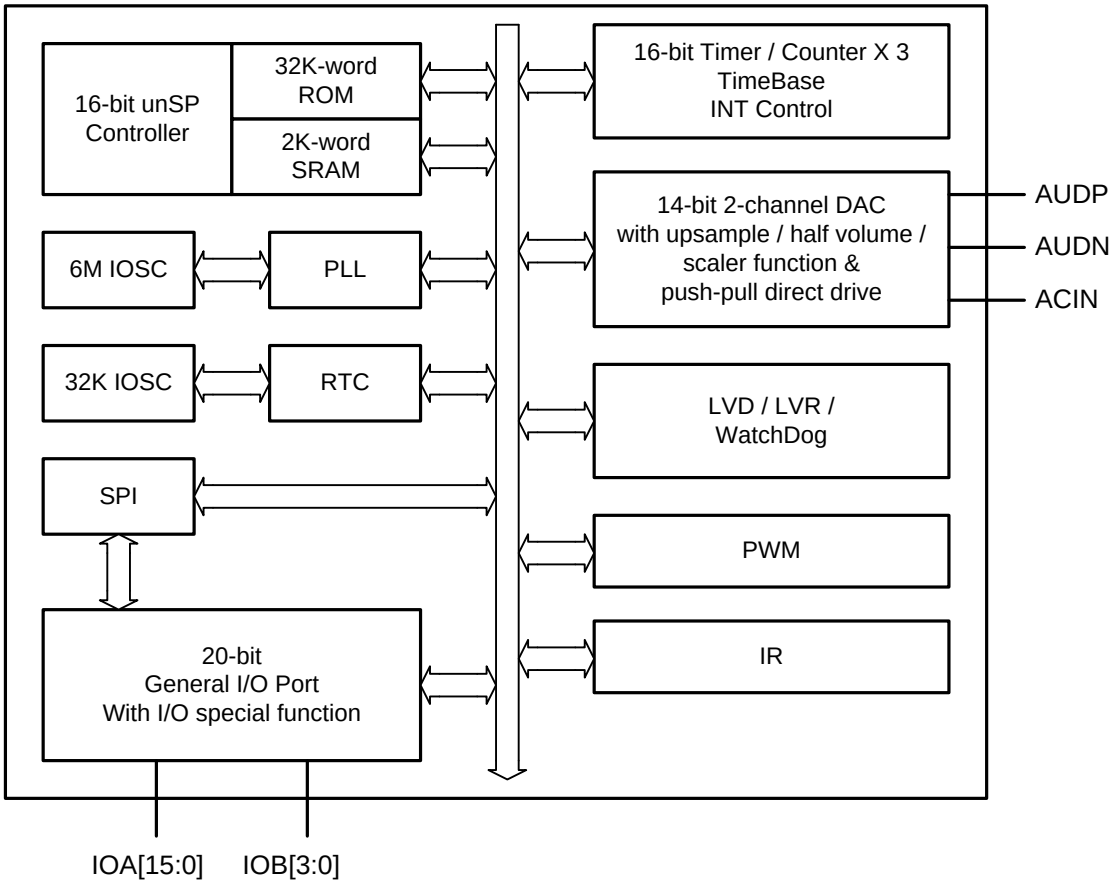
2 FEATURE

- 16-bit *μ'nSP*™ microprocessor
- CPU Clock: 0.140625MHz - 48MHz
- Operating Voltage: 2.4V - 5.5V
- Power regulator built-in with input voltage: 2.4~5.5V, output voltage: 2.4~3.3V
- IO PortA[11:0] & IOB[3:0] Operating Voltage: 2.4V - 5.5V
- IO PortA[15:12] Operating Voltage: 2.4V – 3.3V
- 32K-word fast speeds ROM
- 2K-word working SRAM
- Software-based audio processing
- Two sets of 14-bit software channel with noise filter, mixer and scalar to generate high quality sound
- Standby mode for power savings
- Three 16-bit timers/counters
- One 14-bit DAC with push-pull amplifier with cascade mode supported.
- 20 general I/Os (bit programmable)
- Key wakeup function (IOA0 - 15)
- PLL feature for system clock
- 32KHz internal resistor oscillator selected.
- Low voltage reset and low voltage detection
- Watchdog enable (always on)
- One SPI serial interface I/O

3 APPLICATION FIELD

- Intelligent Interactive Talking Toy
- Advanced Educational Toy
- Children's Learning Product
- Children's Storybook
- General Speech Synthesizer
- Long Duration Audio Product
- Playback Product

4 BLOCK DIAGRAM



5 SIGNAL DESCRIPTIONS

5.1 For Chip Form

Mnemonic	Power Domain	Type	Description
PORT A, Port B			
IOA[11:0]	5V	I/O	IOA[11:0] : bi-directional I/O ports
IOA[15:12]	3V	I/O	IOA[15:12] : bi-directional I/O ports
IOB [3:0]	5V	I/O	IOB [3:0]: bi-directional I/O ports.
Power & GND			
V50_IO	5V	P	Power vdd for Port A [11:0] and Port B[3:0]
VSS_REG	GND	G	Power GND for Port A[11:0] and PortB[3:0]
V33_REG	3V	P	3V Power output from regulator
V50_REG	5V	P	Power supply for regulator (2.4V~5.5V)
VSS_REG	GND	G	Ground reference for regulator
V50_DAC	5V	P	Positive 5V supply for push-pull DAC
V50_AMP	5V	P	Positive 5V supply for push-pull DAC post driver
VSS_DAC	GND	G	Ground reference for push-pull DAC
VSS_AMP	GND	G	Ground reference for push-pull DAC post driver
OPTION			
ROSC_R	3V	I	PLL reference clock selection pin 1: reference clock is ROSC_6M 0: reference clock is IOSC_6M (default : PAD is internal pull low)
TEST	3V	I	TEST Mode selection pin, high is test mode and low is normal mode (Pad internal pull low)
DAC			
AUDP	5V	O	Audio output of push pull DAC
AUDN	5V	O	Audio output of push pull DAC
ACIN	5V	U	Audio analog mixer in
Other Signal			
RESETB	3V	I	System reset pin (active low) (internal 47Kohm pull high resistor)
Trim PAD			
VPP	6.5V	P	eFuse programming power (for IOSC_32K, IOSC_6M, regulator voltage and LVR enable)
VSS_FUSE	0V	G	eFuse programming ground

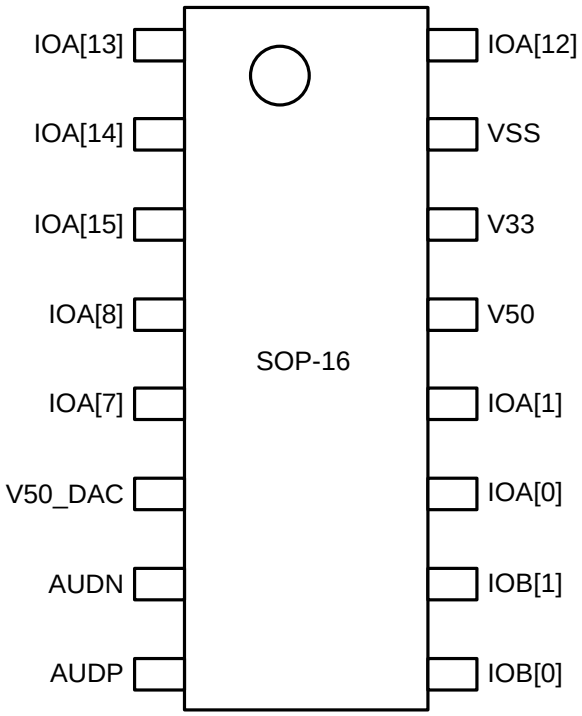
5.2 For SOP-16 Package

5.2.1 Pin Descriptions

Type：I = Input, O = Output, S = Supply, AO=Analog Output

Pin Name	SOP-16	Type	Description
IOA[13]	1	I/O	Bi-directional I/O ports (SPI serial interface I/O)
IOA[14]	2	I/O	Bi-directional I/O ports (SPI serial interface I/O)
IOA[15]	3	I/O	Bi-directional I/O ports (SPI serial interface I/O)
IOA[8]	4	I/O	Bi-directional I/O ports
IOA[7]	5	I/O	Bi-directional I/O ports
V50_DAC	6	S	Positive 5V supply for push-pull DAC
AUDN	7	AO	Audio output of push pull DAC
AUDP	8	AO	Audio output of push pull DAC
IOB[0]	9	I/O	Bi-directional I/O ports.
IOB[1]	10	I/O	Bi-directional I/O ports.
IOA[0]	11	I/O	Bi-directional I/O ports
IOA[1]	12	I/O	Bi-directional I/O ports
V50	13	S	5.0V power input pin
V33	14	S	3.3V regulator output
VSS	15	S	Ground pin
IOA[12]	16	I/O	Bi-directional I/O ports (SPI serial interface I/O)

5.2.2 Pin Map



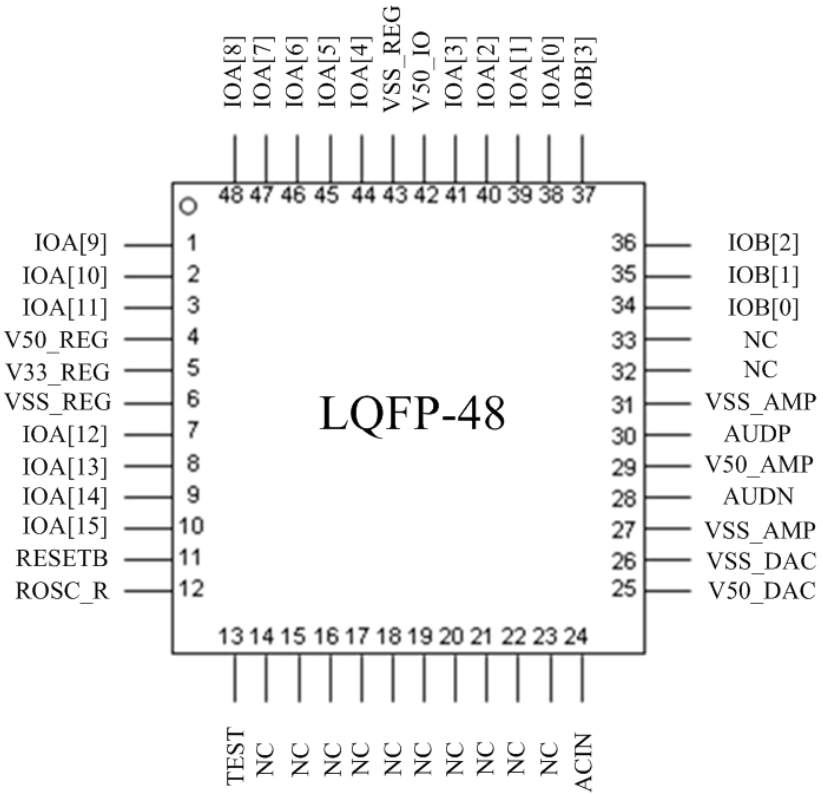
5.3 For LQFP-48 Package

5.3.1 Pin Descriptions

Type：I = Input, O = Output, S = Supply, AO=Analog Output

Pin Name	LQFP-48	Type	Description
IOA[9]	1	I/O	Bi-directional I/O ports
IOA[10]	2	I/O	Bi-directional I/O ports
IOA[11]	3	I/O	Bi-directional I/O ports
V50_REG	4	S	5.0V power input pin
V33_REG	5	S	3.3V regulator output
VSS_REG	6	S	Ground pin
IOA[12]	7	I/O	Bi-directional I/O ports (SPI serial interface I/O)
IOA[13]	8	I/O	Bi-directional I/O ports (SPI serial interface I/O)
IOA[14]	9	I/O	Bi-directional I/O ports (SPI serial interface I/O)
IOA[15]	10	I/O	Bi-directional I/O ports (SPI serial interface I/O)
RESETB	11	I	System reset pin (active low) (internal 47Kohm pull high resistor)
ROSC_R	12	I	PLL reference clock selection pin 1: reference clock is ROSC_6M 0: reference clock is IOSC_6M (default : PAD is internal pull low)
TEST	13	I	TEST Mode selection pin, high is test mode and low is normal mode (Pad internal pull low)
ACIN	24	I	Audio analog mixer in
V50_DAC	25	S	Positive 5V supply for push-pull DAC
VSS_DAC	26	S	Ground reference for regulator
VSS_AMP	27	S	Ground reference for push-pull DAC post driver
AUDN	28	AO	Audio output of push pull DAC
V50_AMP	29	S	Positive 5V supply for push-pull DAC post driver
AUDP	30	AO	Audio output of push pull DAC
VSS_AMP	31	S	Ground reference for push-pull DAC post driver
IOB[0]	34	I/O	Bi-directional I/O ports.
IOB[1]	35	I/O	Bi-directional I/O ports.
IOB[2]	36	I/O	Bi-directional I/O ports.
IOB[3]	37	I/O	Bi-directional I/O ports.
IOA[0]	38	I/O	Bi-directional I/O ports
IOA[1]	39	I/O	Bi-directional I/O ports
IOA[2]	40	I/O	Bi-directional I/O ports
IOA[3]	41	I/O	Bi-directional I/O ports
V50_IO	42	S	Power VDD for Port A [11:0] and Port B[3:0]
VSS_REG	43	S	Ground reference for regulator
IOA[4]	44	I/O	Bi-directional I/O ports
IOA[5]	45	I/O	Bi-directional I/O ports
IOA[6]	46	I/O	Bi-directional I/O ports
IOA[7]	47	I/O	Bi-directional I/O ports
IOA[8]	48	I/O	Bi-directional I/O ports

5.3.2 Pin Map


IOA[8] 48
IOA[7] 47
IOA[6] 46
IOA[5] 45
IOA[4] 44
VSS_REG 43
V50_IO 42
IOA[3] 41
IOA[2] 40
IOA[1] 39
IOA[0] 38
IOB[3] 37
IOA[9] 1
IOA[10] 2
IOA[11] 3
V50_REG 4
V33_REG 5
VSS_REG 6
IOA[12] 7
IOA[13] 8
IOA[14] 9
IOA[15] 10
RESETB 11
ROSC_R 12
LQFP-48
36 IOB[2]
35 IOB[1]
34 IOB[0]
33 NC
32 NC
31 VSS_AMP
30 AUDP
29 V50_AMP
28 AUDN
27 VSS_AMP
26 VSS_DAC
25 V50_DAC
13 TEST
14 NC
15 NC
16 NC
17 NC
18 NC
19 NC
20 NC
21 NC
22 NC
23 NC
24 ACIN

6 FUNCTION DESCRIPTION

6.1 CPU

GPCE2064C is equipped with a 16-bit μ'nSP (pronounced as micro-n-SP) microprocessor. Eight registers are involved in μ'nSP™: R1 - R4 (General-purpose registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP) and SR (Segment Register). The interrupts include three FIQs (Fast Interrupt Request) and eight IRQs (Interrupt Request), plus one software-interrupt, BREAK.

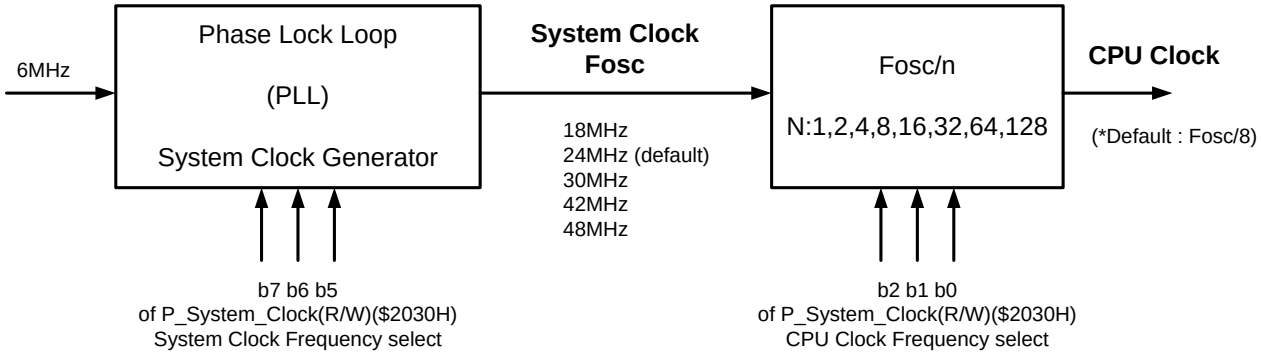
6.2 Memory

6.2.1 SRAM

The amount of SRAM is 2K-word (including Stack), ranged from $0000 through $07FF with access speed of two CPU clock cycles.

6.2.2 ROM

GPCE2064C features a 32K-word high-speed memory with access speed of two CPU clock cycles.



6.3 PLL, Clock, Power Mode

6.3.1 PLL (Phase Lock Loop)

The purpose of PLL is to provide a base frequency (32kHz) and to pump the frequency from 18MHz to 48MHz for system clock (F_{OSC}). The default PLL frequency is 24MHz.

6.3.1.1 System clock

Basically, system clock is supplied by PLL and programmed by Port_SystemClock (R/W) to determine the clock frequency for system. The default system clock F_{OSC} = 24MHz and CPU clock is F_{OSC}/8 if not specified. The initial CPU clock is Fosc/8 after system wakes up and adjusts to desired CPU clock via programming the Port_SystemClock (R/W). This avoids ROM reading failure when system wakes up.

6.3.1.2 32KHz clock

The 32KHz clock is normally used in watch, clock or other time related products. A 2Hz (0.5 seconds) function is loaded in GPCE2064C. It counts the time as well as to wake CPU up whenever 2Hz frequency takes place. Since the clock is generated each 0.5 seconds, actual time can be calculated by the number of 32KHz occurrences. In addition, GPCE2064C supports 32KHz internal resistor oscillator for normal mode and auto-power-saving mode.

6.4 Standby Mode

The GPCE2064C features a power savings mode (or called standby mode) for low power applications. To enter standby mode, the desired key wakeup port (IOA[15:0]) must be configured to input first. And read the Port_IOA_Data to latch IOA state before entering the standby mode as well as remembering to enable the corresponding interrupt source(s) for wakeup preparation. After that, stop the CPU clock by writing $5555 into Port_System_Sleep(W) to enter standby mode. In such mode, SRAM and I/Os retain at their previous states until CPU being awakened. The wakeup sources in GPCE2064C include KEY wakeup (IOA[15:0]), 32KHz wakeup, FIQ and IRQ0 - IRQ7. After GPCE2064C wakes up, CPU will continue to execute the program from where it entered sleep mode. Programmer can also enable or disable the 32KHz when CPU is in standby mode.

6.5 Low Voltage Detection and Low Voltage Reset

6.5.1 Low voltage detection (LVD)

The Low Voltage Detection (LVD) reports the circumstance of present voltage. There are four LVD levels to be selected: 2.6V, 2.8V, 3.0V and 3.2V. Those levels can be programmed via P_LVD_Ctrl. As an example, suppose LVD is given 2.8V. When the voltage drops below 2.8V, the b12 of P_LVD_Ctrl is read as HIGH. In such state, program can be designed to response this condition.

6.5.2 Low voltage reset

In addition to the LVD, the GPCE2064C has another important function, Low Voltage Reset (LVR). With the LVR function, a reset signal is generated to reset system when the operating voltage drops below LVR level. Without LVR, the CPU becomes unstable and malfunctions when the operating voltage drops below LVR level. The LVR will reset all functions to the initial operational (stable) states when the voltage drops below LVR level.

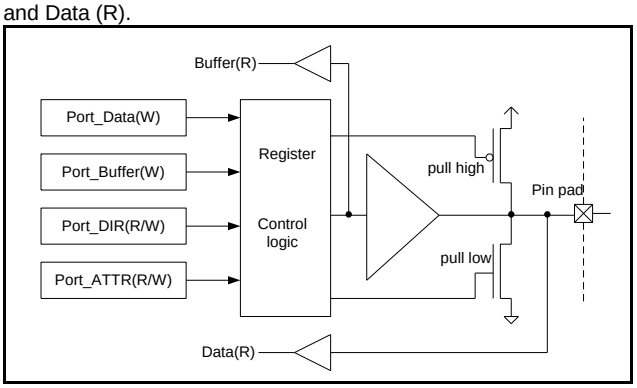
6.6 Interrupt

GPCE2064C has 13 interrupt sources, grouped into two types: FIQ (Fast Interrupt Request) and IRQ (Interrupt request). The priority of FIQ is higher than IRQ. FIQ is a high-priority interrupt and IRQ is the low-priority one, which can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt sources.

Interrupt Source	Interrupt Name / FIQ Name	IRQ Priority
Timer A	IRQ0_TMA/FIQ_TMA	1(High)
Timer B	IRQ1_TMB/FIQ_TMB	2
Timer C	IRQ2_TMC/FIQ_TMC	3
SPI	IRQ3_SPI/FIQ_SPI	4
Key wakeup	IRQ5_KEY/FIQ_KEY	5
EXT1	IRQ5_EXT1/FIQ_EXT1	6
EXT2	IRQ5_EXT2/FIQ_EXT2	7
4096Hz	IRQ6_4KHz/FIQ_4KHz	8
2048Hz	IRQ6_2KHz/FIQ_2KHz	9
512Hz	IRQ6_512Hz/FIQ_512Hz	10
64Hz	IRQ7_64Hz/FIQ_64Hz	11
16Hz	IRQ7_16Hz_FIQ_16Hz	12
2Hz	IRQ7_2Hz/FIQ_2Hz	13(Low)

6.7 I/O

Two I/O ports are built in GPCE2064C - PortA and PortB, total has 20 bit-programmable I/Os. The PortA is a general purpose I/O with programmable wakeup capability, i.e. IOA [15:0] is the key wakeup port. To activate key wakeup function, latch data on Port_IOA_Data and enable the key wakeup function. Wakeup is triggered when the PortA state is different from at the time latched. Furthermore, the PortA[11:0] and PortB[3:0] can be operated at 5V level, higher than the CPU core which is a 3V level system. The PortA[15:12] can be operated at 3.3V level. Suppose system operating voltage is running at 3.3V, V50_IO (power for I/O) operates from 3.3V to 5.5V. In such condition, the I/O pad is capable of operating from 0V through V50_IO. The following diagram is an I/O schematic. Although data can be written into the same register through Port_Data and Port_Buffer, they can be read from different places, Buffer (R) and Data (R).



In addition to a general purpose I/O port function, PortA/B also shares/carries some special functions. A summary of PortA/B special functions is depicted in the following section.

6.8 Special Function in Port

Port	Special Function	Function Description	Note
IOA0	IO_PWM	IO_PWM Output	Refer to Timer section
IOA1	IROUT	IR Output	-
IOA2	-	-	-
IOA3	-	-	-
IOA4	High sinking I/O	-	-
IOA5	High sinking I/O	-	-
IOA6	High sinking I/O	-	-
IOA7	High sinking I/O	-	-
IOA8	Feedback Input1	-	Refer to below Example 1
	EXT1	External interrupt source 1 (negative edge triggered)	Set IOA8 as floating input mode
IOA9	Feedback Output1	Work with IOA8 by adding a RC circuit between them to get an OSC to EXT1 interrupt	Set IOA9 as inverted output
IOA10	Feedback Input2	-	Refer to below Example 1
	EXT2	External interrupt source 2 (negative edge triggered)	Set IOA10 as floating input mode
IOA11	Feedback Output2	Work with IOA10 by adding a RC circuit between them to get an OSC to EXT2 interrupts	Set IOA11 as inverted output
IOA12	SPI CS	SPI chip select	Refer to SPI section
IOA13	SPI CK	SPI clock	Refer to SPI section
IOA14	SPI TX	SPI data output	Refer to SPI section
IOA15	SPI RX	SPI data input	Refer to SPI section
IOB0	-	-	-
IOB1	-	-	-
IOB2	-	-	-
IOB3	-	-	-
IOA[15:0], IOB[3:0]	Io toggle	Io toggle function	Refer to IO Special Functions section

Refer to the above table, the configuration of IOA8, IOA9, IOA10, and IOA11 involves feedback function in which an OSC frequency can be obtained from EXT1 (EXT2) by simply adding a RC circuit between IOA8 (IOA10) and IOA9 (IOA11).

6.9 Timer / Counter

GPCE2064C provides three 16-bit timers/counters - TimerA, TimerB and TimerC or so called universal counters. The clock source of Timer A/B/C are from clock source Input 1 and clock source Input 2 (see below table) which perform AND operation to form the varieties of combinations. When timer overflows, a timeout signal (TAOUT) is sent to CPU interrupt module to generate a timer interrupt signal. In addition, Timer A/B/C hardware interrupt events can be used to latch the DAC audio output and trigger ADC conversion.

Example to Timer A, sending a write signal into TMA_CNT, the value of TMA_DATA (value=N) will reload into TMA_CNT and set an appropriated clock source. Timer will up-count from N, N+1, N+2… 0XFFFF. An INT signal is generated at the moment of timer rolling over from “0xFFFF” to “0x0000”, and an INT signal is processed by INT controller immediately. At the same time, N will be reloaded into TMA_CNT and start counting again.

In Timer A, the clock Input 1 is a high frequency source and clock Input 2 is a low frequency clock source. The combination of clock Input 1 and input 2 provides varieties of speeds to TimerA/CounterA - “1” representing pass signal (not gating), and “0” meaning timer deactivated. For instance, if Input 1=”1”, the clock is depending on Input 2. If Input 1=”0”, TimerA is deactivated. The EXT1/ETX2 is the external clock source 1 and external clock source 2.

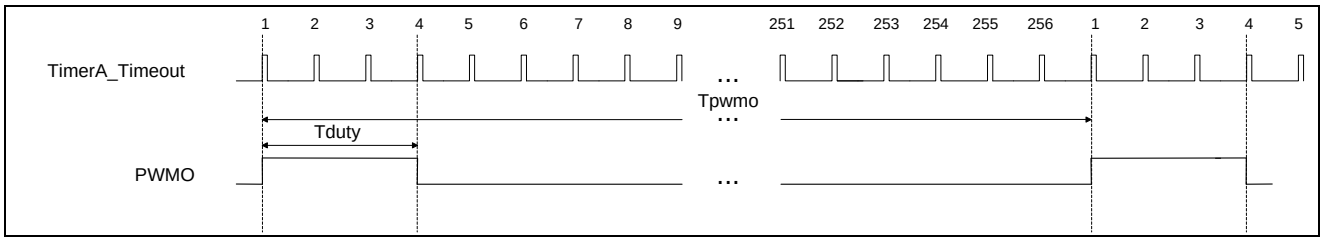
TMXSEL	Input 1	Input 2
0000	‘0’	‘0’
0001	‘1’	‘1’
0010	F_{32kHz}	EXT2

TMXSEL	Input 1	Input 2
0011	F_{PLL}	EXT2
0100	EXT2	64Hz
0101	EXT2	16Hz
0110	EXT2	2Hz
0111	EXT2	'1'
1000	F_{32kHz}	64Hz
1001	F_{32kHz}	16Hz
1010	F_{32kHz}	2Hz
1011	F_{32kHz}	'1'
1100	F_{PLL}	64Hz
1101	F_{PLL}	16Hz
1110	F_{PLL}	2Hz
1111	F_{PLL}	'1'

The following clock source A/B/C means clock source for Timer A/B/C respectively. Generally, the clock source A and C are fast clock sources and source B comes from 32KHz clock. Therefore, clock source B can be utilized as a precise counter for time counting, e.g., the 2Hz clock can be used for real time count.

6.9.1 IO PWM

The duty of an IO PWM is selected from 1/256 to 254/256. Example below is a 3/256-duration cycle. The PWMO waveform is made by selecting a pulse width through Port_PWM_Ctrl. As a result, each 256 cycles will generate a pulse width defined in control port. These PWM signals can be applied for controlling the speed of motor or other devices.



6.9.2 Timebase

Timebase, generated by 32KHz crystal oscillator, is a combination of frequency selection. Furthermore, timebase generates 4KHz, 2KHz, 512Hz, 64Hz, 16Hz and 2Hz interrupt sources (FIQ6/IRQ6, FIQ7/IRQ7) for Real-Time-Clock

6.10 Sleep Mode, Wakeup, Halt Mode, and Watchdog

6.10.1 Sleep and wakeup modes

1) Sleep: After power-on reset, IC starts running until a sleep command is issued. When a sleep command is accepted, IC will turn the system clock (PLL) off. After all, it enters sleep mode.

2) Wakeup: CPU awaking from sleep mode requires a wakeup signal to turn the system clock (PLL) on. The FIQ/IRQ signal makes CPU to complete the wakeup process and initialization. The CPU wakeup source is given in the following table.

Wakeup Source
FIQ source
Timer A interrupt
Timer B interrupt
Timer C interrupt
SPI interrupt
EXT1/EXT2/KEY
32kHz

6.10.2 Watchdog Reset

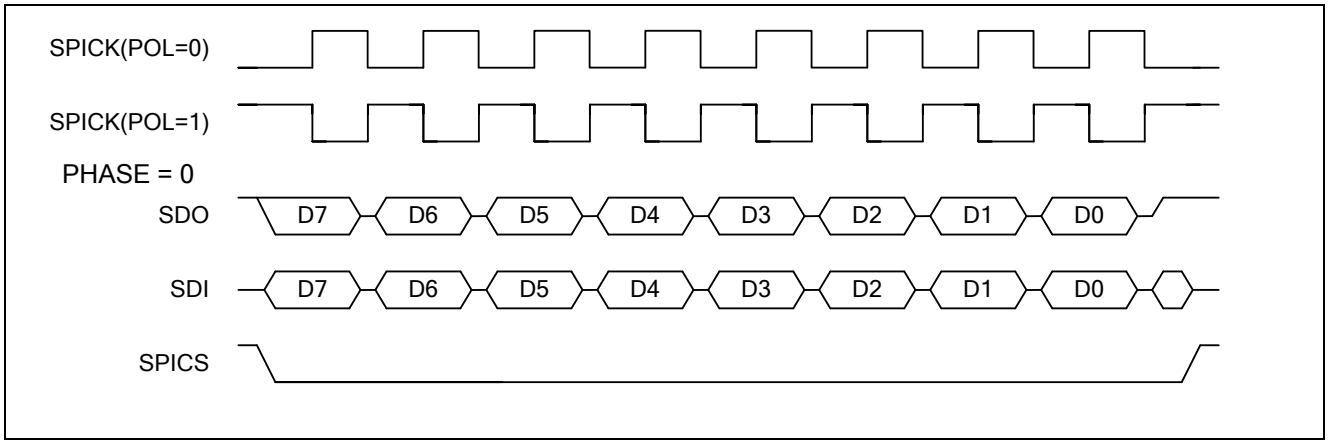
The GPCE2064C features another important function- watchdog reset. The watchdog function is enabled in default. A reset signal is generated to reset system when watchdog counter overflows. The purpose of watchdog is to monitor whether the system operates normally. Within a certain period, watchdog register must be cleared. If it is not cleared, CPU assumes the program has been running into an abnormal condition. As a result, CPU will reset the system to the initial state and start running program all over again.

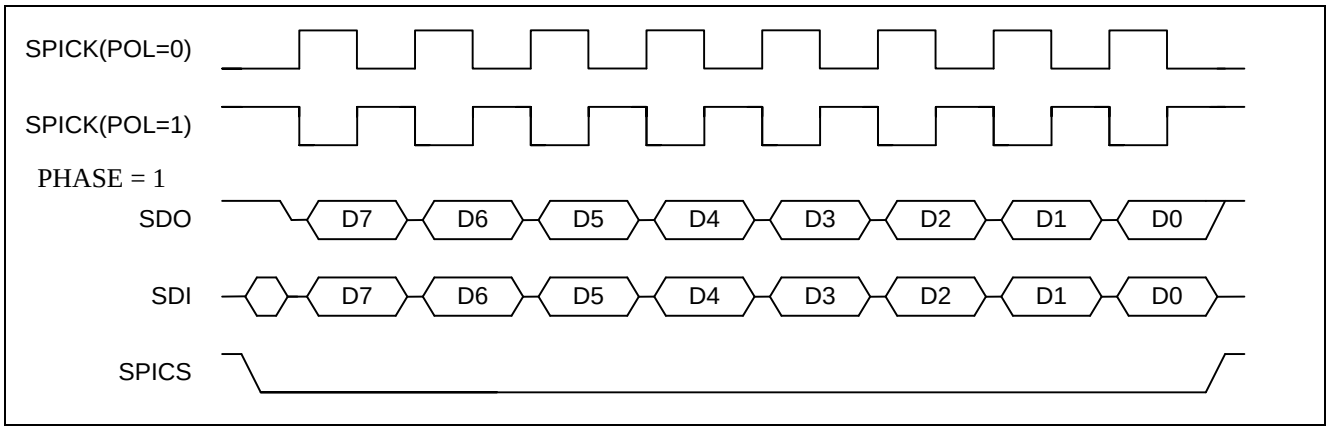
6.11 Soft Reset Protection

Software reset. To write $5555 into P_System_Reset will reset the whole system as hardware reset (pull low RESETB pin), except a flag will set on in P_System_LVD_Ctrl(R/W).

6.12 SPI

A Serial Peripheral Interface (SPI) controller is built in GPCE2064C to facilitate communication with other devices and components. There are four control signals on SPI - SPICS (IOA12), SPICK (IOA13), SDO (IOA14), and SDI (IOA15).





6.13 Audio Algorithm

The following speech types can be used in GPCE2064C: PCM, SACM_S200, SACM_S480, SACM_S530, SACM_A1600, SACM_A1601, SACM_A1800, SACM_A3400pro, SACM_A3600, SACM_DVR520, SACM_DVR1600, SACM_DVR1800, SACM_DVR3200, and SACM_DVR4800. For melody synthesis, GPCE2064C supports SACM_MS01 (FM) and SACM_MS02 (wave-table) synthesizers.

7 ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 4.0V
PortA[11:0]/PortB[3:0] Pad Supply Voltage	V_{IO1}	< 7.0V
PortA[15:12] Pad Supply Voltage	V_{IO2}	< 4.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions, see DC Electrical Characteristics.

7.2 DC Characteristics (VDD = 3.3V, VDDIO = 4.5V (PortA[11:0] & PortB[3:0]), TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.0	3.3	3.6	V	-
Operating Current	I_{OP}	-	9	-	mA	F_{OSC} = 48MHz, DAC disable, no load, No Loading, All GPIO toggling.
Standby Current	I_{STB}	-	-	5	μA	Disable 32KHz crystal
				10	μA	Enable 32KHz,Disable PLL(F_{OSC})
Input High Level	V_{IH}	0.7VDD_{IO}	-	-	V	-
Input Low Level	V_{IL}	-	-	0.3VDD_{IO}	V	-
Output High Current	I_{OH}	-	20	-	mA	V_{OH} = 0.7VDD
Output Low Current (PA[11:8], PA[3:0], PB[3:0])	I_{OL}	-	18	-	mA	V_{OL} = 0.3VDD
Output Low Current (PA[7:4])	I_{OL}	-	44	-	mA	V_{OL} = 0.3VDD
Input Pull-Low Resister (PA[11:0])	R_{PL}	-	110	-	KΩ	V_{IN} = VDD
Input Pull-Low Resister (PB[3:0])	R_{PL}	-	1100	-	KΩ	V_{IN} = VDD
Input Pull-High Resister (PA[11:0], PB[3:0])	R_{PH}	-	110	-	KΩ	V_{IN} = VSS
Internal ROSC frequency deviation	⊿F/F	-3%	6M	+3%	HZ	V33_REG = 3.3V

7.3 DC Characteristics (VDD = 3.3V, VDDIO = 3.3V (PortA[11:0] & PortB[3:0]), TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.0	3.3	3.6	V	-
Operating Current	I_{OP}	-	8	-	mA	F_{OSC} = 48MHz, DAC disable, no load
Standby Current	I_{STB}	-	-	3	μA	Disable 32KHz crystal
				6	μA	Enable 32KHz,Disable PLL(F_{OSC})

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input High Level	V_{IH}	$0.7VDD_{IO}$	-	-	V	-
Input Low Level	V_{IL}	-	-	$0.3VDD_{IO}$	V	-
Output High Current	I_{OH}	-	11	-	mA	V_{OH} = 0.7VDD
Output Low Current (PA & PB)	I_{OL}	-	11	-	mA	V_{OL} = 0.3VDD
Input Pull-Low Resister (PA)	R_{PL}	-	110	-	KΩ	V_{IN} = VDD
Input Pull-Low Resister (PB[3:0])	R_{PL}	-	1100	-	KΩ	V_{IN} = VDD
Input Pull-High Resister (PA & PB)	R_{PH}	-	110	-	KΩ	V_{IN} = VSS
Internal ROSC frequency deviation	⊿F/F	-3%	6M	+3%	HZ	V33_REG = 3.3V

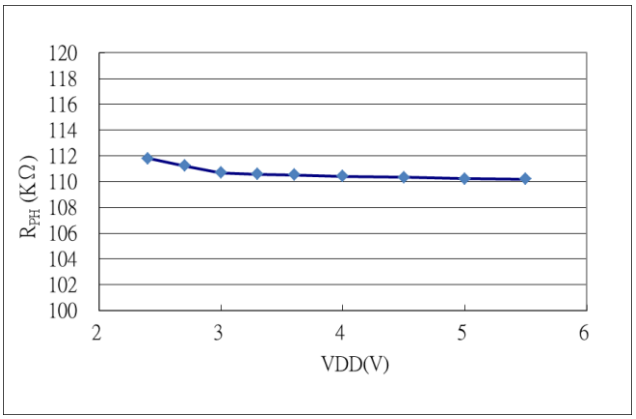
7.4 DAC Characteristics (V50_DAC = 5.0V, TA = 25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
DAC Resolution	RESO	-	-	14	bit
THD+n (5V @0.6W)	-	-	1	-	%
Noise at No Signal	-	-	-78	-	dBr A
Dynamic Range(-60dB)	-	-	-80	-	dBr A

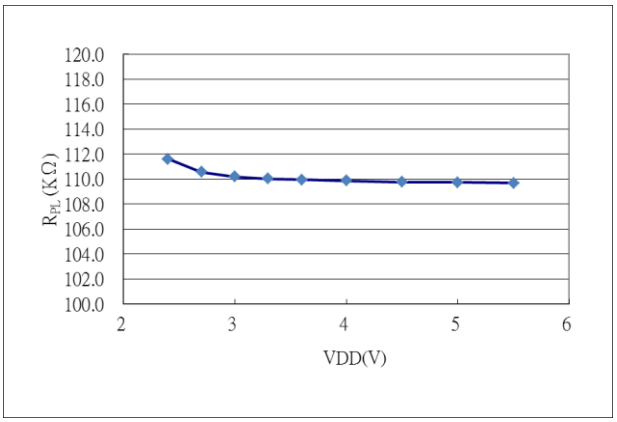
7.5 Regulator Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage	VREGI	2.3	4.5	5.5	V	
Maximum Current Output	IREGO	-	-	45	mA	VDD5V (Regulator in)= 4.5V, △VDD (Regulator out) <100mV
Output Voltage	VREGO	2.3	3.3	3.3	V	
Standby Current	IRGES	-	2.5	-	uA	

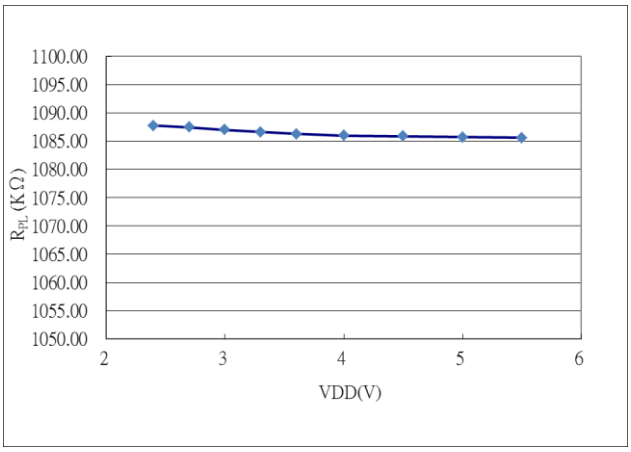
7.6 Pull High Resister and VDDIO



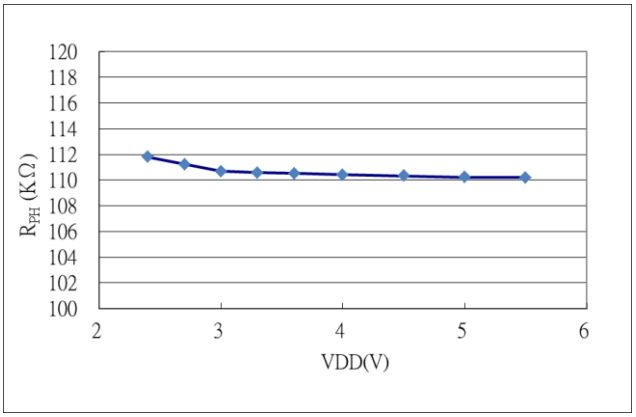
7.7 Pull Low Resister and VDDIO (Normal PAD)



7.8 Pull Low Resister and VDDIO (IOB[3:0] PAD with input high)

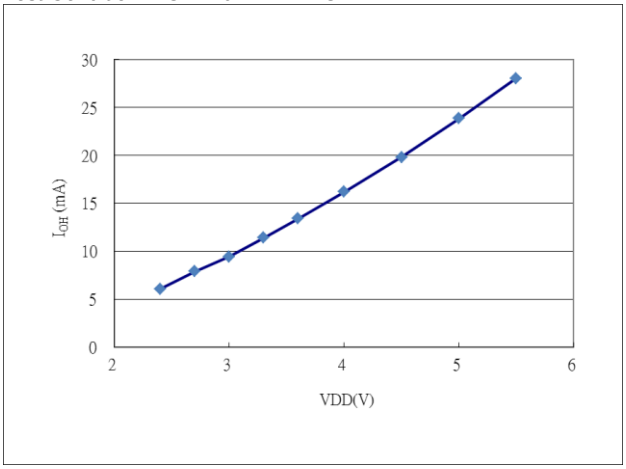


7.9 Pull High Resister and VDDIO (All PAD)



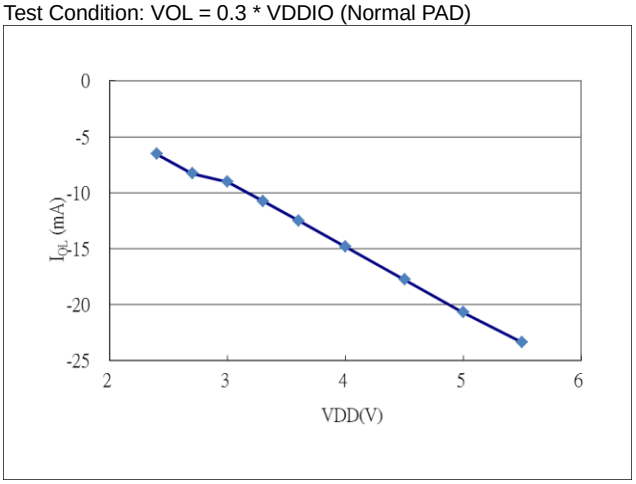
7.10 I/O Output High Current I_{OH} and VDDIO

Test Condition: VOH = 0.7 * VDDIO



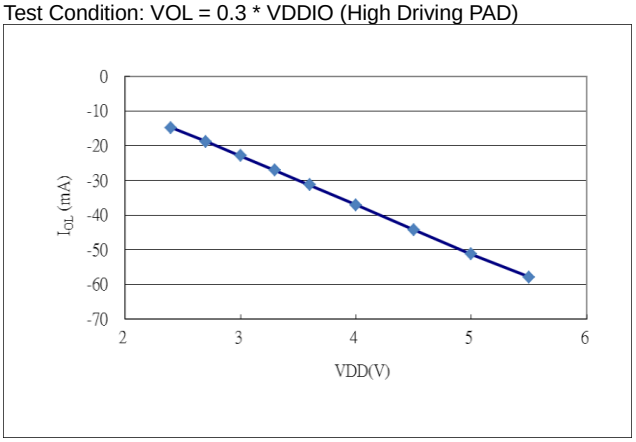
7.11 I/O Output Low Current I_{OL} and VDDIO (Normal Pad)

Test Condition: VOL = 0.3 * VDDIO (Normal PAD)

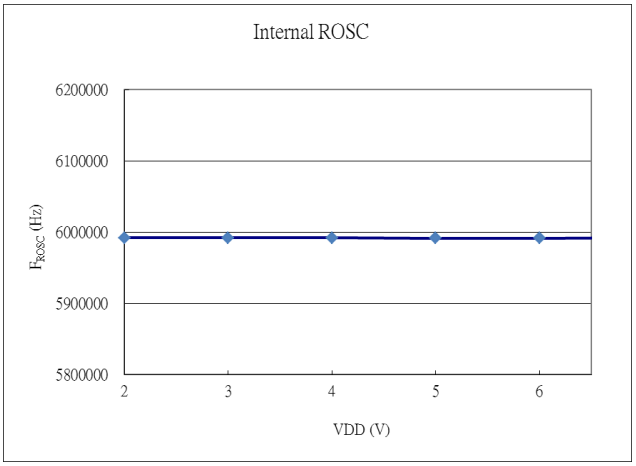


7.12 I/O Output Low Current I_{OL} and VDDIO (High sinking pad)

Test Condition: VOL = 0.3 * VDDIO (High Driving PAD)

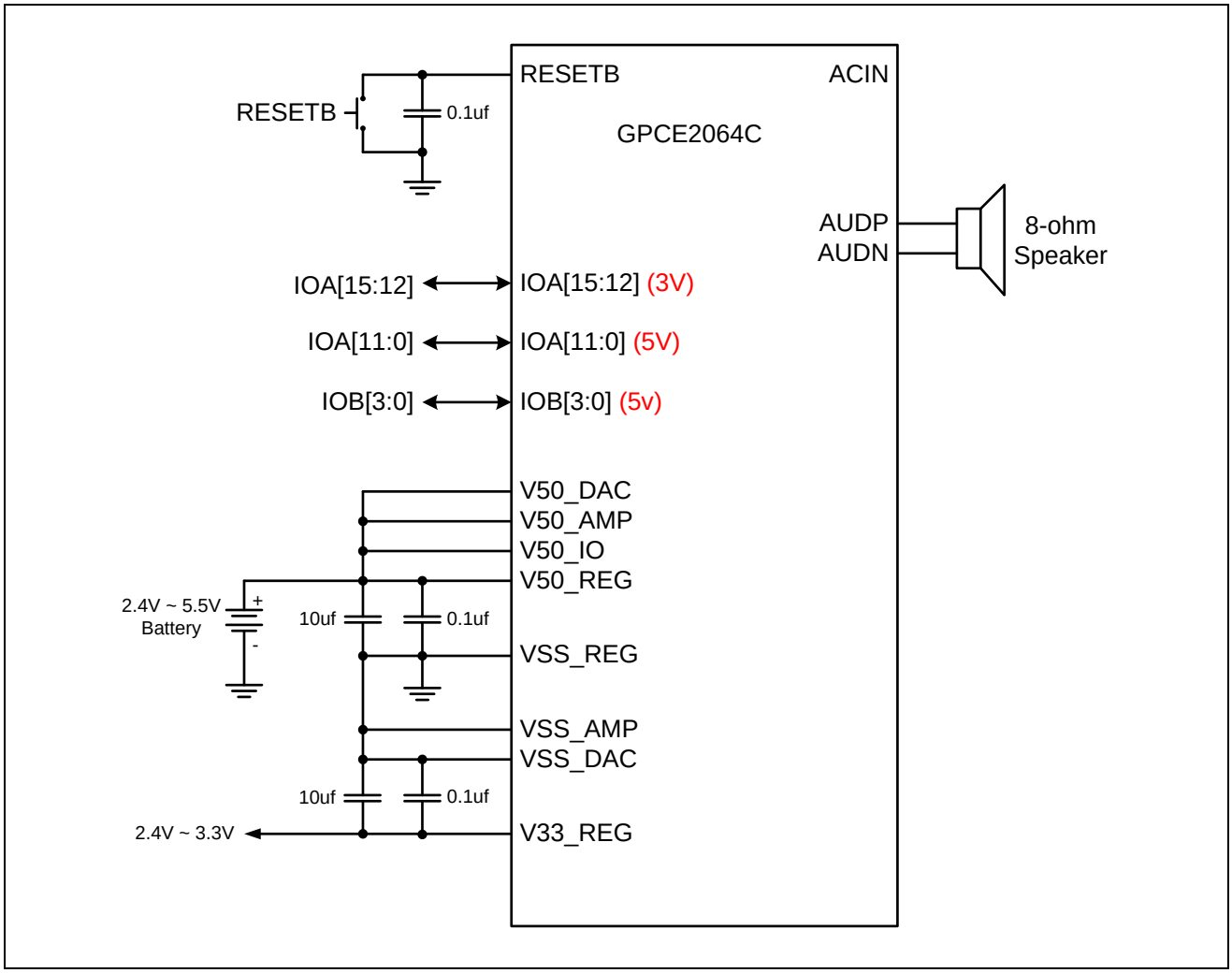


7.13 Internal ROSC and V33_REG

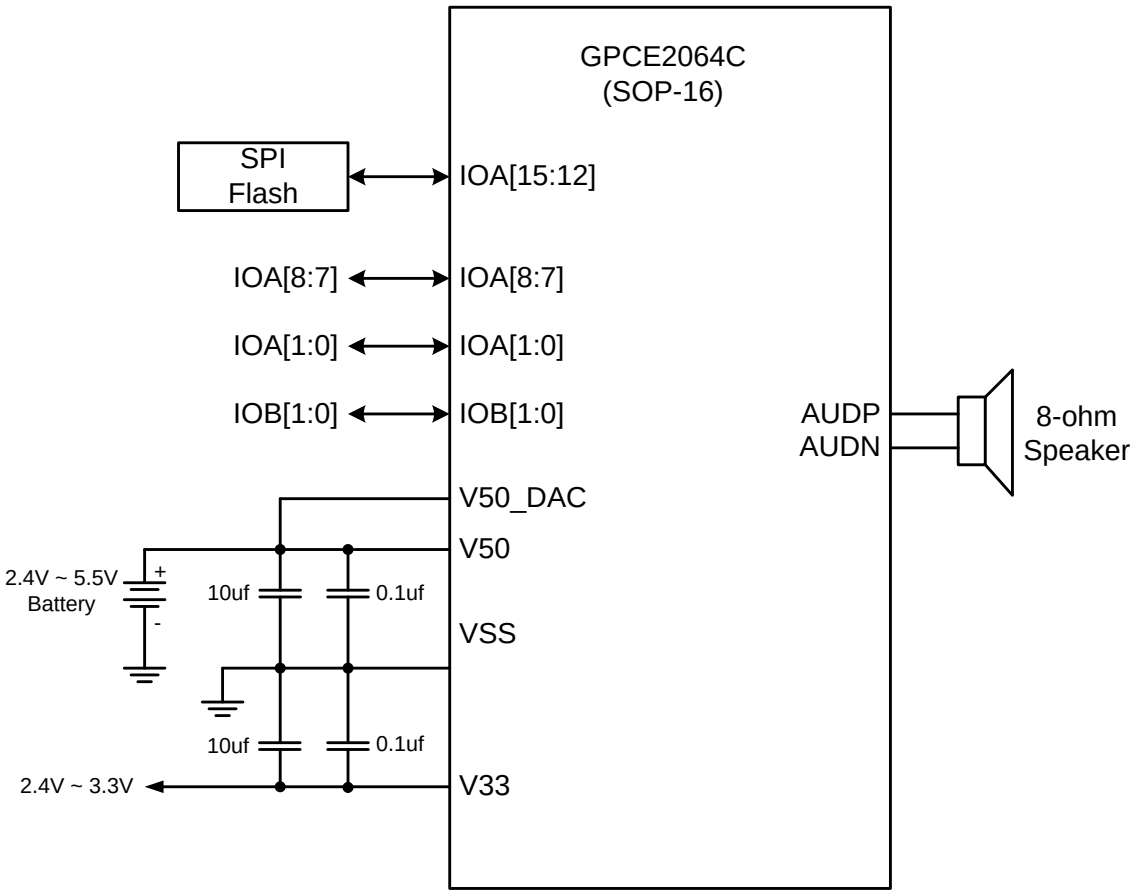


8 APPLICATION CIRCUITS

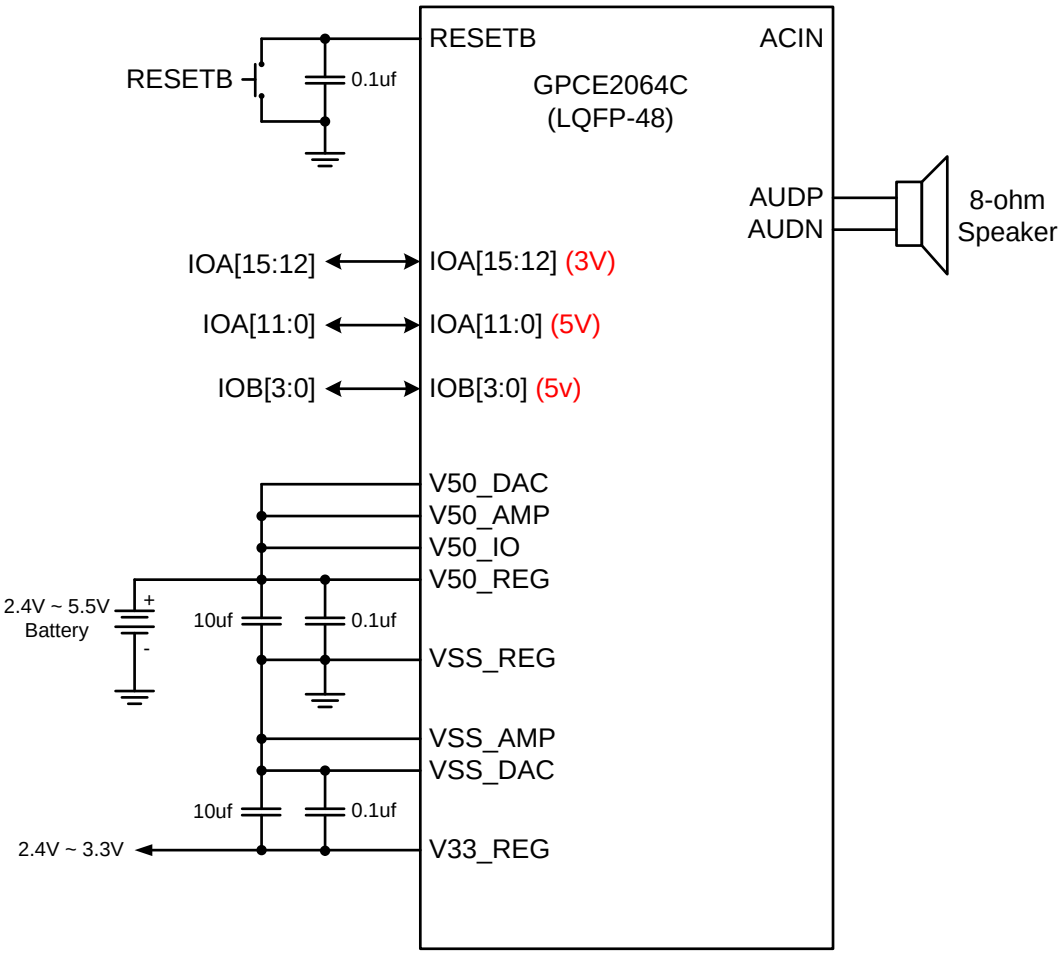
8.1 For Chip Form



8.2 For SOP-16 Package



8.3 For LQFP-48 Package



9 PACKAGE/PAD LOCATIONS

9.1 Ordering Information

Product Number	Package Type
GPCE2064C-NnnV-C	Chip form
GPCE2064C-NnnV-HS03x	Halogen Free Package
GPCE2064C-NnnV-HL23x	Halogen Free Package

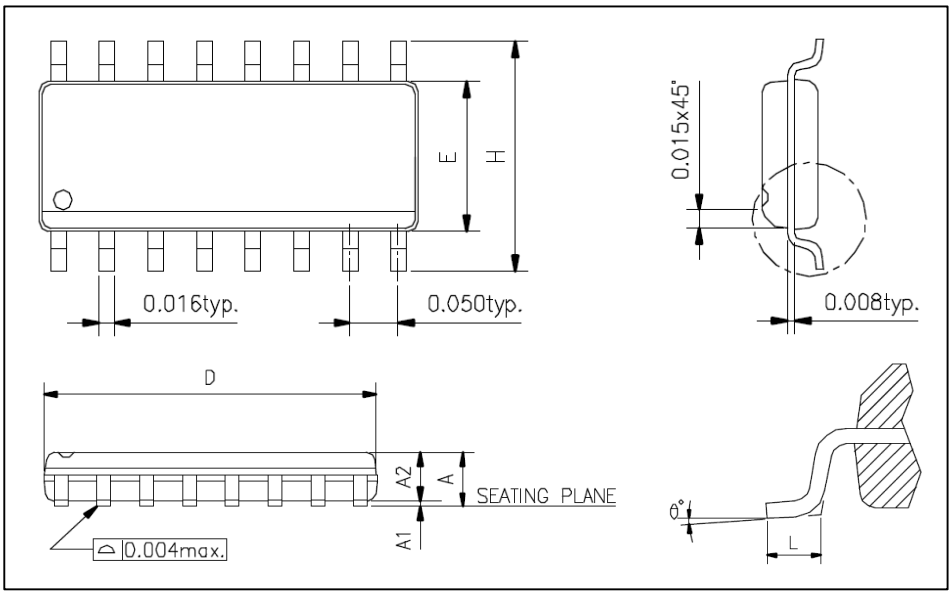
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: x = 0 – 9, serial number

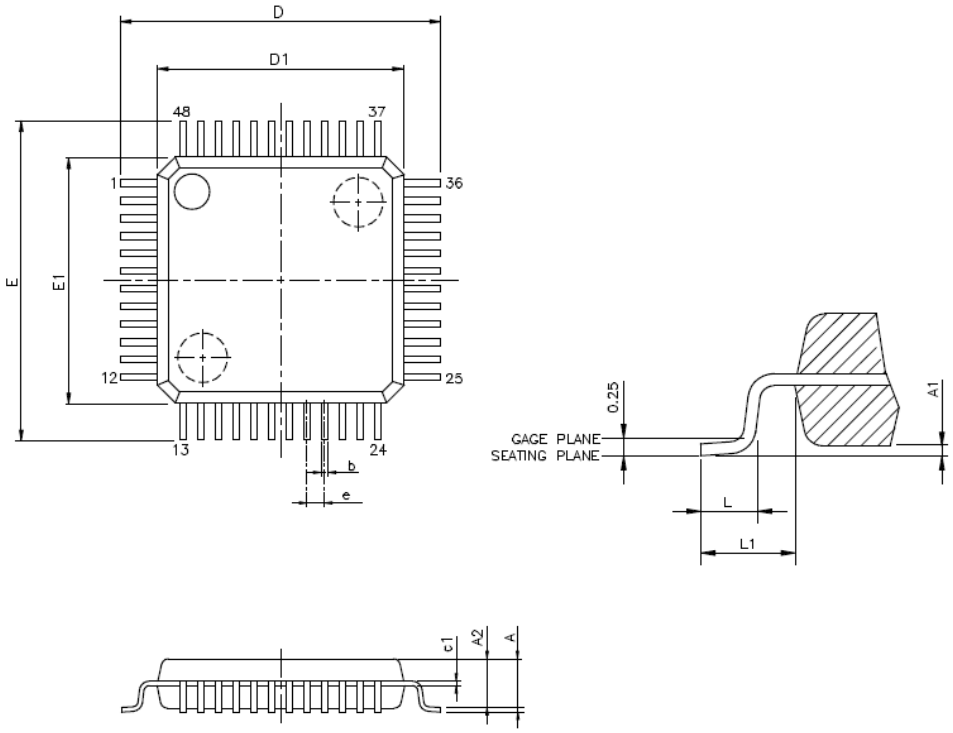
9.2 Package Information

9.2.1 SOP-16



Symbol	Inch		
	Min.	Nom.	Max.
A	0.053	-	0.069
A1	0.004	-	0.010
D	0.386	-	0.394
E	0.150	-	0.157
H	0.228	-	0.244
L	0.016	-	0.050
θ°	0°	-	8°

9.2.2 LQFP-48



SYMBOLS	Min.	Max.
A	-	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
B	0.17	0.27
L	0.45	0.75
L1	1 REF	

10 DISCLAIMER

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11 REVISION HISTORY

Date	Revision #	Description	Page
Jun 12, 2017	1.2	1. Add package information for LQFP-48 2. Section 5 SIGNAL DESCRIPTIONS remove Pin NO.	6,8, 9, 20, 21, 22
Aug 18, 2016	1.1	Add package information	6, 7, 18, 19, 21
Apr 14, 2016	1.0	release to version 1.0	17
Aug 27, 2015	0.1	Original	14