DATA SHEET

GPCH8001B

8-Channel Sound Controller with 512 KB OTP

AUG. 18, 2009

Version 1.1

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8-Channel Sound Controller with 512 KB OTP

1.GENERAL DESCRIPTION

The GPCH8001B embedded with an 8-bit processor, 512K bytes OTP ROM (or External 4M bytes maximal program ROM), 512 bytes working SRAM, 3 sets of 12-bit timer, 32 general I/Os, 1 set of 12-bit ADC with 4 channels input and 2 sets of 12-bit DAC. The microprocessor can implement software based on audio processing, functional control and others. For audio processing, melody and speech can be mixed into one output. The GPCH8001B is implemented with a high performance SPU voice engine to achieve 8-channel voice with ADPCM/PCM data. It operates over a wide voltage range from 2.2V through 5.5V, and it includes a Low Voltage Reset to assure system operating appropriately under low voltage condition. In addition, GPCH8001B provides sleep mode for power savings. It can be awakened from sleep mode by interrupt sources or by IOA's state change. There is a Serial Peripheral Interface (SPI) controller built in GPCH8001B to facilitate communicating with other devices and components. Also a SIO (Serial interface I/O) controller is featured which offers a one-bit serial interface to communicate with other devices.

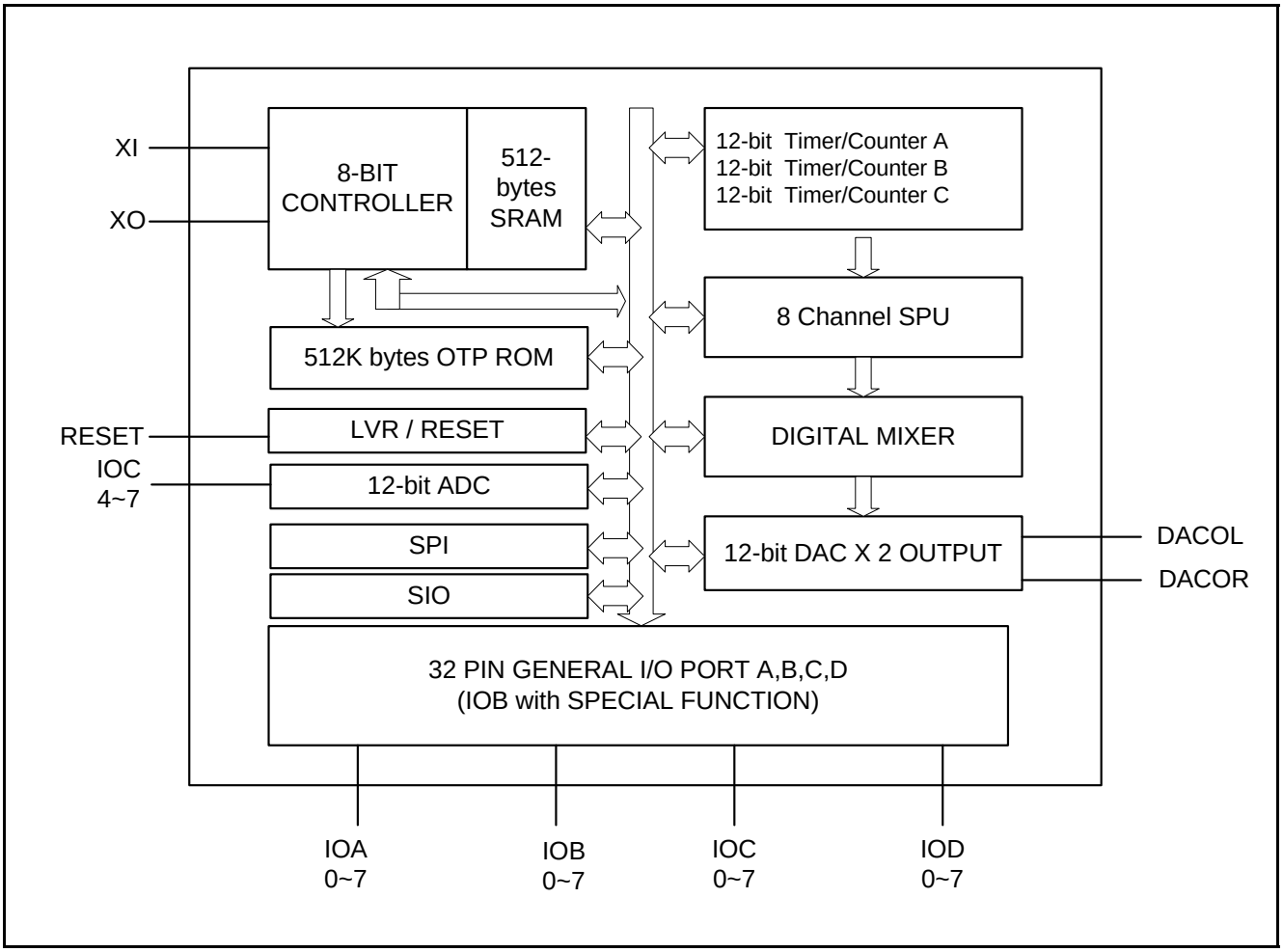
2.FEATURES

- Working Voltage: 2.4V - 5.5V
- CPU Speed: 7.159MHz.
- F_{OSC} = 14.318MHz (2 x CPU clock)
- ROM Size: 512K bytes OTP ROM (or can connect External ROM Max. 4M bytes)
- RAM Size: 512 bytes (Programmable RAM 384 bytes)
- Three 12-bit timers/counters, TMA/TMB/TMC (Programmable and Auto Reload)
- Sleep mode to reduce power
- Key change wake-up function
- 13 IRQs & 7 NMI Interrupts
- Watchdog Function
- Low Voltage Reset: 2.2V
- 32 general I/Os, including 8 general/special I/Os (Bit Programmable)
- 4-bit I/O with high sink current(20mA) for LED application
- IOA with 1M pull low function to prevent current leakage from error key touch
- Two 12-bit DAC outputs (D/A output: 4mA/channel)
- SPU(Sound Processing Unit) engine can output audio data of 15-bit resolution with 12-bit DAC to perform high quality sound
- IR PWM Output
- 8-channel SPU engine with ADPCM/PCM wave table
- Generalplus ICE_CORE embedded, new Application can be developed using SunMidiar® Development tools
- Tone color (Speech) with ADPCM algorithm to save memory usage
- 4-channel input of 12 bit ADC
- One Generalplus Serial I/O interface
- One SPI serial I/O interface

3.APPLICATION FIELD

- Talking Instrument Controller
- General Music Synthesizer
- Industrial Controller
- High End Toy Controller
- Intelligent Education Toys
- and more

4.BLOCK DIAGRAM



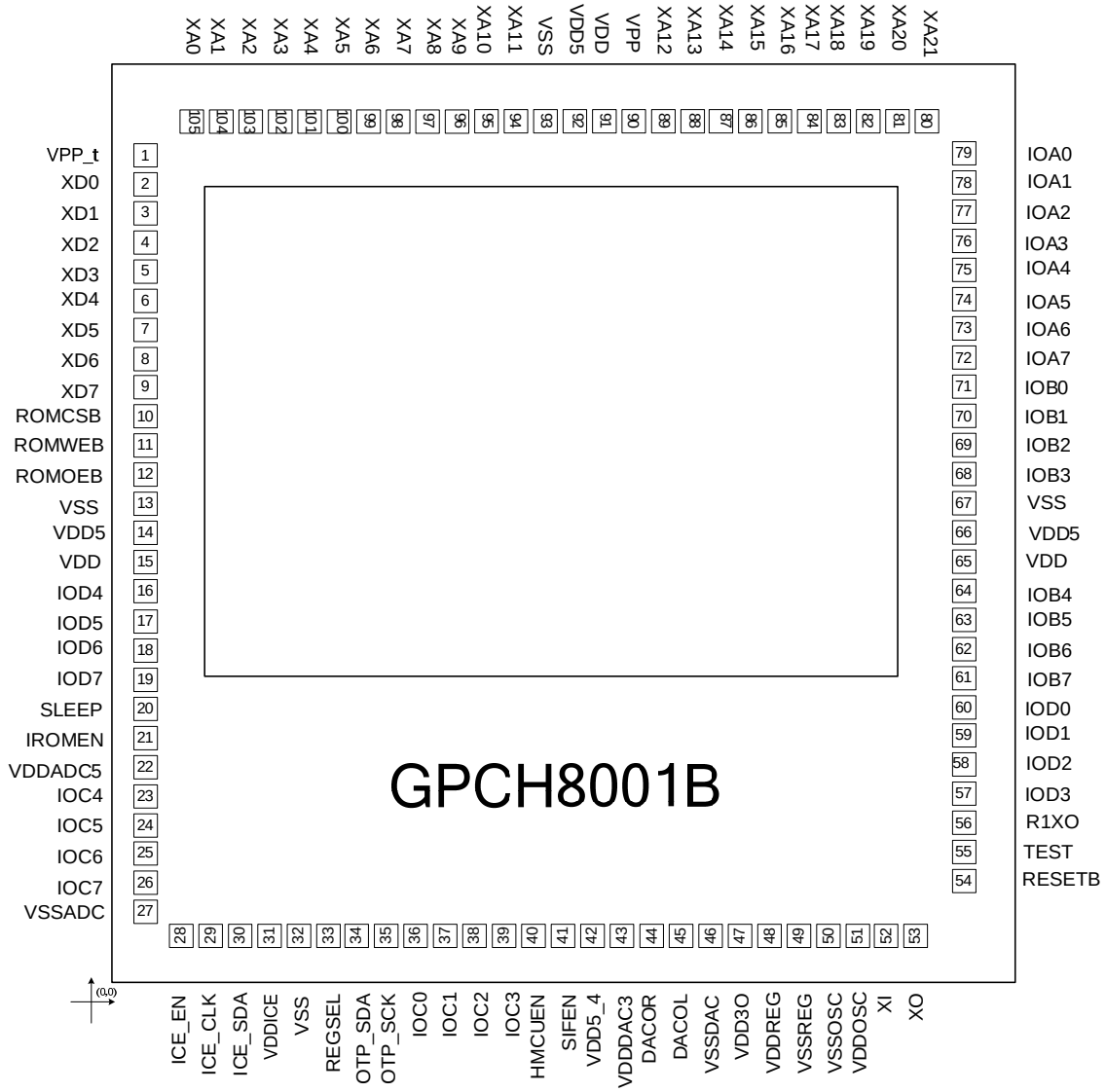
5.SIGNAL DESCRIPTIONS

Name	Pin. No.	LQFP 128 Pin No.	Type	Description	Pull hi/low/float
IO PORT					
IOA0~IOA7	79~72	83~90	I/O	Bi-directional IO ports, can be wakeup pins	-
IOB0~IOB7	71~68,64~61	82~79,75~72	I/O	Bi-directional IO ports	-
IOC0~IOC7	36~39,23~26	41~44,23~26	I/O	Bi-directional IO ports	-
IOD0~IOD7	60~57,16~19	71~68,23~26	I/O	Bi-directional IO ports	-
ROM/OTP Address & Data Bus interface					
XA0~XA21	105~94,89~80	122~111,106~97	O	Address of 4M byte external rom	-
XD0~XD8	2~9	2~9	I/O	Data bus of 4M byte external rom	-
ROMCSB	10	10	O	Rom chip select enable(active low)	-
ROMWEB	11	11	O	Rom write enable(active low)	-
ROMOEB	12	12	O	Rom output enable(active low)	-
IROMEN	21	21	I	Enable OTP(1) or external rom(0)	Floating
ICE related					
ICE_EN	28	33	I	ICE enable	Pull-low
ICE_CLK	29	34	I	ICE clock	Pull-low
ICE_SDA	30	35	I/O	ICE serial data bus	-
OTP related					
OTP_SCK	35	40	I	Serial clock for 512K byte OTP	Pull-low
OTP_SDA	34	39	I/O	Serial data bus for 512K byte OTP	-
SIFEN	41	46	I	Internal OTP controller enable (with serial interface)	Pull-hi
Clock related					
XO	53	58	O	Oscillator Crystal output	-
XI	52	57	I	Oscillator crystal input./R_{OSC} input	Floating
R1XO	56	67	I	R_{OSC} mode(1) or Crystal mode(0)	Floating in Crystal mode
POWER PAD					
VDD	65,91,15	76,108,15	I	Positive supply for logic (from VDD3O)	-
VSS	67,93,13,32	78,110,13,37	I	Ground reference for logic and I/O pins	-
VDDICE	31	36	I	Positive supply for logic ICE pads	-
VDD5, VDD5_4	66,92,14,42	77,109,14,47	I	Positive supply for I/O pins(2.4~5.5 V)	-
VDDADC5	22	22	I	Positive supply for ADC	-
VSSADC	27	27	I	Ground reference for ADC	-
VDDDAC3	43	48	I	Positive supply for DAC	-
VSSDAC	46	51	I	Ground reference for DAC	-
VDDREG	48	53	I	Positive supply for REGULATOR(2.4~5.5 V)	-
VSSREG	49	54	I	Ground reference for REGULATOR	-
VDD3O	47	52	O	3V/2.5V power output from regulator	-
VDDOSC	51	56	I	Positive supply for oscillator	-
VSSOSC	50	55	I	Ground reference for oscillator	-
VPP	90	107	I	OTP high voltage source for program	-
VPP_t	1	1	I	OTP high voltage source for program in test mode	-

Name	Pin. No.	LQFP 128 Pin No.	Type	Description	Pull hi/low/float
Others					
REGSEL	33	38	I	Always connect to VDD5	Floating
HMCUEN	40	45	I	Always connect to VSS	Floating
RESETB	54	65	I	External reset pin(active low)	Pull-hi
TEST	55	66	I	Test pin reserved for Generalplus testing	Pull-low
DACOR	44	49	O	Right DAC output	-
DACOL	45	50	O	Left DAC output	-
SLEEP	20	20	O	Sleep indicator	-

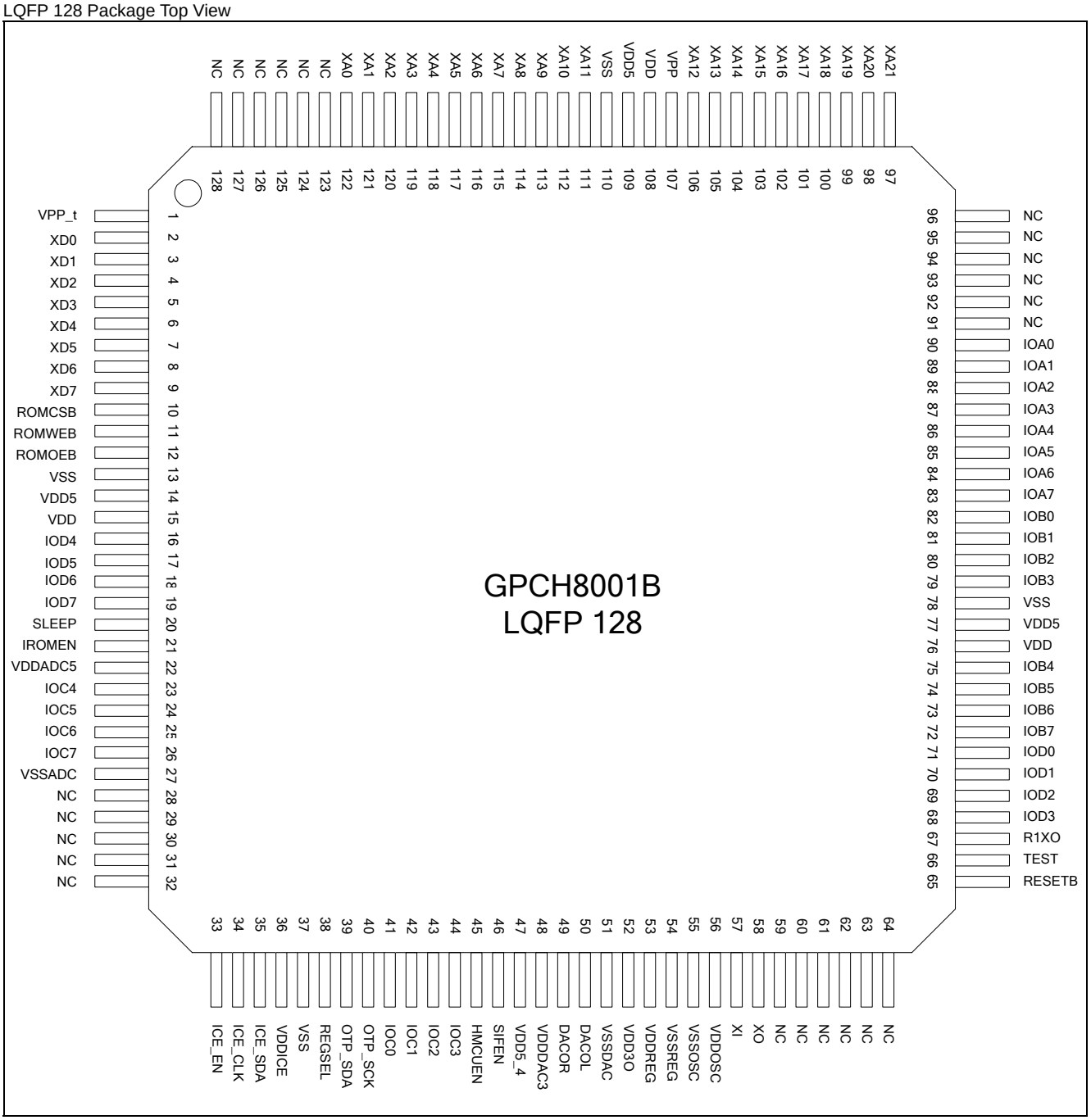
Total 105 pads

5.1. PAD Assignment



5.2. PIN Map

LQFP 128 Package Top View



6. FUNCTIONAL DESCRIPTIONS

6.1. SRAM

The 512-byte SRAM (including Stack) area is located in $000000~$0002FF.

6.2. ROM

GPCH8001B can be selected to use internal OTP ROM with 512k bytes or external ROM with maximum 4M bytes.

6.3. Low Voltage Reset

The GPCH8001B provides another important feature, Low Voltage Reset (LVR). Without LVR, the CPU may become unstable and malfunctioning-when operating voltage drops below 2.2V. It will reset all functions to the initial operational (stable) states when the voltage drops below 2.2V by LVR.

6.4. Interrupt

The GPCH8001B has two interrupt (INT) modes: IRQ (interrupt Request) and NMI (Non-Mask Interrupt Request). The interrupt controller controls 13 IRQs and 7 NMIs. A NMI cannot be interrupted by any other IRQs. An IRQ can be interrupted by a NMI and by a high priority IRQ.

Interrupt Source	Interrupt Name	Priority
Timer A	NMI_TIMER_A	NMI
Timer B	NMI_TIMER_B	NMI
Timer C	NMI_TIMER_C	NMI
CPU_CLOCK/1024	NMI_D1024	NMI
KEY	NMI_KEY	NMI
EXT	NMI_EXT	NMI
ADC	NMI_ADC	NMI
TIMER A	IRQ_TIMER_A	IRQ1
TIMER B	IRQ_TIMER_B	IRQ2
TIMER C	IRQ_TIMER_C	IRQ3
CPU_CLOCK/1024	IRQ_D1024	IRQ4
CPU_CLOCK/4096	IRQ_D4096	IRQ5
CPU_CLOCK/262144	IRQ_D262144	IRQ6
CPU_CLOCK/2097152	IRQ_D2097152	IRQ7
KEY	IRQ_KEY	IRQ8

Interrupt Source	Interrupt Name	Priority
EXT	IRQ_EXT	IRQ9
ADC	IRQ_ADC	IRQ10
SPU	IRQ_SPU	IRQ11
SPI	IRQ_SPI	IRQ12
SIO	IRQ_SIO	IRQ13

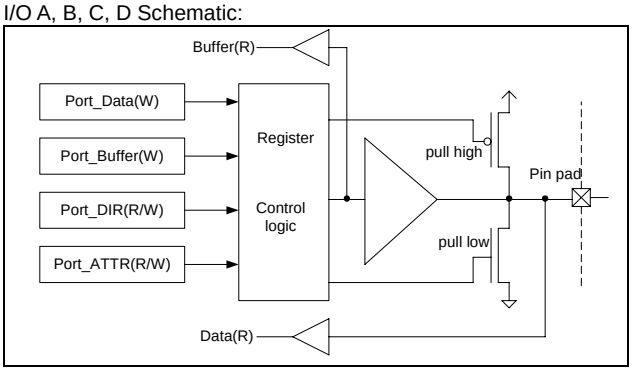
6.5. I/O

The purpose of input and output ports is to communicate with other devices. Four programmable I/O ports are built-in, including Port A, B, C, and D. The PortA is a general I/O with programmable wake-up capability. In addition to general I/O function, PortB also offers some special functions in certain pins. Refer to **Special Function in PortB**. PortC0~3 provides large sink current (20mA) for LED application. The Port C and Port D are sharing other module's function such as ADC, SPI, SIO, etc. Refer to **IO Share**.

6.5.1. I/O configuration

The following diagram represents the I/O schematic.

I/O A, B, C, D Schematic:



Port_Data and Port_Buffer are written into the same register but read from different nodes. The IOA [7:0] is the key wakeup port. To activate key wakeup function, first latch data on IOA_Data and enable the key wakeup function. Wakeup is triggered when the PortA state is different from first latched data. In addition to a general I/O port, PortB can be assigned to some special functions. A summary of PortB special functions is listed as follows. The next table lists IO sharing pins with ADC, SPI, SIO and etc.

Special function in PortB

PortB	Special Function	Function Description	Note
IOB5	PWMO IR	IR carrier frequency output	Refer to Timer/Counter section
IOB6	EXT	External interrupt source	Negative edge trigger INT(default)
	Feedback Output	Works with IOB7 by adding a RC circuit between them to get an OSC to EXT interrupt	-

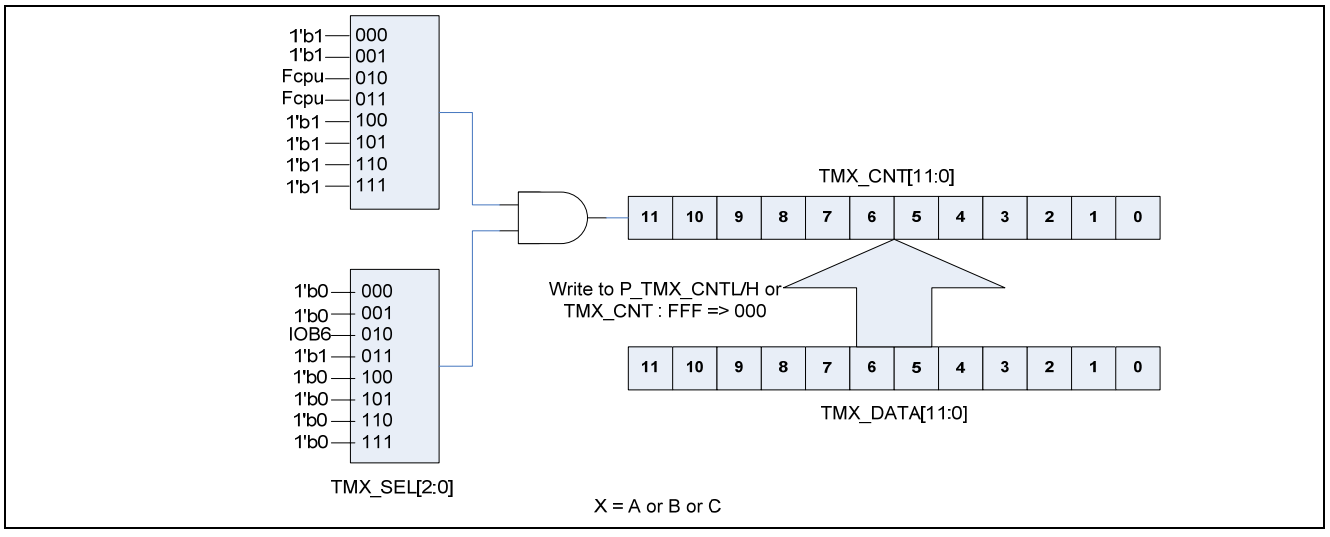
PortB	Special Function	Function Description	Note
IOB7	Feedback Input	Schmitt Inverter Input	-

IO Share

IO Pin	Share
IOC4	Linein 0
IOC5	Linein 1
IOC6	Linein 2
IOC7	Linein 3
IOD0	SPICSN
IOD1	SPICK
IOD2	SPIDO
IOD3	SPIDI
IOD4	SIO_SCK
IOD5	SIO_SDA

6.6. Timer/Counter (Timer A/Timer B/Timer C)

Three timers are embedded in GPCH8001B, Timer A, B and C. There three timers all have the same behavior which includes a 12-bit up counter and a preload register and programmable clock source. Timer A can also be the clock source of the software channel. The clock source of each timer can be set individually. Two clock sources including CPU clock and external clock can be selected individually or combined together for timer's clock source.



Select	Input 1	Input 2	Function	Comment
000	'1'	'0'	Disable	Disable
001	'1'	'0'	Disable	Disable
010	F_{CPU}	IOB6	Duration count by F_{CPU}	Duration count by F_{CPU}
011	F_{CPU}	'1'	Timer by F_{CPU}	Timer by F_{CPU}
100	'1'	'0'	Disable	Disable
101	'1'	'0'	Disable	Disable
110	'1'	'0'	Disable	Disable
111	'1'	'0'	Disable	Disable

6.7. Sleep, Wakeup and Watchdog

6.7.1. Sleep and Wakeup

Sleep mode is to save power by stopping clock running while device is not in use. When sleep acts, the device runs from operating mode to standby mode. Wake-up from sleep mode means turning back to operating mode.

1). Sleep: After power on reset, IC starts working until a sleep command is given. When a sleep signal is accepted, IC will turn off system clock and enter sleep mode.

2). Wake-up: While an IRQ/NMI interrupt signal is generated, GPCH8001B is waking up from sleep mode. While wake-up completed, program counter will continue to execute the next command.

6.7.2. Watchdog

The purpose of watchdog is to monitor system's operation normally. Within a certain period, watchdog must be cleared; otherwise, CPU assumes the program has been running in an abnormal condition and therefore, CPU will reset the system to the initial state and start running the program from program's beginning. It protects the system from incorrect code execution by generating a system reset when the watchdog timer overflows as a result of failure of software to clear the timer within 0.75 seconds. Watchdog function can be removed by option.

6.8. Speech and DAC

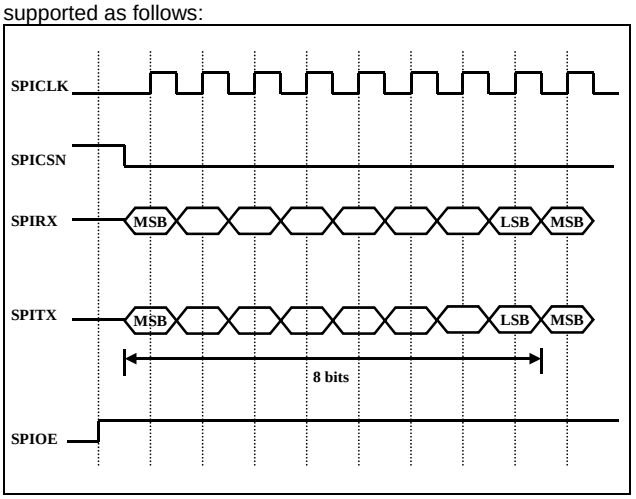
The GPCH8001B uses a high performance SPU voice engine to archive 8-channel voice with ADPCM/PCM. The SPU also supports automatic zero-crossing concatenating function. A hardware multiplier is also embedded in this SPU for software usage. The fixed address of RAM area $0000 - $007F is designed as address pointers and a data buffer for 8-channel speech/melody generation. There are two 12-bit D/As with 4mA driving current for DAC1 and DAC2.

6.9. Analog/Digital Converter

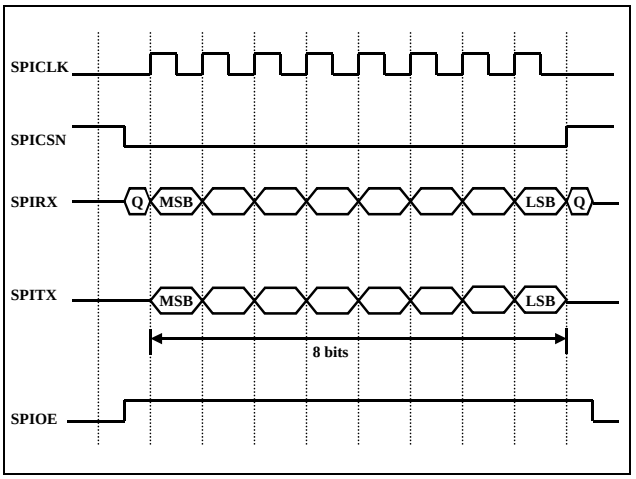
The 12-bit general purpose analog/digital converter (ADC) is embedded in GPCH8001B. The ADC with 4-channel input which can be selected by software programming with maximum 100KHz sampling rate. Key press interrupt generation is supported.

6.10. SPI Controller

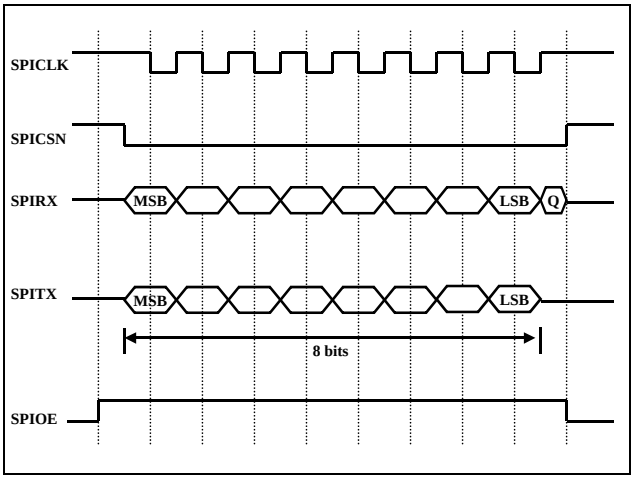
A Serial Peripheral Interface (SPI) controller is built in GPCH8001B to facilitate communicating with other devices and components. There are four control signals on SPI including SPICSN, SPICLK (SCK), SPIRX (SDI), and SPITX (SDO); the four signals are shared with PortD0, PortD1, PortD2 and PortD3. While SPI module is enabled by corresponding control bit. These four pins cannot be GPIOs and any setting on corresponding GPIO control register will have no effect. Four types of timing are supported as follows:



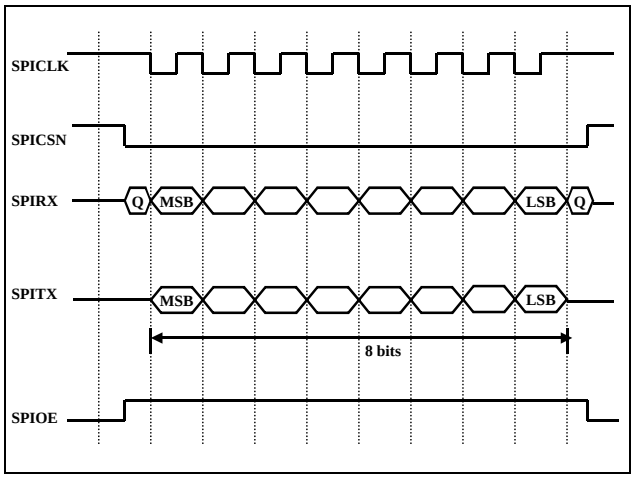
Master Mode, SPO = 0, SPH=0



Master Mode, SPO = 0, SPH=1



Master Mode, SPO = 1, SPH=0



Master Mode, SPO = 1, SPH=1

6.11. Generalplus Serial IO Controller

SIO (Serial interface I/O) controller is Generalplus' serial interface, which offers a one-bit serial interface that communicates with other devices from Generalplus. This serial interface is capable of transmitting or receiving data via two I/O pins, SCK and SDA. The SCK and SDA are shared with IOD4 and IOD5 respectively.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see DC Electrical Characteristics.

7.2. DC Characteristics (VDD5/VDD5_4 = 3.0V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.2	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	14	-	mA	F_{CPU} = 7.0MHz, no load, playing midi with inner OTP ROM, DAC enabled
			21			F_{CPU} = 7.0MHz, no load, playing midi with AMIC flash (model: A29L040-70), DAC enabled
Standby Current	I_{STB}	-	-	10.0	μA	VDD5/VDD5_4 = 3.0V
OSC Frequency	F_{OSC}	-	-	15	MH_Z	VDD5/VDD5_4 = 3.0V
Input High Level	V_{IH}	0.7 VDD	-	VDD	V	-
Input Low Level	V_{IL}	VSS	-	0.3VDD	V	-
Audio Output Current	I_{AUD}	-	-4.3	-	mA	-
Output High Current	I_{OH}	-2.6	-	-	mA	VDD5/VDD5_4 = 3.0V, V_{OH} = 2.7V
Output Low Current (IOA7:0, IOB7:0, IOC7:4, IOD7:0)	I_{OL1}	2.8	-	-	mA	VDD5/VDD5_4 = 3.0V, V_{OL} = 0.3V
Output Low Current (IOC3:0)	I_{OL2}	12	-	-	mA	VDD5/VDD5_4 = 3.0V, V_{OL} = 0.3V
Input Pull-Low Resister (PA7:0)	R_{PL}	-	1800	-	KΩ	V_{IN} = VDD5/VDD5_4
Input Pull-High Resister (PA7:0, PB7:0, PC7:0)	R_{PH}	-	170	-	KΩ	V_{IN} = VSS

7.3. DC Characteristics (VDD5/VDD5_4 = 5.0V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	21	-	mA	F_{CPU} = 7.0MHz , no load, playing midi with inner OTP ROM, DAC enabled
			37			F_{CPU} = 7.0MHz , no load, playing midi with AMIC flash (model:A29L040-70), DAC enabled
Standby Current	I_{STB}	-	-	15.0	μA	VDD5/VDD5_4 = 5.0V
OSC Frequency	F_{OSC}	-	-	15	MHz	VDD5/VDD5_4 = 5.0V

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input High Level	V_{IH}	0.7 VDD	-	VDD	V	-
Input Low Level	V_{IL}	VSS	-	0.3VDD	V	-
Audio Output Current	I_{AUD}	-	-7.2	-	mA	-
Output High Current	I_{OH}	-6.0	-	-	mA	VDD5/VDD5_4 = 5.0V, V_{OH} = 4.5V
Output Low Current (IOA7:0, IOB7:0, IOC7:4, IOD7:0)	I_{OL1}	6.0	-	-	mA	VDD5/VDD5_4 = 5.0V, V_{OL} = 0.5V
Output Low Current (IOC3:0)	I_{OL2}	27	-	-	mA	VDD5/VDD5_4 = 5.0V, V_{OL} = 0.5V
Input Pull-Low Resister (PA7:0)	R_{PL}	-	900	-	KΩ	V_{IN} = VDD5/VDD5_4
Input Pull-High Resister (PA7:0, PB7:0, PC7:0, PD7:0)	R_{PH}	-	60	-	KΩ	V_{IN} = VSS

7.4. DAC Characteristics (VDD5 = 3.0V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Resolution of DAC	RESO	-	-	12	bit
THD+N (f=1kHz)	SNR	-	0.1	-	%
Noise at no signal	-	-	-80	-	dBr A
Dynamic range(-60dB)	-	-	-75.9	-	dBr A
Sample Rate	F_S	-	-	400K	Hz

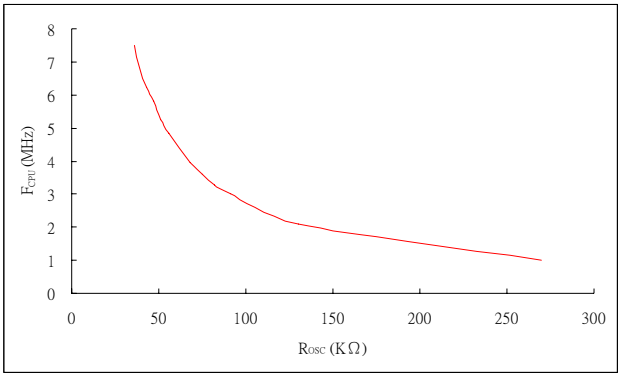
7.5. Regulator Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	2.4	4.5	5.5	V
Maximum Current Output	IREGO	-	-	60	mA
Output Voltage	VREGO	2.4	3	3.3	V
Standby Current	IRGES	-	7.2	-	uA

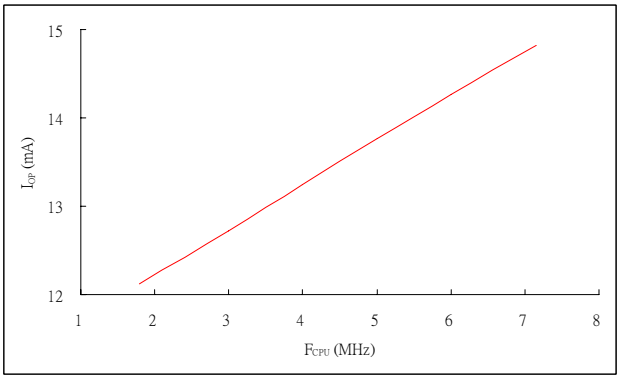
7.6. ADC Characteristics (VDD5 = 3.0V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Resolution of ADC	RESO	-	-	12	bits
Signal-to-Noise Plus Distortion of ADC from Line in	SINAD	-	58	-	dB
Effective Number of Bit	ENOB	-	9.3	-	bits
Integral Non-Linearity of ADC	INL	-	±1.0	-	LSB
Differential Non-Linearity of ADC	DNL	-	±0.6	-	LSB
No Missing Code	-	-	11	-	bits
AD Conversion Rate	F_{CONV}	-	-	100K	Hz
Supply Voltage	VADC	2.2	5	5.5	V

7.7. The Relationships between the R_{OSC} and the F_{CPU}

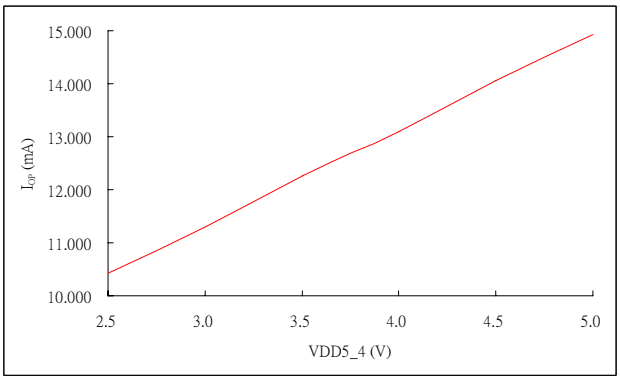


7.8. The Relationships between the F_{CPU} and the I_{OP}



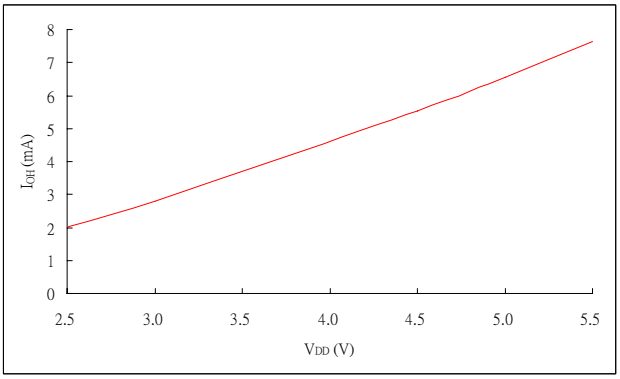
7.9. The Relationships between the I_{OP} and the VDD

7.9.1. F_{CPU} = 7.159 MHz. VDD = VDD5_4



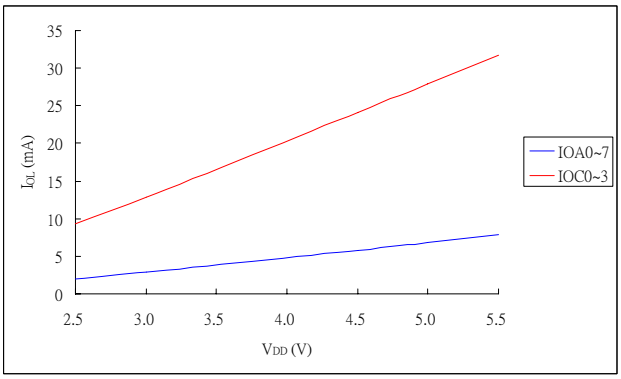
7.10. The Relationships between the I_{OH} and the VDD

7.10.1. V_{OH} = 0.9VDD



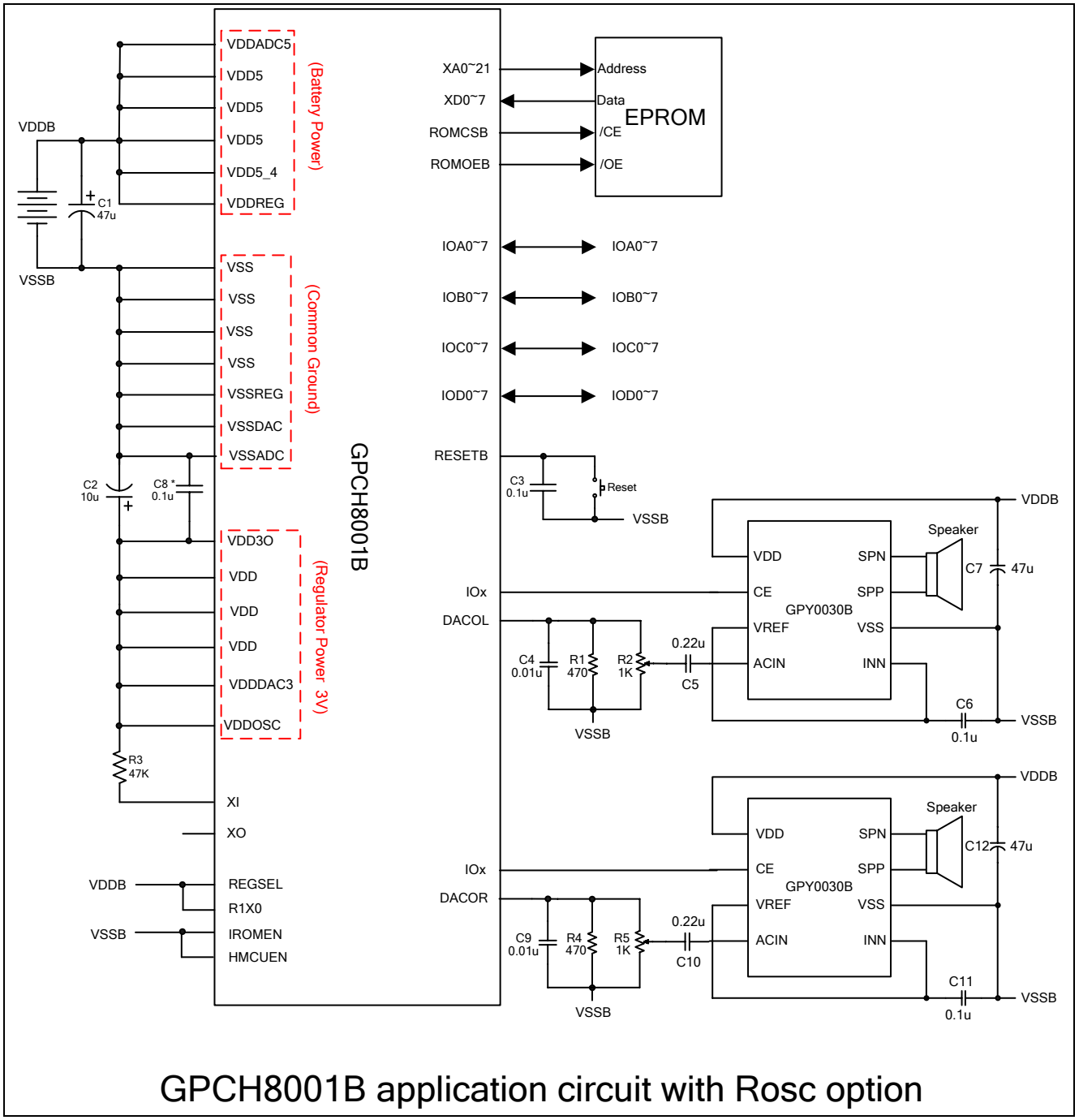
7.11. The Relationships between the I_{OL} and the VDD

7.11.1. V_{OL} = 0.1VDD



8.APPLICATION CIRCUITS

8.1. GPCH8001B Application Circuit with R_{OSC} Option



GPCH8001B application circuit with Rosc option

Note*: This capacitor can be removed if there is good power line layout on PCB that no harm to sound quality.

Note: Important note to power connection:

(a) Battery or Power supply connects to VDDB (including VDDREG, VDD5 , VDD5_4 and VDDADC5, 2.4V~5.5V)

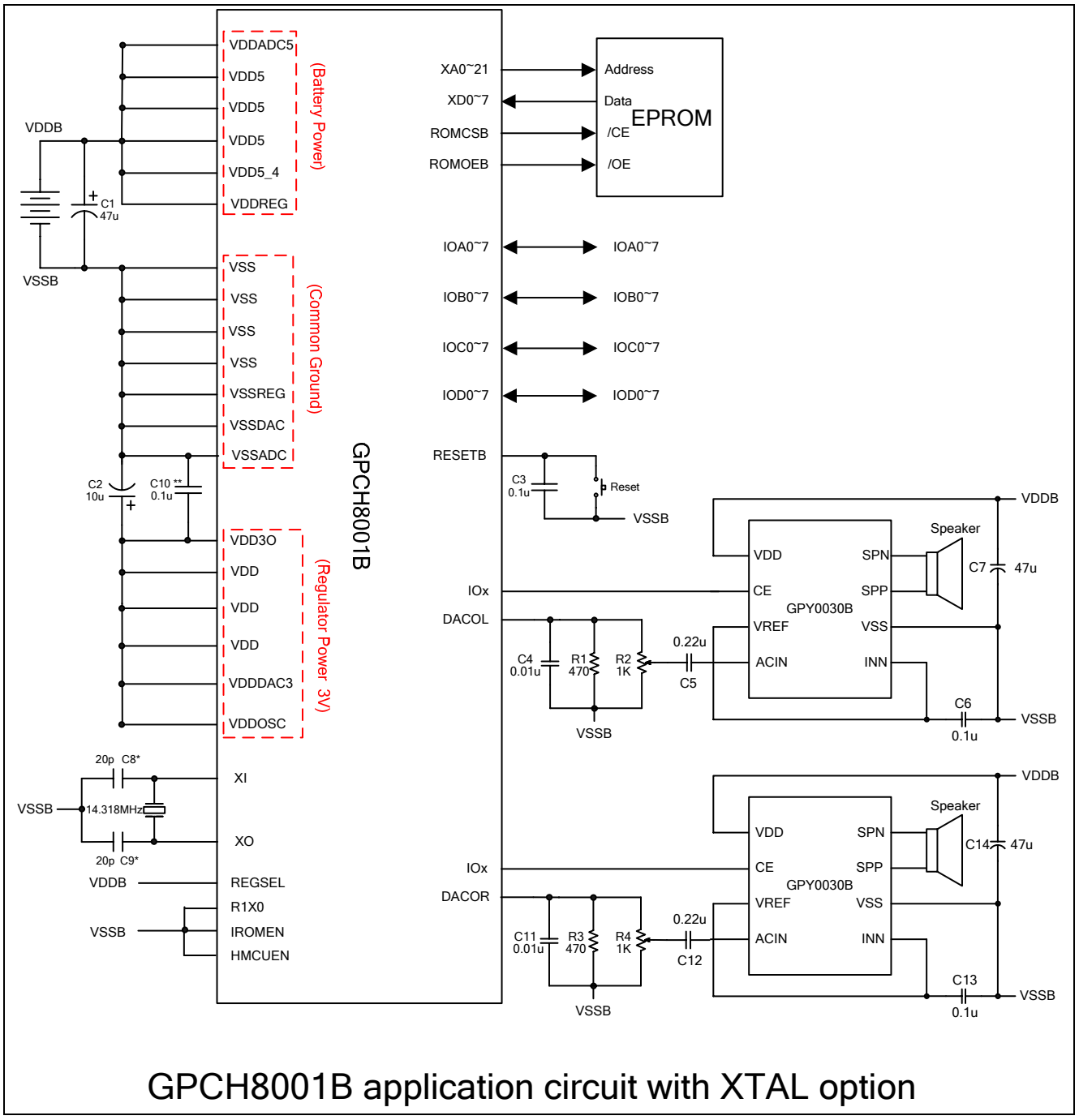
(b) VDD3O is internal regulator output that supplies power to VDD, VDDDAC3, VDDOSC, etc. Connect VDD3O, VDD, VDDDAC3 and VDDOSC all together.

(c) VDDB should NOT be connected to VDD3O, VDD, VDDDAC3, VDDOSC, etc.

(d) The built-in regulator can NOT be disabled, so user should NOT bypass this regulator.

(e) Recommended capacitor placement for power distribution on PCB: C1 close to battery, C2 close to VDD3O pad and C8 close to VDDDAC3 pad.

8.2. GPCH8001B Application Circuit with Crystal Option



GPCH8001B application circuit with XTAL option

Note*: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note:** This capacitor can be removed if there is good power line layout on PCB that no harm to sound quality.

Note: Important note to power connection:

(a) Battery or Power supply connects to VDDB (including VDDREG, VDD5 , VDD5_4 and VDDADC5, 2.4V~5.5V)

(b) VDD3O is internal regulator output that supplies power to VDD, VDDDAC3, VDDOSC, etc. Connect VDD3O, VDD, VDDDAC3 and VDDOSC all together.

(c) VDDB should NOT be connected to VDD3O, VDD, VDDDAC3, VDDOSC, etc.

(d) The built-in regulator can NOT be disabled, so user should NOT bypass this regulator.

(e) Recommended capacitor placement for power distribution on PCB: C1 close to battery, C2 close to VDD3O pad and C10 close to VDDDAC3 pad.

8.3. Current Mode DAC Speaker Driver

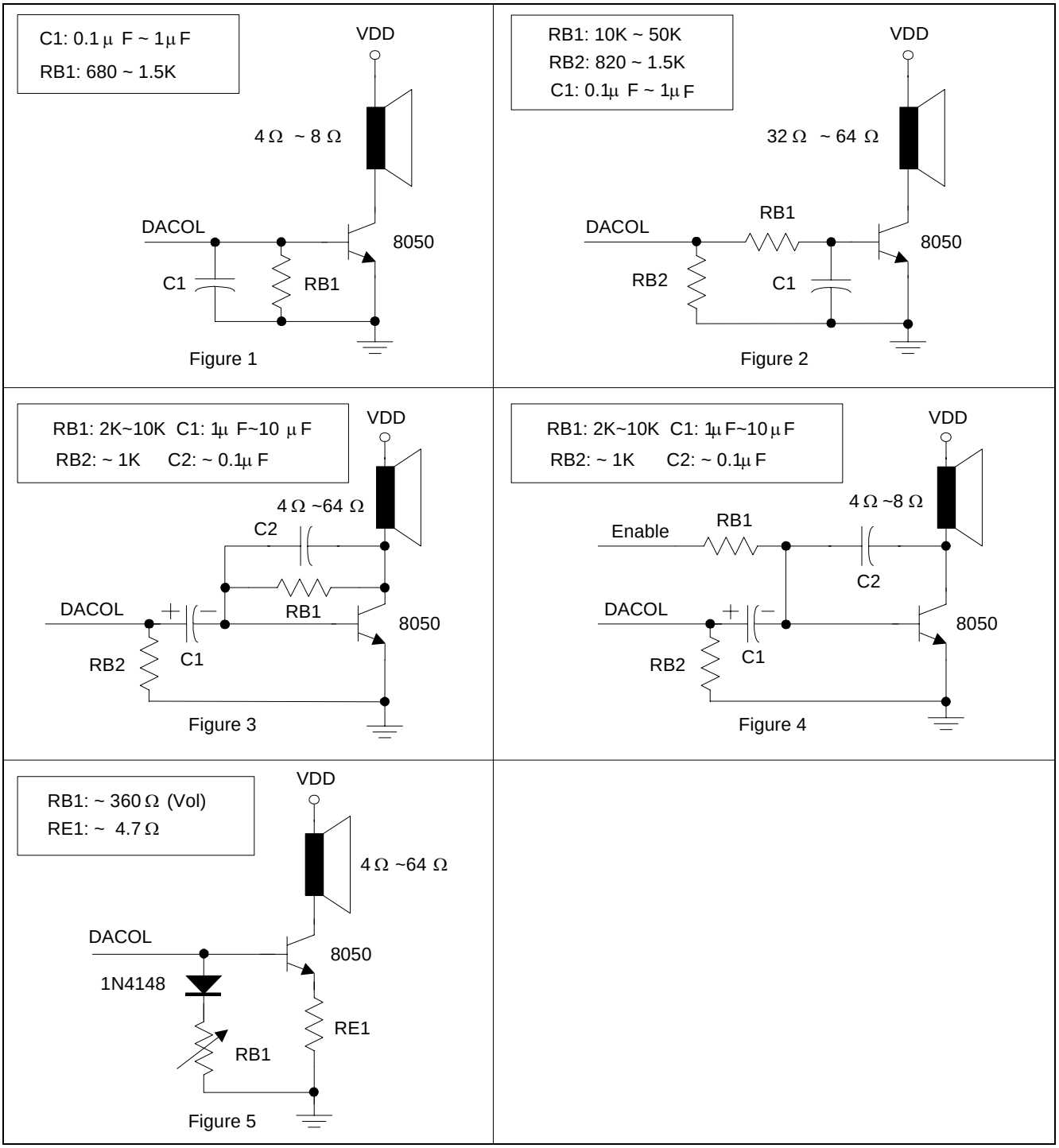


Figure 1: The simplest CKT uses with low impedance speaker. It has high operation current, but the cost is the cheapest.

Figure 2: It is the same as Figure 1 but a high impedance speaker is used.

Figure 3: The CKT has low pass filter. It can provide higher speech quality, but it always takes high operation current.

Figure 4: Improved version of Figure 3. The standby current can be controlled by enable pin.

Figure 5: The current mirror mode. It is able to control the volume. In addition, it has more stable and lower operation current than Figure 1-3.

9.PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPCH8001B-NnnV-C	Chip form
GPCH8001B-NnnV-QL09x	Halogen Free Package

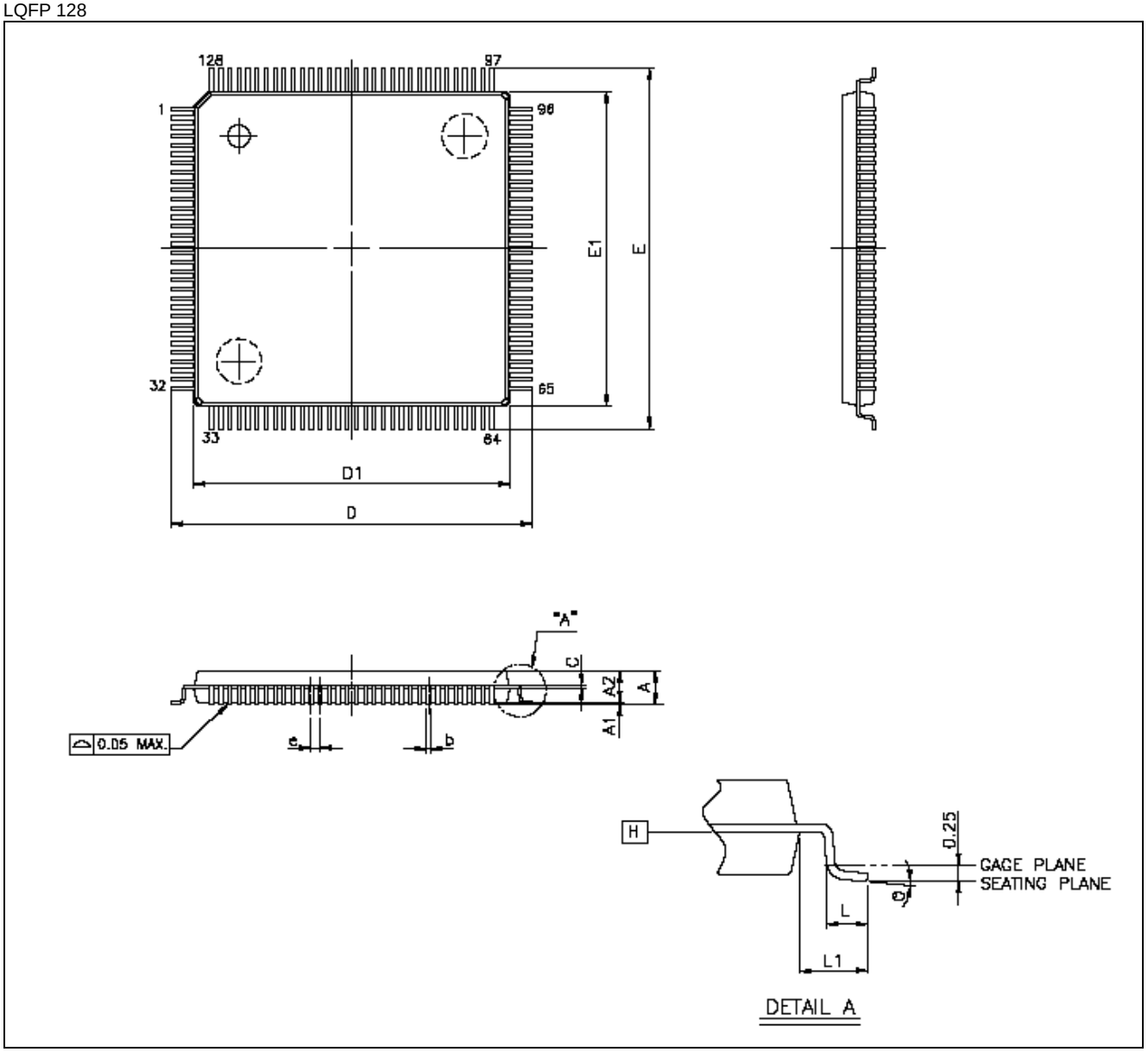
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

9.2. Package Information

LQFP 128



Symbol	Millimeter		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15

Symbol	Millimeter		
	Min.	Nom.	Max.
A2	1.35	1.40	1.45
D	16.00 BCS.		
D1	14.00 BCS.		
E	16.00 BCS.		
E1	14.00 BCS.		
e	0.40 BCS.		
θ	0°	3.5°	7°
b	0.13	0.16	0.23
c	0.09	-	0.20
L	0.45	0.60	0.75
L1	1.00 REF		

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
AUG. 18, 2009	1.1	1. Modify 7.2 DC Characteristics (VDD5 = 3.0V, TA = 25℃) 2. Modify 7.3 DC Characteristics (VDD5 = 5.0V, TA = 25℃)	13 14
JUN. 02, 2009	1.0	Original	22