DATA SHEET

GPCL171A

Low Power Sound Controller with 512KB OTP ROM

Dec 25, 2012

Version 1.1

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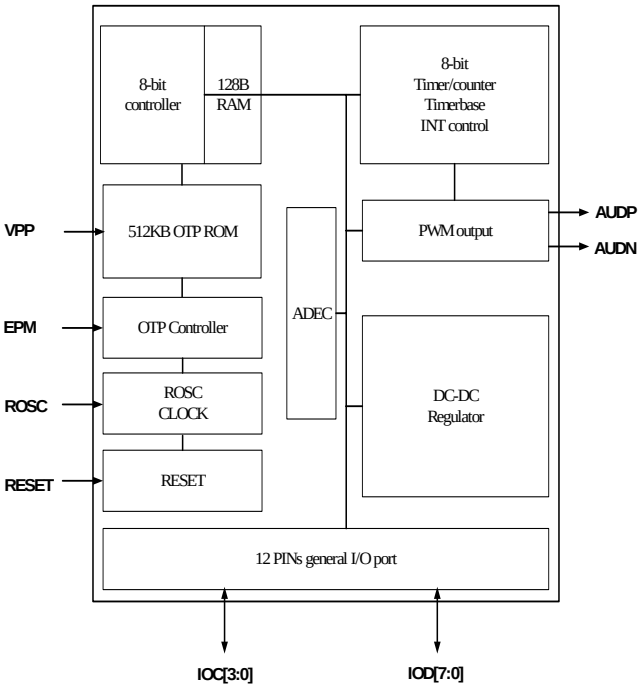
LOW POWER SOUND CONTROLLER WITH 512KB OTP ROM

1. GENERAL DESCRIPTION

The GPCL171A, a speech/wavetable synthesizer, equips an 8-bit CMOS microprocessor, 512K-byte OTP ROM, and 128-byte working SRAM. Other primary features include two 8-bit Timer/Counters which can cascade to one 16-bit timer/counter, 12 software selectable I/Os and a pair of PWM outputs. It is designed for widely input voltage (by User Option, 1 Cell: 1.0V-1.7V; 2 Cell: 1.3V-3.6V), and the circuit works at a stable and programmable pumped voltage (by user's option, 1 Cell: 3.3V - 3.9V; 2 Cell: 3.3V - 4.5V). Plus, Clock Stop mode is built-in for power savings. The unique power saving mode saves the RAM content, but it freezes the oscillator to stop executing other functions. The maximum CPU frequency can run up to 6MHz and the instruction cycle is two clock cycles (min.) ~ six clock cycles (max).

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- 512K bytes OTP ROM
- 128-byte working SRAM
- Software-based audio processing
- Wide input voltage:（user's option）
  - 1 Cell: 1.0V-1.7V
  - 2 Cell: 1.3V-3.6V
  - *Lower input voltage can drive lighter loading only.
- Pumped voltage*:（user's option）
  - 1 Cell: 3.3V-3.9V ; step: 0.3V
  - 2 Cell: 3.3V-4.5V ; step: 0.3V
  - *The output pumped voltage is greater than or equal to input voltage.
- Operating clock: 6.0MHz
- Supports ROSC only
- Standby mode (Clock Stop mode) for power savings.
  - 1 Cell: Max. 5.0μA @ 1.5V
  - 2 Cell: Max. 10.0μA @ 3.0V
- 12 general I/Os
- Low Voltage Reset (LVR) function
- Two 8-bit timer/counters and can cascade to one 16-bit timer/counter
- Six INT sources
- Key wakeup function
- Watchdog function
- A pair of PWM outputs

4. APPLICATION FIELD

- Intelligent education toys
  - Ex. Pattern to voice (animal, car, color, etc.)
  - Spelling (English or Chinese)
  - Math
- Advanced toy controller
- General speech synthesizer

5. SIGNAL DESCRIPTIONS

Mnemonic	Type	Description
VSSP	P	Ground reference for VPP
VPP	P	7.5V Power supply voltage input, for OTP programming, NC at normal run
AUDP	O	Audio output
AVDD	P	PWM power pad
AVSS	P	PWM ground pad
AUDN	O	Audio output
REG_IN	I	Regulator Power Pad.
REG_OUT	O	Regulator Output Power Pad.
CVDD	P	Digital power pad
EPM	I	Program control pin, NC at normal run
RESETB	I	Reset pin, low active to reset whole system
IOD0	I/O	Bit-controlled programmable I/O pins
IOD1	I/O	In input mode, Port D can be either pure or pull-low state.
IOD2	I/O	In output mode, Port D can be a buffer.
IOD3	I/O	Pins in Port D are the key wake-up I/O pins.
IOD4	I/O	
IOD5	I/O	
IOD6	I/O	
IOD7	I/O	
IOC0	I/O	Nibble-controlled programmable I/O pins
IOC1	I/O	In input mode, Port C can be either pure or pull-low state. In output mode, Port C can be a buffer.
IOC2	I/O	
IOC3	I/O	
TEST	I	TEST pin, NC
ROSC	I	ROSC resistor input (Resistor must be connected to VDD.)
VDD	P	Power Supply Voltage Input Pad.
VSS	P	Ground reference.
VIN	P	DC-DC: Power pad
Lpump	I	DC-DC: Inductance input (Inductance must be connected to VIN)
VDDO	P	DC-DC: Pumped voltage output
VSSIN	P	DC-DC: Ground pad

6. FUNCTION DESCRIPTIONS

6.1. CPU

The microprocessor in GPCL171A is an 8-bit high performance processor equipped Accumulator, Program Counter, X and Y Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure). The maximum CPU speed of 6.0MHz is able to bring you clearer speech and music as well as achieving the best performance.

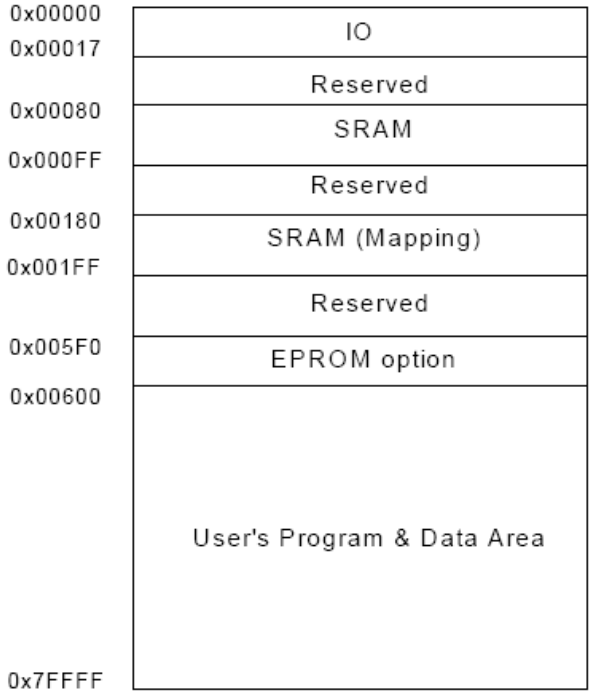
6.2. RAM Area

The total RAM size is 128-byte (including Stack) starting from address $0080 through $00FF or mapping to $0180 through $01FF.

6.3. OTP ROM Area

The GPCL171A provides a 512K-byte OTP ROM that can be defined as the program area, audio data area or both.

6.4. Map of Memory and I/Os

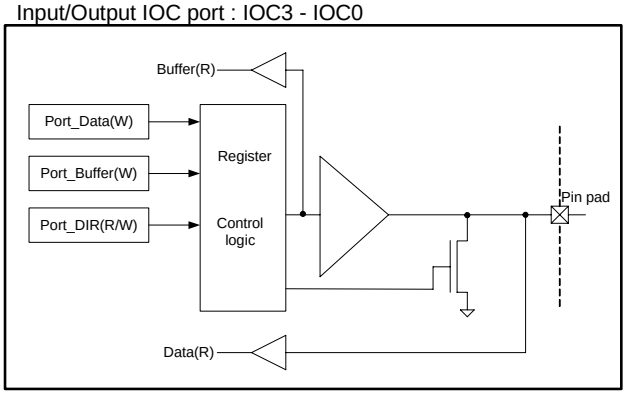


6.5. I/O Port

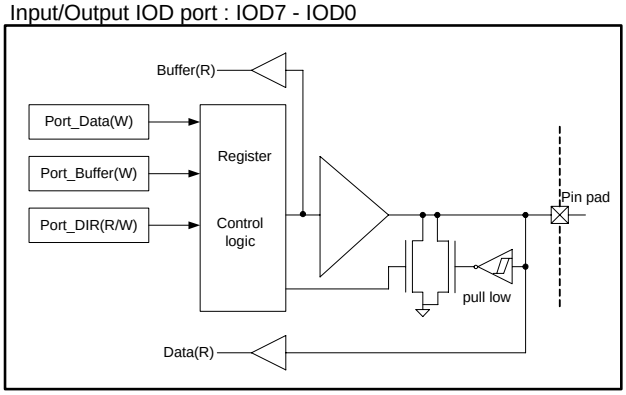
There are 12 IOs (IOC3-0 and IOD7-0) in the GPCL171A; IOC3-0 is nibble-controlled IO, but IOD7-0 is bit-controlled IO. They can be programmed as input (pure input or pull-low) or output buffer. A pull-low input IOD7-0 keeps a less impedance to get better noise immunity. While pressing the key (IOD7-0 to VDD), a larger impedance is retained to save DC power.

6.6. IO Port Configuration

Input/Output IOC port : IOC3 - IOC0



Input/Output IOD port : IOD7 - IOD0



6.7. DC-DC

The GPCL171A can work with widely input voltage (By User Option, 1 Cell: 1.0V-1.7V; 2 Cell: 1.3V-3.6V). Inside the chip, it is implemented a high efficient DC-DC circuit. The DC-DC circuit pumps input voltage to programmed voltage (By User Option, 1 Cell: 3.3V-3.9V; 2 Cell: 3.3V-4.5V) that supplies chip as working voltage.

6.8. Power Saving Mode

The GPCL171A includes a power saving mode (Standby mode) for those applications that require very low standby current. To enter standby mode, the wake-up register must be enabled and then stop the CPU clock by writing the STOP CLOCK register to enter standby mode. In such mode, RAM and I/Os will remain in their previous states until awake. Port IOD7-0 is the only wake-up source in the GPCL171A. After GPCL171A wakes up, the internal CPU will stay at RESET State for a period (Tw) and then continue to execute the program. Wake-up reset will neither affect RAM, nor I/Os.

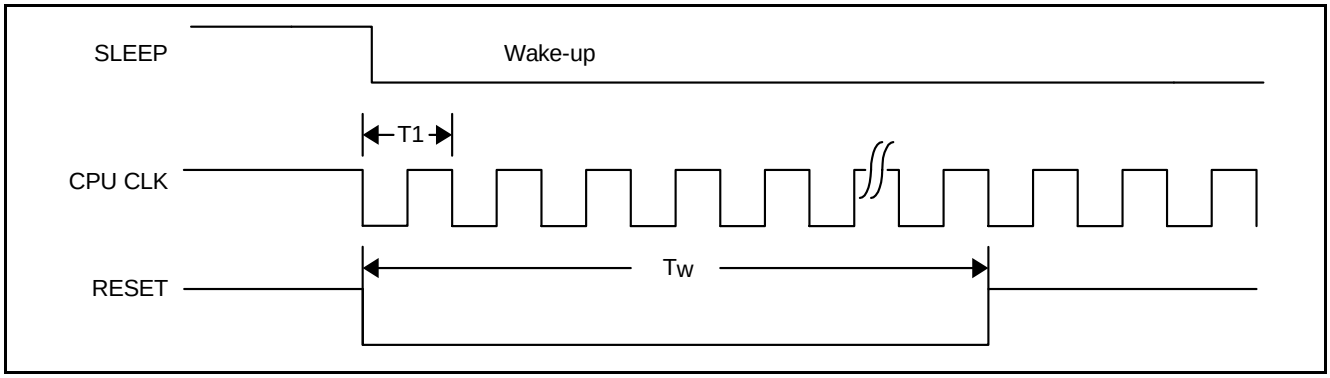


FIG. 1

$T1 = 1 / (F_{CPU})$

6.9. Timer/Counter

The GPCL171A has two 8-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer, but TMB can be used as a timer or a counter. In the timer mode, TMA and TMB are re-loaded up-counters. When the timer rollovers from $FF to $00, the carry (overflow) signal will make the user's preset value to be loaded into timer automatically and count up again. At the same time, the carry signal will generate an INT signal if the corresponding bit is enabled in the INT ENABLE register. Suppose TMB is specified as a counter, it can be reset by loading #00 into the counter. After the counter has been activated, the value in the counter can also be read at the same time. The read instruction will neither affect the value of the counter nor reset it.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	8-BIT TIMER	CPU CLOCK (T) or T/8, T/64, TMB overflow
TMB	8-BIT TIMER	T, T/65536, EXTCLK, 0, 1

6.10. Speech and Melody

In speech synthesis, the NMI is utilized for accurate sampling frequency. User can store the speech data in ROM and play it back with realistic sound quality. Several algorithms are recommended for high fidelity and sound compression: PCM, ADPCM, SACM-A3400 and SACM-A3400 Pro.

6.11. User Option

■ Watchdog option $5F3[5]: The watchdog is designed for recovering system from abnormal operation.

1: enable

0: disable

■ BTSEL Option: For 1 Cell / 2Cell Select.

2 Cell: $5F3 = 11X11001.（X: Watchdog Option）

1 Cell: $5F3 = 00X11001.（X: Watchdog Option）

■ Security Option $5F7[7]: For data security.

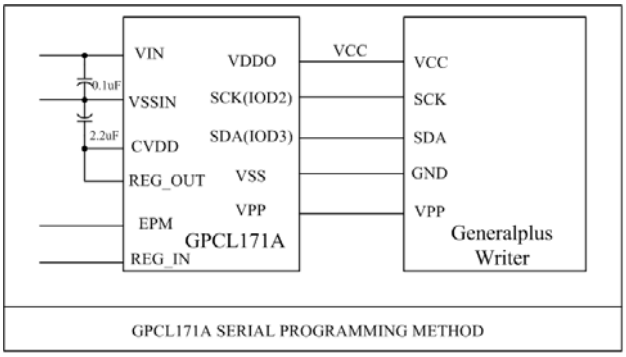
1: Security disable

0: Security enable

■ $5F0 has to be set 9Ah; $5F1 must be set 87h; $5F2 has to be set 18h; $5F6 has to be set 00h.

All the above option bits can be set by G+ IDE.

6.12. OTP Programming Circuit



Note1: Don't connect any component with IOD2 and IOD3 while programming.

Note2: Connect EPM to VCC during OTP programming cycle, and keep it floating in normal run.

Note3: Make sure the power source of Generalplus writer is 18 Volts.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device.

7.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC}	-	-	6.0	MHz	VIN = 1.0V - 3.6V

7.3. Power Characteristics (1 Cell, TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage (Min.)*	VIN	1.0	-	-	V	I(VDD)=40mA@VDD=3.3V, L=22uH/0.5W
Input Voltage (Max.)	VIN	-	-	1.7	V	-
Operating Voltage**	VDD	3.3	-	3.9	V	-
Standby Current	I_{STBY}	-	-	5.0	μA	VIN = 1.5V

*As I(VDD) is greater than the value of test condition; VDD can be observed voltage drop.

**VDD is the pumped voltage. It is greater than or equal to input voltage. It is possible to be lower with heavy loading under operating.

7.4. Power Characteristics (2-Cell, TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage (Min.)*	VIN	1.3	-	-	V	I(VDD)=40mA@VDD=3.3V, L=22uH/0.5W
Input Voltage (Max.)	VIN	-	-	3.6	V	-
Operating Voltage**	VDD	3.3	-	4.5	V	-
Standby Current	I_{STBY}	-	-	10.0	μA	VIN = 3.0V

*As I(VDD) is greater than the value of test condition; VDD can be observed voltage drop.

**VDD is the pumped voltage. It is greater than or equal to input voltage. It is possible to be lower with heavy loading under operating.

7.5. DC Characteristics (1 Cell, VDD=3.9V,T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	I_{OP}	-	10	-	mA	F_{osc} = 6.0MHz @ VDD=3.9V(no load)
Audio Output Current	I_{AUD}	-	170	-	mA	VDD = 3.9V, 8 Ohms load
Input High Level	V_{IH}	0.7 VDD	-	-	V	VDD = 3.9V
Input Low Level	V_{IL}	-	-	0.3 VDD	V	VDD = 3.9V
Output Source Current	I_{OH}	-	11	-	mA	VDD = 3.9V, V_{OH} = 2.73V
Output Sink Current	I_{OL}	-	25	-	mA	VDD = 3.9V, V_{OL} = 1.17V
Input Resistor (IOC)	R_{IN}	-	100	-	KΩ	VDD = 3.9V, V_{IN} = VDD
Input Resistor (IOD)	R_{IN}	-	195	-	KΩ	VDD = 3.9V, V_{IN} = VDD

7.6. DC Characteristics (1 Cell, VDD=3.3V,T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	I_{OP}	-	8	-	mA	F_{osc} = 6.0MHz @ VDD=3.3V(no load)
Audio Output Current	I_{AUD}	-	135	-	mA	VDD = 3.3V, 8 Ohms load
Input High Level	V_{IH}	0.7 VDD	-	-	V	VDD = 3.3V
Input Low Level	V_{IL}	-	-	0.3 VDD	V	VDD = 3.3V
Output Source Current	I_{OH}	-	8	-	mA	VDD = 3.3V, V_{OH} = 2.31V
Output Sink Current	I_{OL}	-	19	-	mA	VDD = 3.3V, V_{OL} = 0.99V
Input Resistor (IOC)	R_{IN}	-	110	-	KΩ	VDD = 3.3V, V_{IN} = VDD
Input Resistor (IOD)	R_{IN}	-	250	-	KΩ	VDD = 3.3V, V_{IN} = VDD

7.7. DC Characteristics (2 Cell, VDD=4.5V,T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	I_{OP}	-	5.5	-	mA	F_{osc} = 6.0MHz @ VDD=4.5V(no load) VIN=3.0V
Audio Output Current	I_{AUD}	-	200	-	mA	VDD = 4.5V, 8 Ohms load
Input High Level	V_{IH}	0.7 VDD	-	-	V	VDD = 4.5V
Input Low Level	V_{IL}	-	-	0.3 VDD	V	VDD = 4.5V
Output Source Current	I_{OH}	-	14	-	mA	VDD = 4.5V, V_{OH} = 3.15V
Output Sink Current	I_{OL}	-	33	-	mA	VDD = 4.5V, V_{OL} = 1.35V
Input Resistor (IOC)	R_{IN}	-	95	-	KΩ	VDD = 4.5V, V_{IN} = VDD
Input Resistor (IOD)	R_{IN}	-	160	-	KΩ	VDD = 4.5V, V_{IN} = VDD

7.8. DC Characteristics (2 Cell, VDD=3.3V, TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current I(VIN)	I_{OP}	-	3.5	-	mA	F_{osc} = 6.0MHz @ VDD=3.3V(no load) VIN=3.0V
Audio Output Current	I_{AUD}	-	135	-	mA	VDD = 3.3V, 8 Ohms load
Input High Level	V_{IH}	0.7 VDD	-	-	V	VDD = 3.3V
Input Low Level	V_{IL}	-	-	0.3 VDD	V	VDD = 3.3V
Output Source Current	I_{OH}	-	8	-	mA	VDD = 3.3V, V_{OH} = 2.31V
Output Sink Current	I_{OL}	-	19	-	mA	VDD = 3.3V, V_{OL} = 0.99V
Input Resistor (IOC)	R_{IN}	-	110	-	KΩ	VDD = 3.3V, V_{IO} = VDD
Input Resistor (IOD)	R_{IN}	-	250	-	KΩ	VDD = 3.3V, V_{IO} = VDD

7.9. Pump Efficiency (1 Cell, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Pump Efficiency (L=22uH/0.5W)	Eff.	-	80	-	%	I(VDD)=30mA;VIN=1.5V; VDD=3.3V
		-	70	-	%	I(VDD)=60mA;VIN=1.5V; VDD=3.3V
		-	79	-	%	I(VDD)=30mA;VIN=1.5V; VDD=3.9V
		-	70	-	%	I(VDD)=60mA;VIN=1.5V; VDD=3.9V

*Use Color Code Inductance

7.10. Pump Efficiency (2 Cell, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Pump Efficiency (L=22uH/0.5W)	Eff.	-	87	-	%	I(VDD)=50mA;VIN=3.0V; VDD=3.9V
		-	84	-	%	I(VDD)=100mA;VIN=3.0V; VDD=3.9V
		-	86	-	%	I(VDD)=50mA;VIN=3.0V; VDD=4.5V
		-	82	-	%	I(VDD)=100mA;VIN=3.0V; VDD=4.5V

*Use Color Code Inductance

7.11. VIN v.s. Max. Supplied Current (I(VDD)) (1 Cell, TA = 25℃)

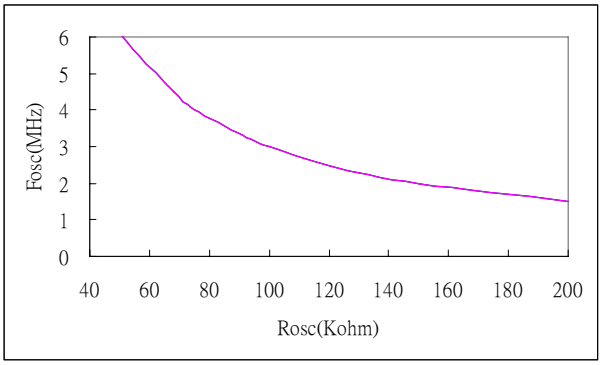
VIN (V)	I(VDD) (mA)	Condition
1.0	40	VDD=3.3V ; L=22uH/0.5W (Color Code Inductance)
	30	VDD=3.9V ; L=22uH/0.5W (Color Code Inductance)
1.2	60	VDD=3.3V ; L=22uH/0.5W (Color Code Inductance)
	50	VDD=3.9V ; L=22uH/0.5W (Color Code Inductance)
1.5	90	VDD=3.3V ; L=22uH/0.5W (Color Code Inductance)
	80	VDD=3.9V ; L=22uH/0.5W (Color Code Inductance)

7.12. VIN v.s. Max. Supplied Current (I(VDD)) (2 Cell, TA = 25℃)

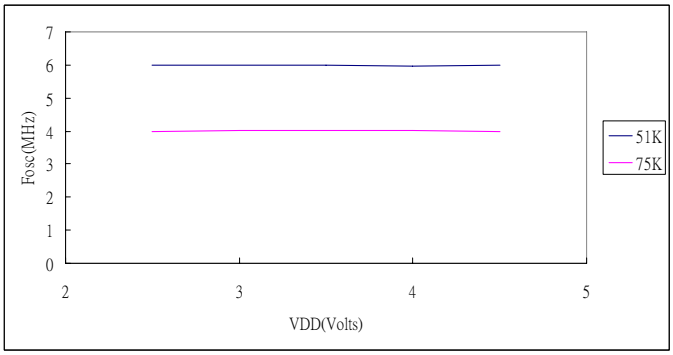
VIN (V)	I(VDD) (mA)	Condition
1.5	30	VDD=3.9V ; L=22uH/0.5W (Color Code Inductance)
	10	VDD=4.5V ; L=22uH/0.5W (Color Code Inductance)
1.8	70	VDD=3.9V ; L=22uH/0.5W (Color Code Inductance)
	50	VDD=4.5V ; L=22uH/0.5W (Color Code Inductance)
2.4	170	VDD=3.9V ; L=22uH/0.5W (Color Code Inductance)
	150	VDD=4.5V ; L=22uH/0.5W (Color Code Inductance)
3.0	200	VDD=3.9V ; L=22uH/0.5W (Color Code Inductance)
	200	VDD=4.5V ; L=22uH/0.5W (Color Code Inductance)

7.13. The Relationship between the ROSC and the FCPU

7.13.1. VDD = 3.3V, T_A = 25℃

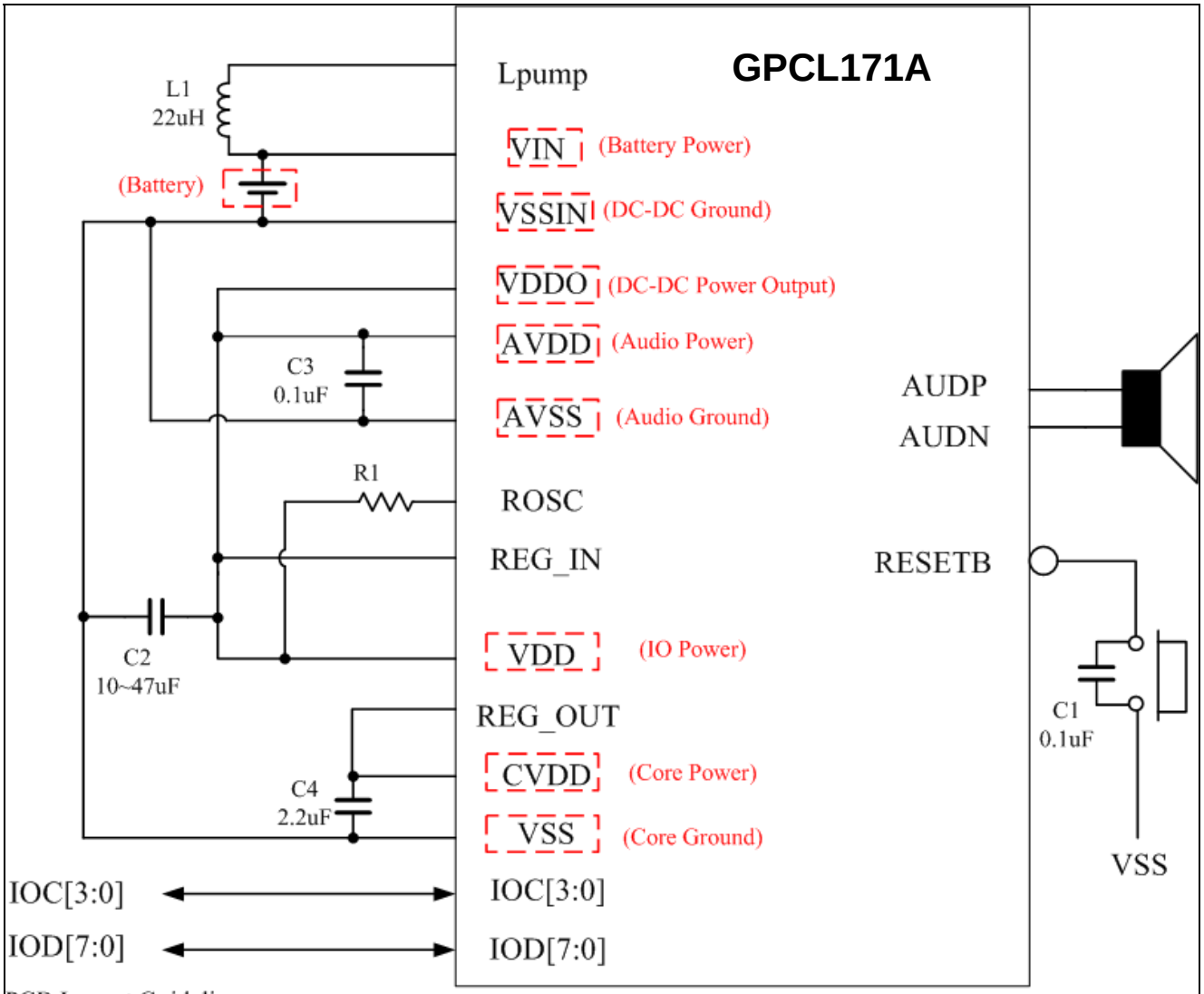


7.13.2. Frequency vs. VDD



8. APPLICATION CIRCUITS

8.1. Light Loading and Circuit without Noise



PCB Layout Guidelines :

1.R1 should be close as possible to ROSC pin.

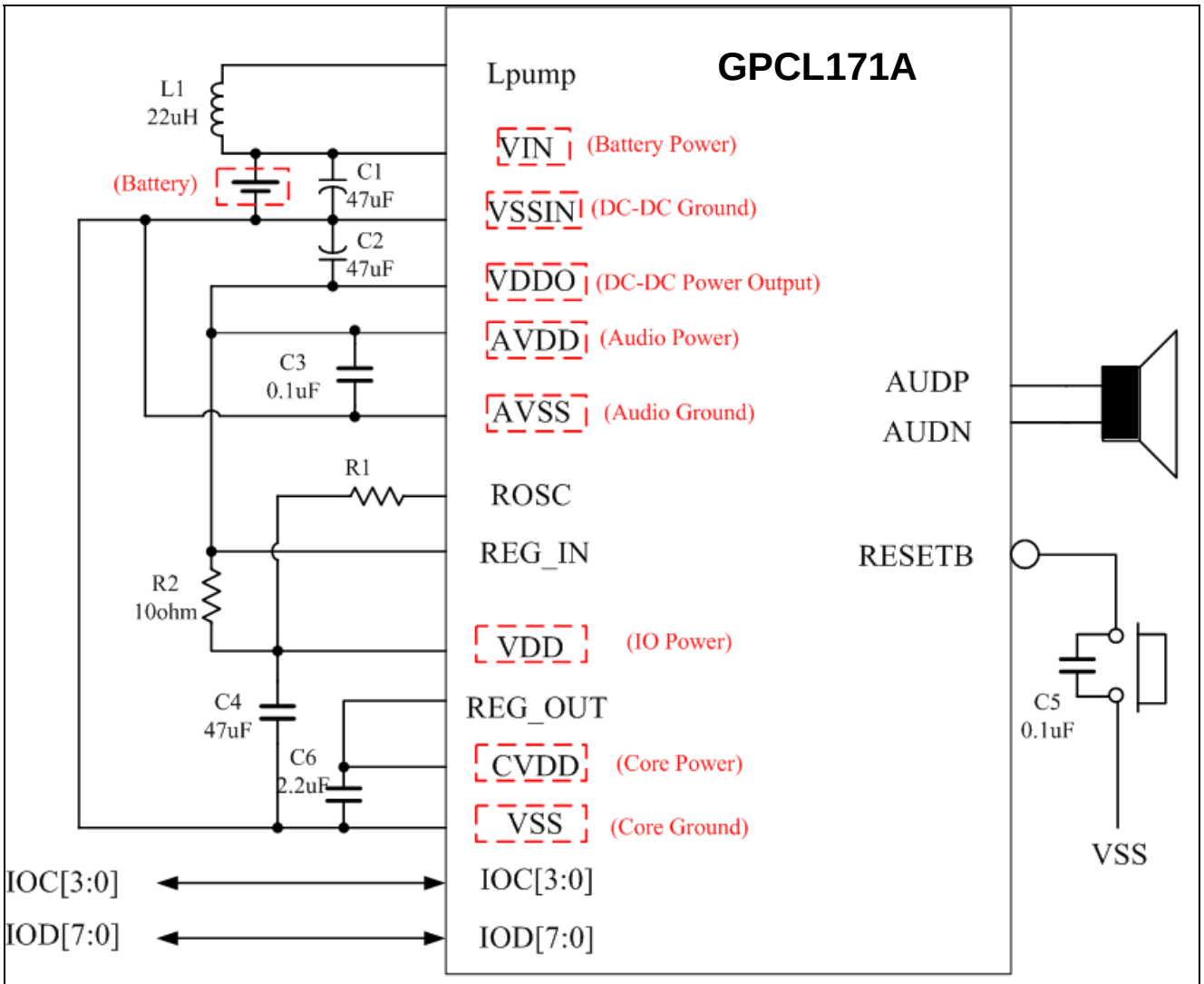
2.C3 should be as close as possible to AVDD/AVSS, and C3 can be removed if there is good power line layout on PCB that no harm to sound quality.

3.L1 should be as close as possible to VIN/Lpump. **Please use inductance with lower resistance to gain higher efficiency. 22uH/0.5W@IDC(max)>250mA ,ESR<1.5ohm is the suggested inductance spec. .**

4.The value of C2 depends on the loading. 10uF~47uF is the suggested value range. One end of C2 should be placed between VSS and VSSIN. The other end of C2 should be placed between VDDO and VDD. C2 should be as close as possible to VDDO/VDD.

5.C4 should be as close as possible to REG_OUT/CVDD pin.

8.2. Heavy Loading or Circuit with Noise



PCB Layout Guidelines :

1.R1 should be close as possible to ROSC pin.

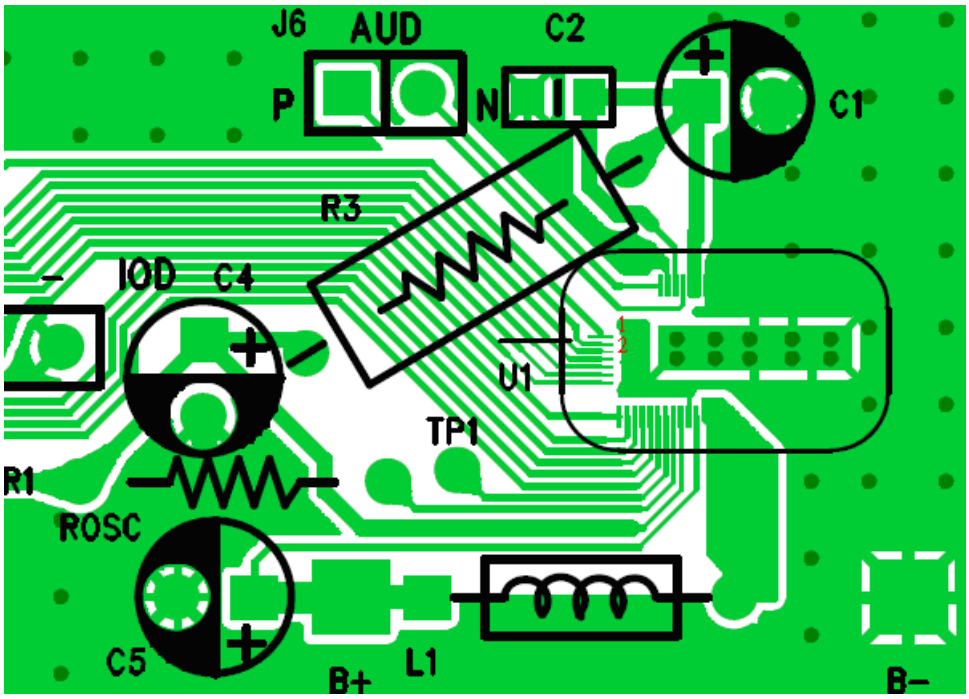
2.C3 should be as close as possible to AVDD/AVSS, and C3 can be removed if there is good power line layout on PCB that no harm to sound quality.

3.C4 should be as close as possible to VDD/VSS, and C4 can be smaller if there is good power line layout on PCB that the Power stable enough.

4.L1 should be as close as possible to VIN/Lpump. **Please use inductance with lower resistance to gain higher efficiency. 22uH/0.5W@IDC(max)>250mA ,ESR<1.5ohm is the suggested inductance spec. .**

5.C6 should be as close as possible to REG_OUT/CVDD pin.

9. PCB LAYOUT GUIDELINE



PCB Layout Guidelines:

1. The chip should be placed to where it makes VSSIN as close as possible to PCB pin out.
2. Make the width of VSSIN, VDDO and Lpump's PCB pin out as wide as possible.
3. The substrate under chip requires holes to dissipate heat and please connect substrate with VSS.
4. The route through chip, battery, and inductor should be as short as possible; its wire diameter should be as thick as possible.
5. Connect the VSS and battery's negative to a whole GND.
6. Place all chip's components as close as possible to IC, especially the capacitor to VDDO.
7. Please use inductance with lower resistance to reach higher efficiency. 22uH/0.5W@IDC(max)>250mA ,ESR<1.5ohm is the suggested inductance specification.

10. PACKAGE/PAD LOCATIONS

10.1. Ordering Information

Product Number	Package Type
GPCL171A - NnnV - C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

11. DISCLAIMER

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12. REVISION HISTORY

Date	Revision #	Description	Page
Dec.25, 2012	1.1	1.Modify User Option	6
		2.Modify Test Condition of Power Characteristics (1 Cell, TA = 25℃) Table.	7
		3.Modify Test Condition of Pump Efficiency (1 Cell, TA = 25℃) Table.	8
Nov. 07, 2012	1.0	Original	15