DATA SHEET

GPDS207A/GPDS208A

Audio Decoder with Card Reader

Preliminary

MAY 14, 2009

Version 0.1

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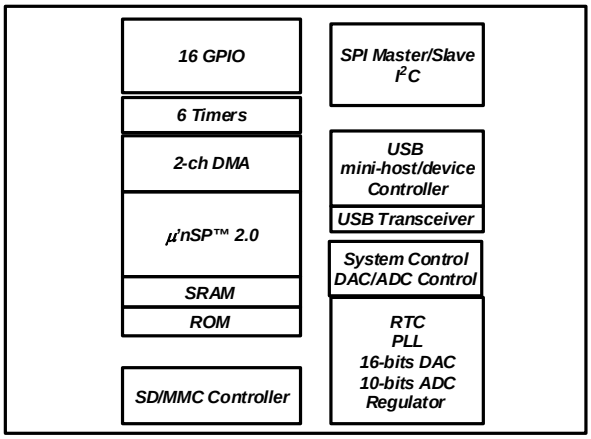
Audio Decoder with Card Reader

1. GENERAL DESCRIPTION

The GPDS207A/ GPDS208A is highly integrated system-on-a chip and targets a cost-effective, high performance micro-controller solution for car dongle MP3 application applications. It embedded *μ'nSP*® 2.0 (16-bit CPU developed by Sunplus Technology), two-channel DMA controller, six-channel 16-bit timers, SD/MMC memory interface, USB mini-host/device, SPI master/slave controller, I^2C master/slave controller, programmable I/O ports, 16-bit DAC for audio playback, 10-bit ADC for AD key, PLL, and embedded SRAM and ROM.

Providing a complete set of system peripherals, the GPDS207A/ GPDS208A chip minimizes overall system costs and eliminates the need to configure additional components. The GPDS207A/ GPDS208A features not only the high-speed performance and low cost for a system.

2. BLOCK DIAGRAM



3. FEATURES

- *μ'nSP*® 2.0 16-bit CPU with frequency up to 48MHz.
- SRAM for programming or LCD frame buffers.
- ROM for embedded algorithm.
- Two-channel DMA controller.
- Universal Serial Bus (USB) 2.0 full speed compliant device and USB mini-host with built-in transceiver.
- Watch-dog timer.
- Real-time clock.
- Six 16-bit timer.
- SD/MMC memory interface.
- SPI master/slave interface.
- I^2C Interface.
- 30 Programmable general I/O ports (GPIO) with pull-high/low control.
- Power manager.
- 3.0V to 1.8V Regulator.
- Low voltage reset.
- USB transceiver.
- High speed and low speed PLL.
- 16-bit stereo DAC for audio playback.
- 10-bit ADC with 4 line-in.

4. SIGNAL DESCRIPTIONS

Left Side

No	Name	Type	Normal Function Description	Package Pin	GPIO Group
1	DVSS	P	Digital Ground	48	-
2	RESETB	I/O	Reset input pin (Low active)	1	-
3	GPIO7	I/O	GPIO7	2	IOA7
4	GPIO12	I/O	GPIO12	3	IOA12
5	DVCC18	P	1.8V power for core logic	4	
6	INT1	I/O	External Interrupt 1	5	IOB3
7	INT2	I/O	External Interrupt 2	6	IOB4
8	SPICSN	I/O	SPI Chip Select, low active	7	IOA8
9	SPICLK	I/O	SPI Clock pins	8	IOB7
10	SPITX	I/O	SPI transmit data pin	9	IOB8
11	SPIRX	I/O	SPI receive data pin	10	IOB9
12	KEYA	I/O	Key change pin A	11	IOB10
13	DVCC33	P	3.3V IO Power	12	
14	AVDD	P	3.3V ADC Power	12	
15	LINEIN0	A/I/O	ADC Line in 0	13	IOB11
16	LINEIN1	A/I/O	ADC Line in 1	-	IOC13

Bottom Side

No	Name	Type	Normal Function Description	Package Pin	GPIO Group
17	LINEIN2	A/I/O	ADC Line in 2	-	IOC14
18	LINEIN3	A/I/O	ADC Line in 3	-	IOC15
19	AVSS	P	ADC Ground	14	
20	DVSS	P	Digital Ground	14	
21	SDDAT2	I/O	SD Data 2	15	IOA10
22	SDDAT3	I/O	SD Data 3	16	IOA11
23	SDCMD	I/O	SD Command	17	IOB0
24	SDCLK	I/O	SD Clock	18	IOB1
25	SDDAT0	I/O	SD Data 0	19	IOB2
26	SDDAT1	I/O	SD Data 1	20	IOA9
27	TEST	I/O	Test Mode Selection, high active	21	
28	DVCC18	P	1.8V power for core logic	22	
29	I2CSDA	I/O	I2C Data Pin	23	IOB5
30	I2CSCL	I/O	I2C Clock Pin	24	IOB6
31	DVCC33	P	3.3V IO Power	25	
32	BM2	I	Boot mode selection	-	
33	ICECK	I/O	ICE Clock	-	
34	ICEDA	I/O	ICE Data	-	
35	KEYB	I/O	Key Change pin B	-	IOB12
36	IOB13	I/O	IOB13	-	IOB13

Right Side

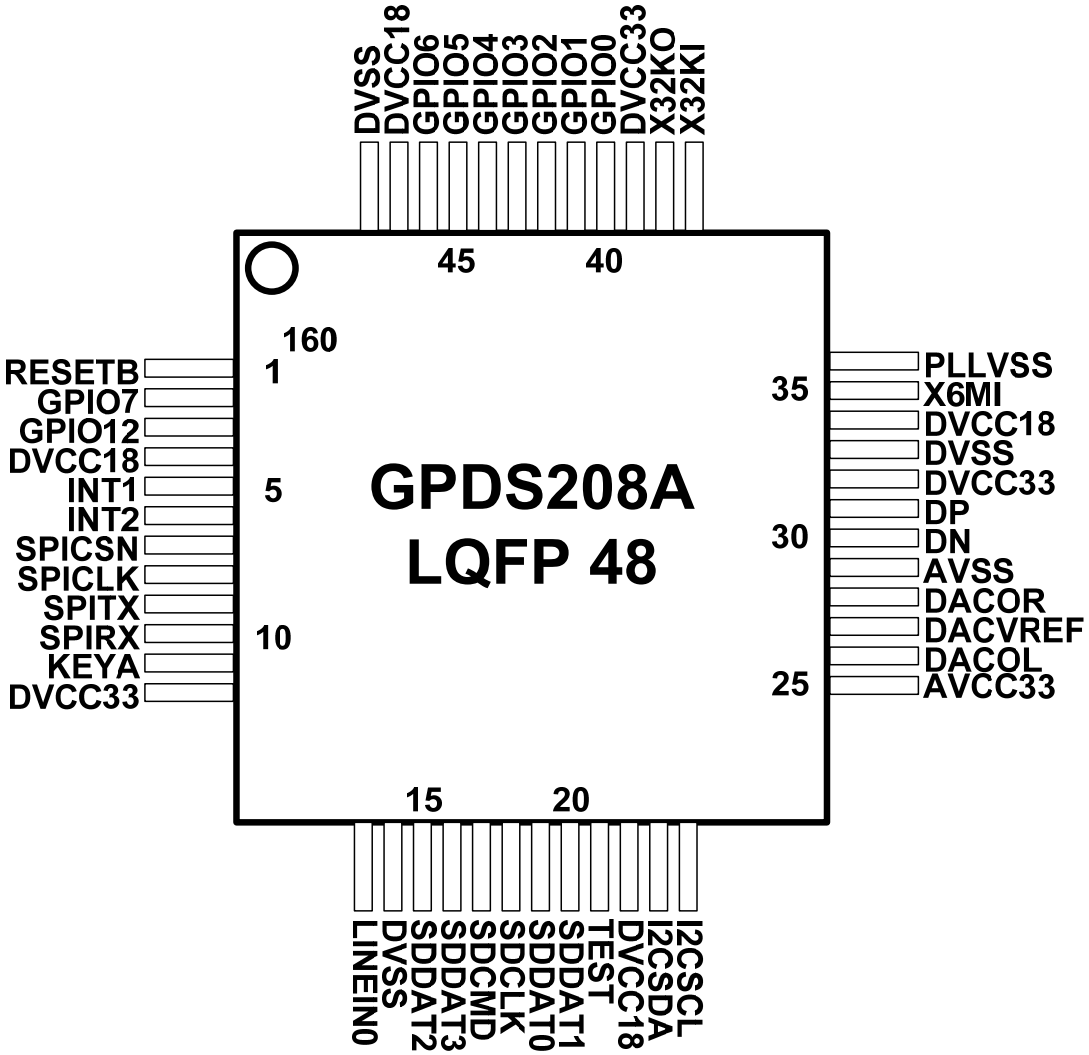
No	Name	Type	Normal Function Description	Package Pin	GPIO Group
37	AVDD	P	3.3V DAC Power	25	
38	DACOL	A	DAC Left output	26	
39	DACVREF	A	DAC VREF	27	
40	DACOR	A	DAC Right Output	28	
41	AVSS	P	DAC Ground	29	
42	AVSS	P	USB PHY Ground	29	
43	DN	I/O	DN pin of USB PHY	30	
44	DP	I/O	DP pin of USB PHY	31	
45	AVDD	P	3.3V USB PHY Power	32	
46	DVCC33	P	3.3V Regulator Power	32	
47	DVCC33	P	3.3V Regulator Power	32	
48	AVSS	P	Regulator Ground	33	
49	DVCC18	P	1.8V regulator output	34	
50	DVCC18	P	1.8V power for core logic	34	
51	PLLV18	P	1.8V power for PLL	34	
52	X6MO	O	6M Crystal output		
53	X6MI	I	6M Crystal input	35	
54	PLLVSS	P	PLL Ground	36	

Top Side

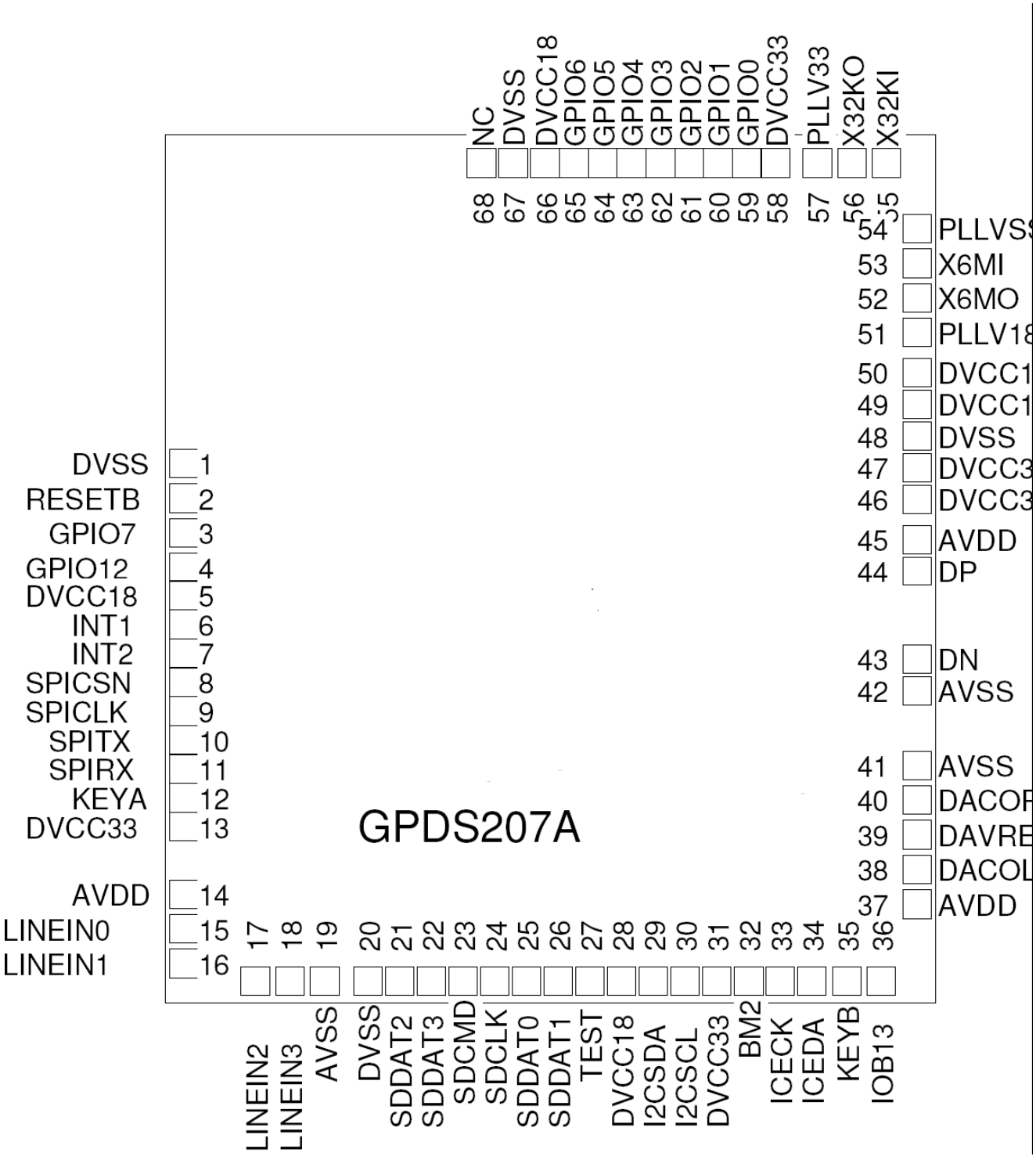
No	Name	Type	Normal Function Description	Package Pin	GPIO Group
55	X32KI	I	32768Hz Crystal Input	37	
56	X32KO	O	32768Hz Crystal Output	38	
57	PLLV33	P	3.3V power for 32768Hz crystal	39	
58	DVCC33	P	3.3V IO Power	39	
59	GPIO0	I/O	GPIO0	40	IOA0
60	GPIO1	I/O	GPIO1	41	IOA1
61	GPIO2	I/O	GPIO2	42	IOA2
62	GPIO3	I/O	GPIO3	43	IOA3
63	GPIO4	I/O	GPIO4	44	IOA4
64	GPIO5	I/O	GPIO5	45	IOA5
65	GPIO6	I/O	GPIO6	46	IOA6
66	DVCC18	P	1.8V power for core logic	47	
67	DVSS	P	Digital Ground	48	
68	NC		NC	-	

4.1. PIN Map

LQFP 48 Package Top View



4.2. PAD Locations



This IC substrate should be connected to VSS

Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

5. FUNCTIONAL DESCRIPTIONS

5.1. CPU

The GPDS207A/ GPDS208A is equipped with a 16-bit *μ'nSP*™ 2.0, the newest 16-bit microprocessor by SUNPLUS and pronounced as *micro-n-SP*. Sixteen registers are involved in *μ'nSP*™ 2.0: R1 - R4 (General-purpose registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP), SR (Segment Register) and R8 - R15 (General-purpose register). The interrupt include three FIQs (Fast Interrupt Request) and eight IRQs (Interrupt Request), plus one software-interrupt, BREAK.

5.2. PLL, Clock, Power Mode

5.2.1. PLL (Phase Lock Loop)

There are two PLLs embedded in GPLDS207A. When chip type is used, an external 6M crystal can be selected to become the clock source as the input of the fast PLL (6M=>48M). When package type is selected, the slow (32768=>6M) PLL will generate the input clock for fast PLL. The output frequency of fast PLL is programmable and ranged from 15MHz ~ 48MHz (3MHz per step).

5.2.2. System Clock

The system clock can be selected from 32768Hz or 6M or 48M (determined by fast PLL's output frequency) by register setting. Furthermore, a clock divider which can divide clock up to 1/128 is provided to reduce the power consumption.

5.3. Power Savings Mode

The GPDS207A/ GPDS208A provide 4 power modes, Normal, Wait, Halt and Sleep.

Mode	CPU	System	RTC	POWEREN	After wakeup
Normal	ON	ON	ON	ON	-
Wait	OFF	ON	ON	ON	Next Instruction
Halt	OFF	OFF	ON	OFF	Reset CPU
Sleep	OFF	OFF	OFF	OFF	Reset System

Entering the Wait/Halt/Sleep mode, is done by writing designated value to designated sport. The wake-up source can be interrupt or timer or key-change.

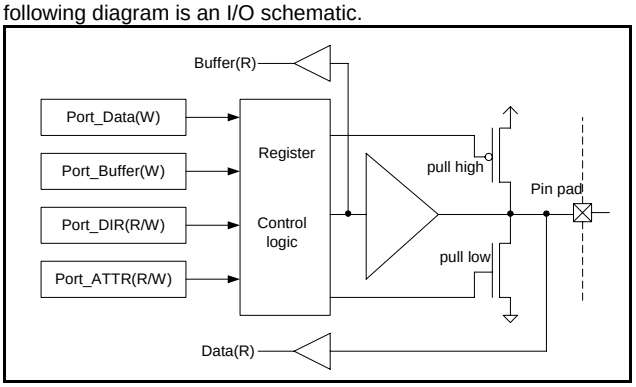
5.4. Interrupt

The GPDS207A/ GPDS208A has 20 interrupt sources, grouped into two types, FIQ (Fast Interrupt Request) and IRQ (Interrupt request). The priority of FIQ is higher than IRQ. FIQ is the high-priority interrupt while IRQ is low-priority one. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt sources. Some of the interrupt source can be programmed as FIQ or IRQ by register setting.

5.5. I/O

5.5.1. GPIO

Three I/O ports are built in GPDS207A/ GPDS208A, IOA, IOB, and IOC. Each IO has its normal function and is described in the signal description section. When the normal function of the IO is disabled, it will switch to GPIO function automatically. The following diagram is an I/O schematic.



5.6. Timer / Counter

The GPDS207A/ GPDS208A provides six 16-bit timers/counters, TimerA to TimerF. The clock source of each timer can be set individually. For Timer A to TimerD, an INT will be sent to CPU when timer overflow.

The GPL162002A is embedded with a time base controller which is used to generate the slow interrupt form 32768Hz crystal. The following table shows the available time base.

TimeBase A	TimeBase B	TimeBase C
--	8Hz	128Hz
1Hz	16Hz	256Hz
2Hz	32Hz	512Hz
4Hz	64Hz	1024Hz

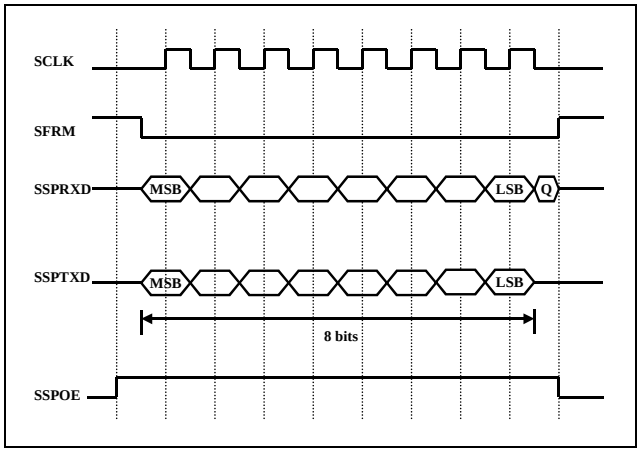
5.7. Watchdog

The purpose of watchdog is to monitor if the system operates normally. Within a certain period, watchdog must be cleared or CPU assumes the program has been running in an abnormal condition. As a result, the CPU will reset the system to the initial state and start running the program all over again. In GPDS207A/ GPDS208A, the clear period is software programmable. If watchdog is cleared before it expires, the system will not be reset.

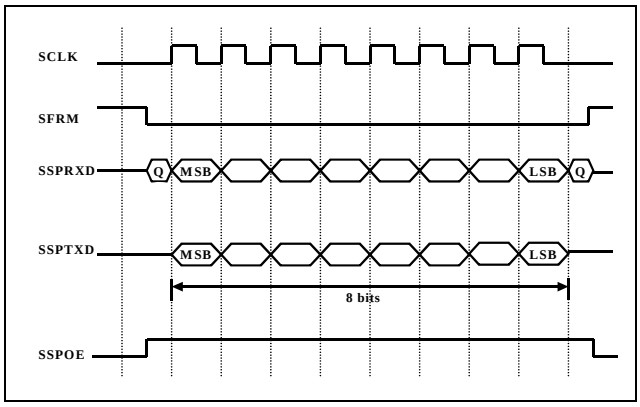
5.8. Serial Interface

5.8.1. Serial Peripheral Interface (SPI)

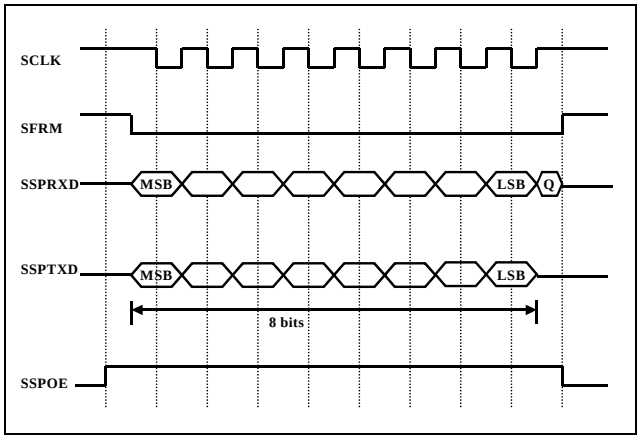
The SPI interface is a master/slave interface that enables synchronous serial communication with slave/master peripherals. Two 8-byte FIFOs are used for transmitting and receiving data. Four types of timing are supported and shown in the following diagram.



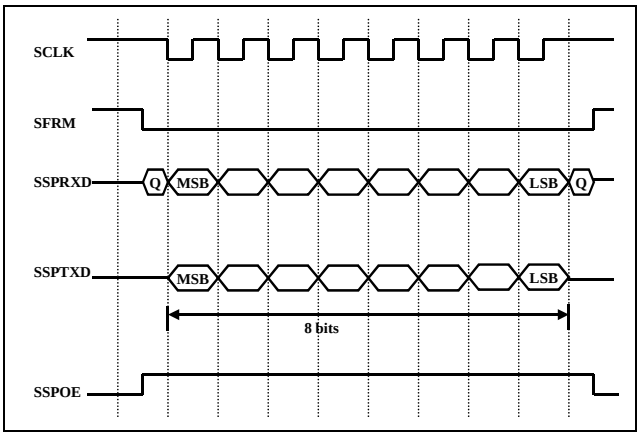
SPO = 0, SPH = 0, only this mode is supported in SPI slave mode.



SPO = 0, SPH = 1



SPO = 1, SPH = 0



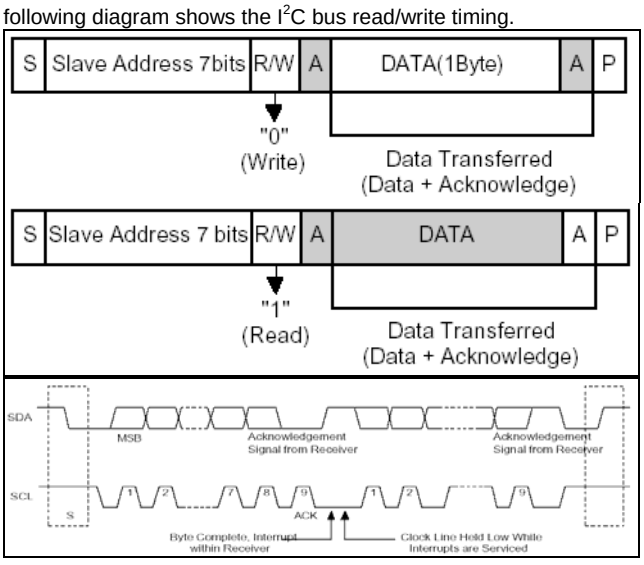
SPO = 1, SPH = 1

5.8.2. USB Mini-host/Device Function

GPDS207A/ GPDS208A provides both USB mini-host and device function which is compatible with USB 1.1 and USB 2.0 full speed standard. The mini-host and device function are not allowed to be activated concurrently. An USB transceiver is built-in for both host and devices function. A FIFO with size of 128x8 is used for bulk-in and bulk-out transfer and an 8-bytes FIFO is used for controlling pipe-transfer. Interrupt pipe is also supported. The DMA transfer is enabled for bulk-in and bulk-out to maximize the transfer performance.

5.8.3. I²C Function

GPDS207A/ GPDS208A provides an I²C controller which supports master read/write transfer, slave read/write transfer and 7-bit address mode. Multi-master mode is also supported. The following diagram shows the I²C bus read/write timing.



5.9. SD/MMC Controller

GPDS207A/ GPDS208A features a SD/MMC controller which is compatible with MMC system specification version 2.3 and SD

Memory Card specification 1.1. Both 1-bit mode and 4-bit mode are supported. The controller supports automatically CRC generation and check, 1 bit and four bits transfer, interrupt generation when buffer empty/full, DMA transfer for page read/write.

5.10. Real Time Clock (RTC)

The RTC block offers alarm function, schedule function, and hour/minute/second/half-second interrupt function.

5.11. Analog Control

5.11.1. DAC Control

A 16-bit DAC is embedded in GPDS207A/ GPDS208A. For both left and right channel, a 16x16 FIFO is used to prevent the sound glitch when CPU is busy. The left and right channel must have the same sample rate.

5.11.2. ADC Control

A 10-bit ADC is embedded in GPL162002A for AD key detection application. The ADC has four inputs which can be selected by software programming with maximum 60KkHz sample rate.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Rating

Rating	Symbol	Value	Unit
Supply Voltage 1	DVCC33 PLLV33	-0.3 to 4.0	V
Supply Voltage 2	AVDD	-0.3 to 4.0	V
Supply Voltage 3	DVCC18 PLLV18	-0.3 to 2.16	V
Input Voltage	V_{IN}	-0.3 to 4.0	V
Operating Temperature	T_A	0 to 85	℃
Storage Temperature	T_{STG}	-40 to +150	℃

6.2. DC Characteristics

Characteristic	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage 1	DVCC33 PLLV33	2.7 3.0[3]	3.0	3.6	V	-
Operating Voltage 2	AVDD	2.7	3.0	3.3	V	-
Operating Voltage 3	DVCC18 PLLV18	1.62	1.8	1.98	V	-
Operating Current	I_{OP}	-	TBD	-	mA	@48MHz, 3.3V, all clocks on
Power Down Current	I_{PD}	-	TBD	-	μA	Halt Mode
High Input Voltage	V_{IH}	0.7DVCC33	-	DVCC33	V	-
Low Input Voltage	V_{IL}	VSS	-	0.8	V	-
Crystal Frequency 1	-	-	32768	-	Hz	-
Crystal Frequency 2	$F_{CRYSTAL}$	-	6.0[1]	-	MHz	-
System Clock	F_{SYS}	256Hz[2]	48	48	MHz	-

Note1: 6M Crystal is used only when die form is selected.

Note2: By setting clock divider and changing system clock to 32768Hz mode.

Note3: When USB function is enabled, the minimum voltage of DVCC33 is 3.0V.

6.3. DAC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	-	16	-	Bit	-
Full Scale Output Voltage	-	2	-	Vp-p	-
THD+N (f = 1kHz)	-	TBD	-	%	-
Noise at No Signal	-85	90	-	dBv	-
Frequency Response	20	-	19200	Hz	-

6.4. 10 Bits ADC Characteristics (VDD = 3.3V, T_A = 25℃)

Characteristics	Symbol	Unit			Unit
		Min.	Typ.	Max.	
ADC Power Dissipation	IADC	-	1.8	-	mA
ADC Input Voltage Range	VINL (Note1)	VSS - 0.3	-	VDD + 0.3	V
Resolution of ADC	RESO	-	-	12	bits
Signal-to-Noise Plus Distortion of ADC from Line in	SINAD (Note3)	-	TBD	-	dB
Effective Number of Bit	ENOB (Note4)	8.0	9	-	bits
Integral Non-Linearity of ADC	INL	-	±1.0	-	LSB (Note2)
Differential Non-Linearity of ADC	DNL (Note5)	-	±1.0	-	LSB
AD Conversion Rate	F_{CONV}	F_{CPU} / 2048	-	F_{CPU} / 256	Hz

Note1: Internal protection diodes clamp the analog input to VDD and VSS. These diodes allow the analog input to swing from (VSS - 0.3V) to (VDD + 0.3V) without causing damage to the devices.

Note2: LSB means Least Significant Bit (at 10 bits resolution). With VINL = 2.0V, 1LSB = 2.0V / 2^10 = 1.953mV.

Note3: The SINAD testing condition at VINLp-p = 0.8 * VDD, F_{CONV} = 100KHz, Fin = 1.0KHz Sine waves at VDD = 3.0V from the ADC input.

Note4: ENOB = (SINAD - 1.76) / 6.02.

Note5: This ADC can guarantee no missing code at 10 bits resolution.

6.5. Regulator Characteristics

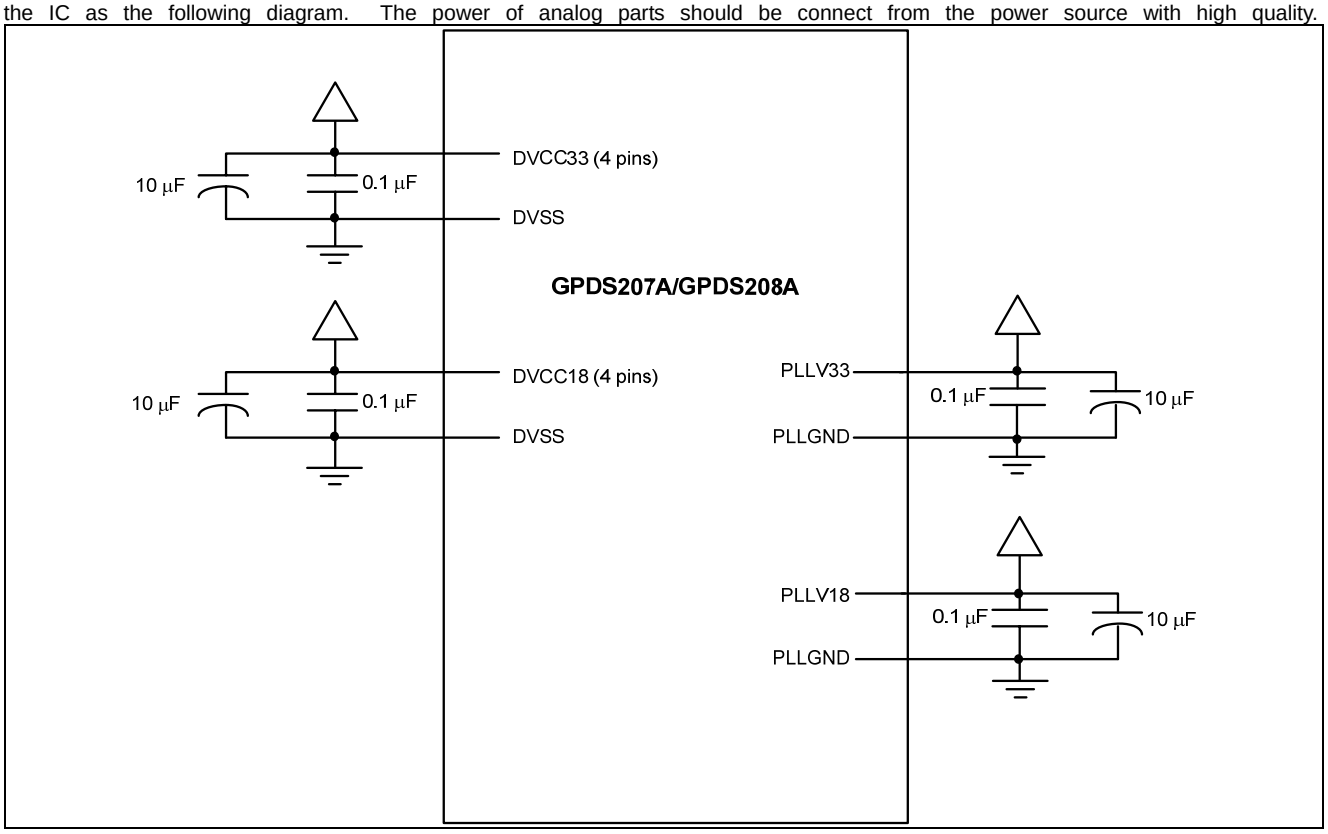
Characteristics	Symbol	Unit			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	2.7	3.0	3.6	V
Maximum Current Output	IREGO	-	50	60	mA
Output Voltage	VREGO	1.35[1]	1.8	1.89	V
Standby Current	IREGS	-	10	-	-

Note1: By software program, it is not allowed to switch the voltage below 1.35 V when system is running at full speed (>48MHz).

7. RECOMMENDED BOARD LAYOUT

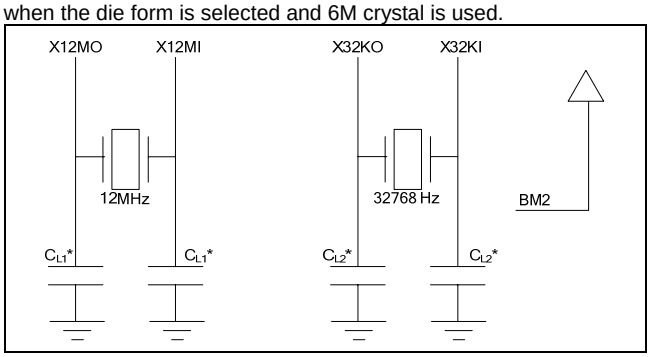
7.1. Power and Ground

All digital power and ground should be connected. The decoupling capacitor of 0.1μF and 10μF should be connected to each power pin of the IC as the following diagram. The power of analog parts should be connect from the power source with high quality.

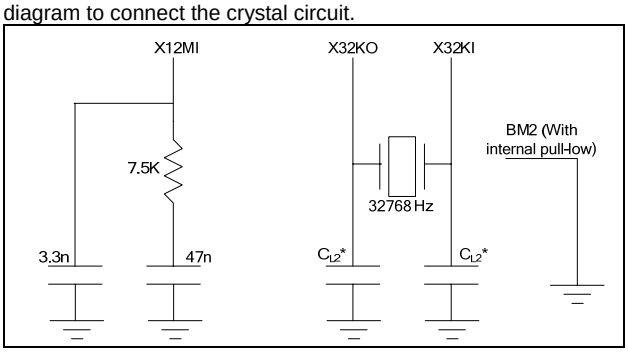


7.2. Crystal and PLL

Please refer to following diagram to connect the crystal circuit when the die form is selected and 6M crystal is used.



When the package form is selected, please refer to the following diagram to connect the crystal circuit.



Note*: Please refer to the crystal's application circuit.

8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GPDS207A - NnnV - C	Chip Form
GPDS208A - NnnV - QL15x	Halogen Free Package

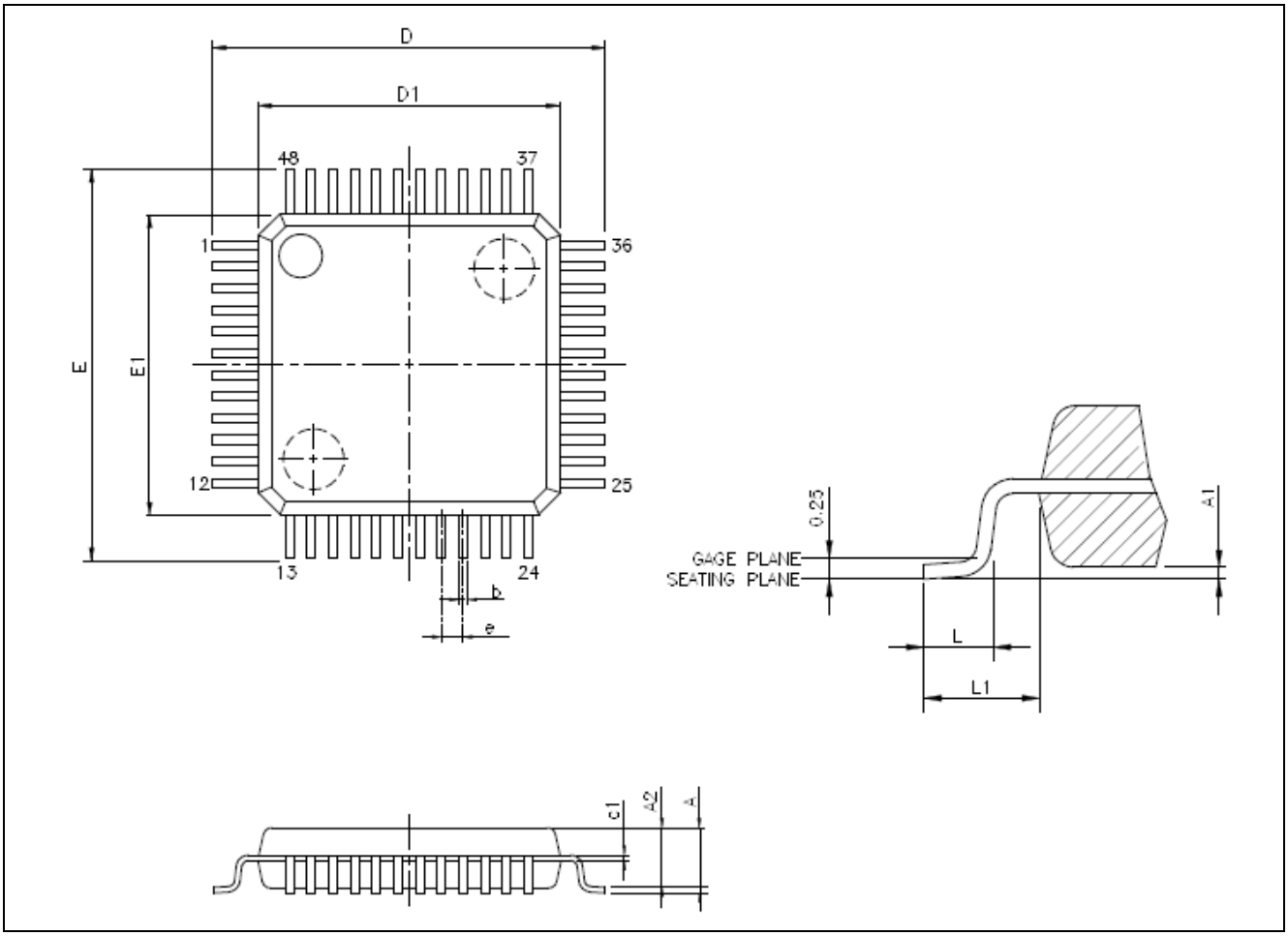
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: x = 0 - 9, serial number.

8.2. Package Information

LQFP 48



Symbol	Millimeter		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	-	1.45
c1	0.09		0.16
D	9.00 BSC.		
D1	7.00 BSC.		
E	9.00 BSC.		

Symbol	Millimeter		
	Min.	Nom.	Max.
E1		7.00 BSC.	
e		0.5 BSC.	
b	0.17	-	0.27
L	0.45	-	0.75
L1		1.00 REF	

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10. REVISION HISTORY

Date	Revision #	Description	Page
MAY 14, 2009	0.1	Preliminary version.	17