DATA SHEET

GPF16128B

16-Channel MIDI Synthesizer with 128K X 16 ROM

Nov. 01, 2011

Version 1.4

GENERALPLUS TECHNOLOGY INC. reserves the right to change this documentation without prior notice. Information provided by GENERALPLUS TECHNOLOGY INC. is believed to be accurate and reliable. However, GENERALPLUS TECHNOLOGY INC. makes no warranty for any errors which may appear in this document. Contact GENERALPLUS TECHNOLOGY INC. to obtain the latest version of device specifications before placing your order. No responsibility is assumed by GENERALPLUS TECHNOLOGY INC. for any infringement of patent or other rights of third parties which may result from its use. In addition, GENERALPLUS products are not authorized for use as critical components in life support devices/systems or aviation devices/systems, where a malfunction or failure of the product may reasonably be expected to result in significant injury to the user, without the express written approval of Generalplus.

Table of Contents

PAGE

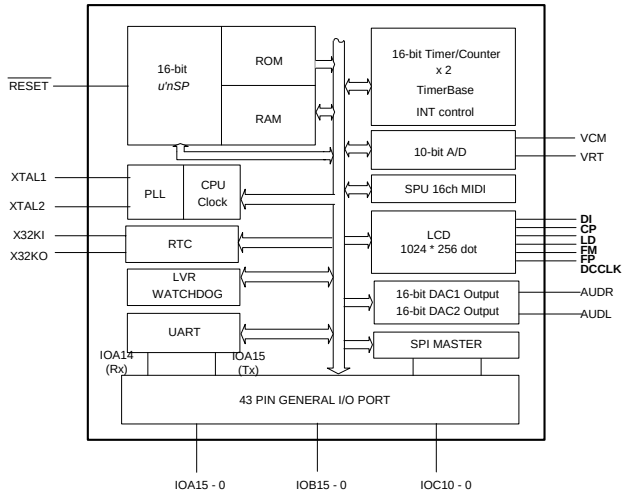
16-CHANNEL MIDI SYNTHESIZER WITH 128K X 16 ROM

1.GENERAL DESCRIPTION

GPF16, a single-chip integrating multi-processors, equips *μ'nSP*® (16-bit CPU developed by Sunplus Technology) and 16-channel Sound Processor Unit (SPU) for electronic pianos, portable Karaoke or other similar products. With the 16-bit CPU running up to 27MHz, most of the voice compression algorithms can be utilized with MIDI synthesizer applications simultaneously. In addition, it supports the interface with single color LCD panel up to 1024 x 256 dots and standard MIDI interface. Furthermore, it has up to 43 programmable I/Os and 128K-word ROM for electronic instrument applications. Its low power consumption offers the potentials to be used in battery-powered products.

The GPF16 provides not only the high-speed performance and high quality of 16 channels synthesizer, but it also integrates several powerful tools into the development system, such as development system with C language, assembly compiler, linker, source debugger functions and project management tools.

2.BLOCK DIAGRAM



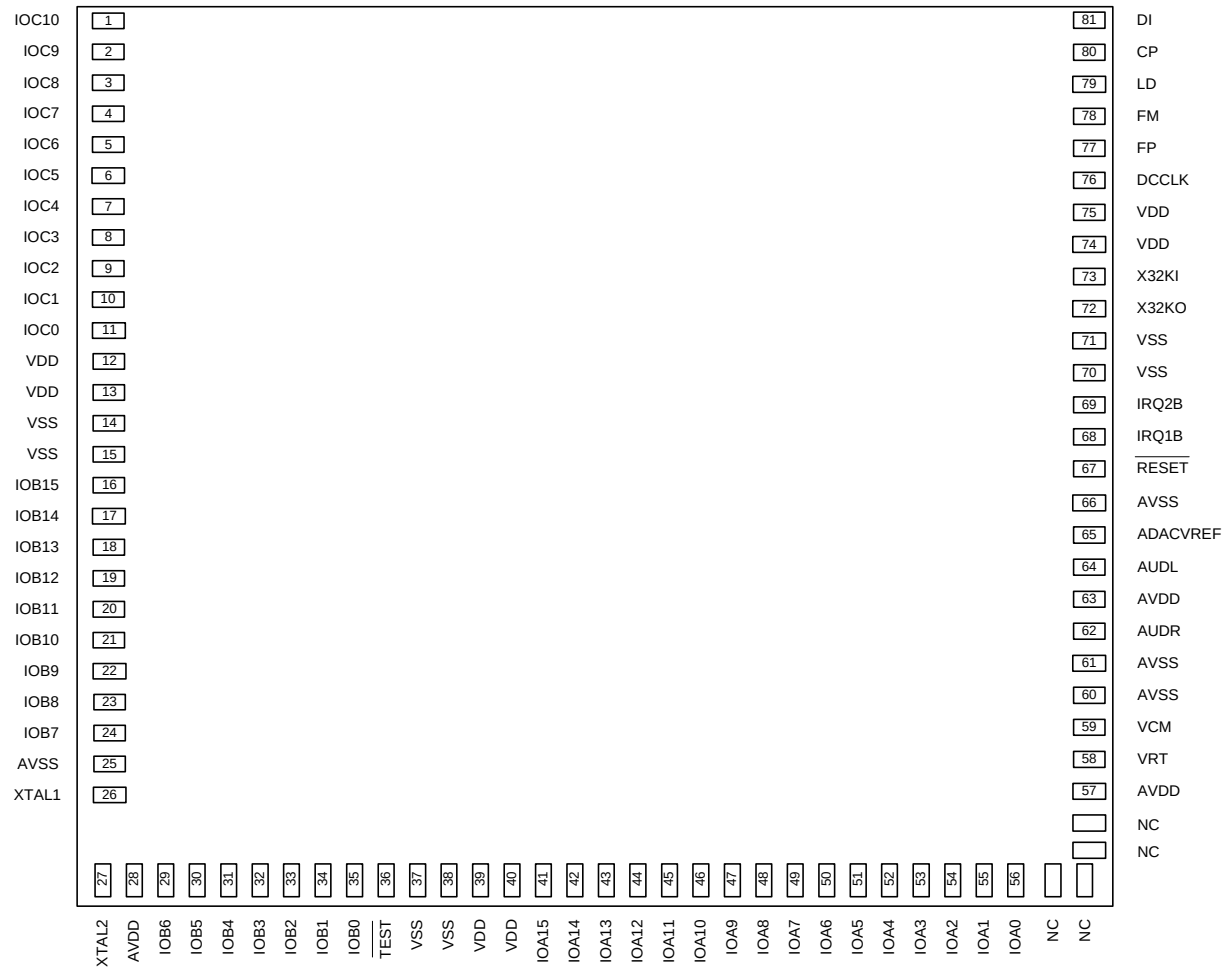
3.FEATURES

- *μ'nSP*® 16-bit CPU.
- Equips 16-channel Sound Processor Unit (SPU) for MIDI synthesis applications.
- 128K-word ROM for both programs and sound fonts. (tone colors)
- 2K-word working RAM for programming or delay buffers.
- Single color LCD interface up to 1024 x 256 dots.
- 16-bit stereo DAC.
- ADPCM sound fonts real-time decoding logic for each channel.
- 7-bit Master volume control.
- Max. 256 piece-wise slope with repetition for envelope control.
- Variable sampling rates play back for sound fonts (tone colors) wave table samples.
- Beat event IRQ and Envelope IRQ for MIDI event control.
- Channel release control logic.
- Built-in PLL to generate 27MHz internal clock with external 6MHz crystal.
- 32768Hz real time counter.
- Two 16-bit timers/counters. (Programmable and Auto Reload)
- 43 general I/Os can be programmed bit by bit.
- 14 interrupt sources: SPU, Timer, Timebase, External Input, Key wakeup, … etc.
- Key wakeup capability.
- 8 independent channels AD converters with 9-bit resolution.
- UART (MIDI) Interface.
- Built-in watchdog function.
- SPI master interface.
- LVR Function.

4.SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
VDD	12, 13, 39 40, 74, 75	P	Digital Power input.
VSS	14, 15, 37 38, 70, 71	P	Digital Ground pin.
AVDD	28, 57, 63	P	Analog power input.
AVSS	25, 60, 61, 66	P	Analog ground pin.
IRQ1B	68	I	External IRQ 1.
IRQ2B	69	I	External IRQ 2.
$\overline{\text{RESET}}$	67	I	System reset. (Low active)
IOA[15:0]	41 - 56	I/O	GPIO A, Bit 0-7 could be used as ADC input.
IOB[15:0]	16 - 24 29 - 35	I/O	GPIO B.
IOC[10:0]	1 - 11	I/O	GPIO C.
FP	77	I/O	LCD interface frame pulse, GPIO D0.
LD	79	I/O	LCD interface latch data pulse, GPIO D1.
CP	80	I/O	LCD interface clock signal, GPIO D2.
DI	81	I/O	LCD interface data signal, GPIO D3.
FM	78	I/O	LCD interface frame signal, GPIO D4.
DCCLK	76	I/O	LCD interface DC-DC clock signal, GPIO D5.
XTAL1	26	I	External crystal input, should be 6MHz.
XTAL2	27	O	External crystal output.
X32KI	73	I	External 32768Hz crystal input.
X32KO	72	O	External 32768Hz crystal output.
AUDL	64	O	Audio left channel output.
AUDR	62	O	Audio right channel output.
ADACVREF	65	I	Audio DAC reference voltage.
VCM	59	O	ADC reference voltage output.
VRT	58	I	ADC reference voltage input.
$\overline{\text{TEST}}$	36	I	Connected to GND for test mode, normally connected to VDD. (test mode disabled)

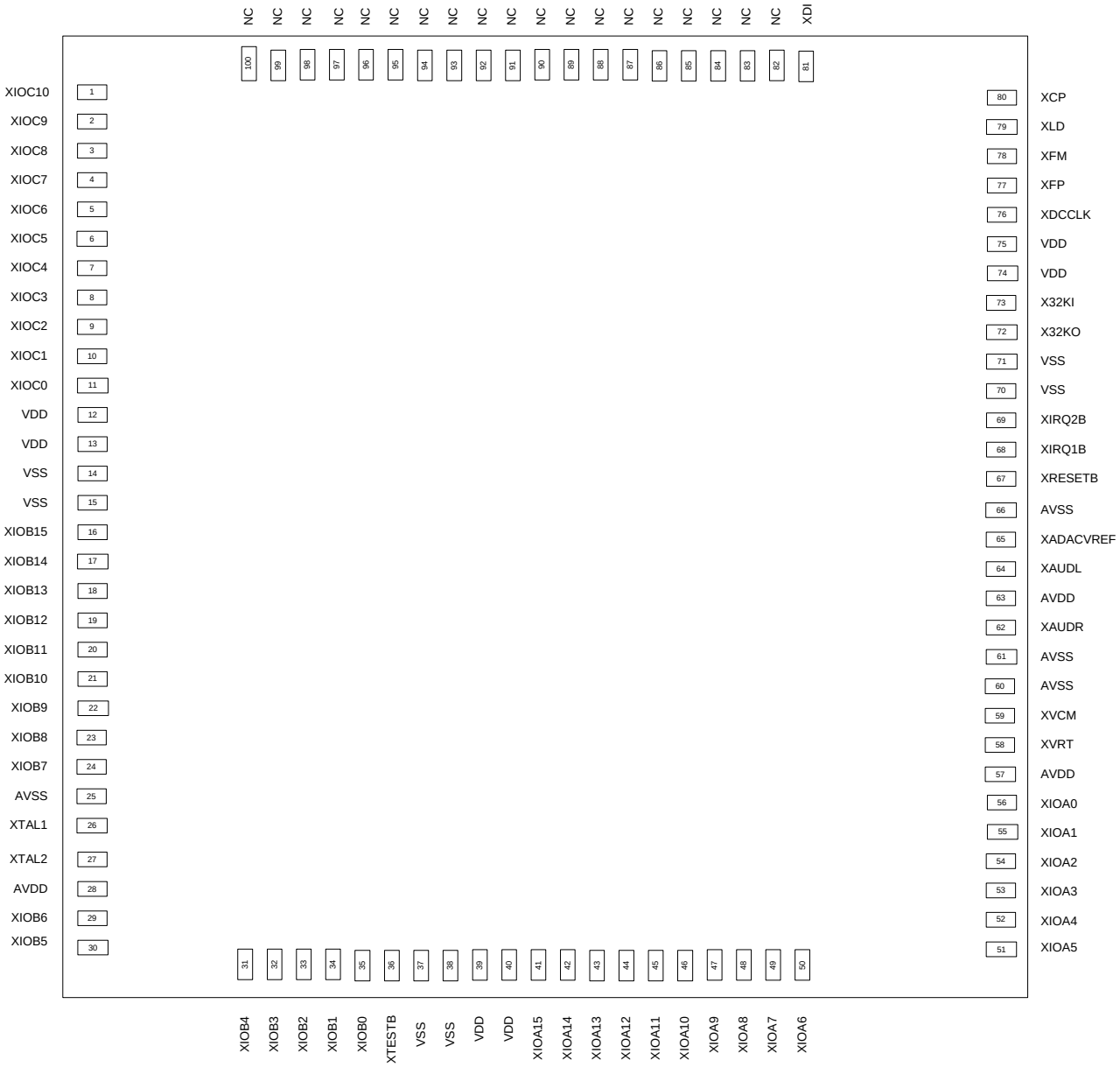
4.1. PAD Locations



This IC substrate should be connected to VSS

Note1: To ensure the IC functions properly, please bond all of VDD and VSS pins.
Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as closed as possible.

4.2. PIN Map


NC 100
NC 99
NC 98
NC 97
NC 96
NC 95
NC 94
NC 93
NC 92
NC 91
NC 90
NC 89
NC 88
NC 87
NC 86
NC 85
NC 84
NC 83
NC 82
XDI 81
XIOC10 1
XIOC9 2
XIOC8 3
XIOC7 4
XIOC6 5
XIOC5 6
XIOC4 7
XIOC3 8
XIOC2 9
XIOC1 10
XIOC0 11
VDD 12
VDD 13
VSS 14
VSS 15
XIOB15 16
XIOB14 17
XIOB13 18
XIOB12 19
XIOB11 20
XIOB10 21
XIOB9 22
XIOB8 23
XIOB7 24
AVSS 25
XTAL1 26
XTAL2 27
AVDD 28
XIOB6 29
XIOB5 30
80 XCP
79 XLD
78 XFM
77 XFP
76 XDCCLK
75 VDD
74 VDD
73 X32KI
72 X32KO
71 VSS
70 VSS
69 XIRQ2B
68 XIRQ1B
67 XRESETB
66 AVSS
65 XADACVREF
64 XAUDL
63 AVDD
62 XAUDR
61 AVSS
60 AVSS
59 XVCM
58 XVRT
57 AVDD
56 XIOA0
55 XIOA1
54 XIOA2
53 XIOA3
52 XIOA4
51 XIOA5
31 XIOB4
32 XIOB3
33 XIOB2
34 XIOB1
35 XIOB0
36 XTESTB
37 VSS
38 VSS
39 VDD
40 VDD
41 XIOA15
42 XIOA14
43 XIOA13
44 XIOA12
45 XIOA11
46 XIOA10
47 XIOA9
48 XIOA8
49 XIOA7
50 XIOA6

5.FUNCTIONAL DESCRIPTIONS

5.1. CPU

The GPF16128B is equipped with a 16-bit *μ'nSP*™, the newest 16-bit microprocessor by SUNPLUS and pronounced as *micro-n-SP*. Eight registers are involved in *μ'nSP*™*:* R1 - R4 (General-purpose registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP) and SR (Segment Register). The interrupt include three FIQs(Fast Interrupt Request) and eight IRQs(Interrupt Request), plus one software-interrupt, BREAK.

Moreover, a high performance hardware multiplier with the Capability of FIR filter is also built in to reduce the software multiplication loading.

5.2. Memory

5.2.1. SRAM

The amount of SRAM is 2K-word (including Stack), ranged from $0000 through $07FF with access speed of two CPU clock cycles.

5.2.2. ROM memory

ROM memory ($004000 ~ $023FFF) is a high-speed memory with access speed of two CPU clock cycles.

5.3. PLL, Clock, Power Mode

5.3.1. PLL (Phase Lock Loop)

The purpose of PLL is to provide a base frequency (6MHz) and to pump the frequency 27MHz for system clock (F_{OSC}).

5.3.2. System clock

Basically, the system clock is provided 27MHz by PLL and programmed by the P_WaitState_num_Ctrl (W) to determine two~ nine wait-state cycles to access ROM.

5.4. Power Savings Mode

The GPF16128B also offers a power savings mode (standby mode) for low power application needs. To enter standby mode, the desired key wakeup port (IOA [15:0], IOB [15:0], IOC [10:0]) must be configured to input first. And read the Port Latch REG to latch the GPIO state before entering the standby mode. Also remember to enable the corresponding interrupt source(s) for wakeup. After that, stop the CPU clock by writing the STOP CLOCK Register P_Sleep_Mode(W) to enter standby mode. In such mode, SRAM and I/Os remain in the previous states till CPU being awoken.

5.5. Interrupt

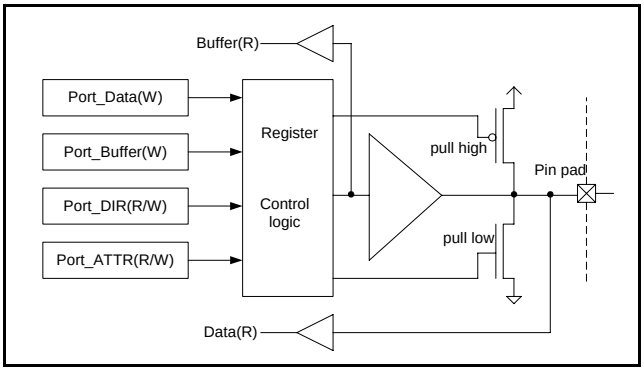
The GPF16128B has 14 interrupt sources, grouped into two types, FIQ (Fast Interrupt Request) and IRQ (Interrupt request). The priority of FIQ is higher than IRQ. FIQ is the high-priority interrupt while IRQ is the low-priority one. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt sources.

Interrupt Source	Interrupt Name	Priority
SPU Channel	FIQ / IRQ1	High(FIQ)
Timer A	FIQ_TMA/ IRQ2_TMA	High(FIQ)
Timer B	FIQ_TMB/ IRQ2_TMB	High(FIQ)
UART, SPI, ADC	IRQ3	Low
SPU Beat, Envelope	IRQ4	Low
EXT2	IRQ5_EXT2	Low
EXT1	IRQ5_EXT1	Low
4096Hz	IRQ6_4KHz	Low
2048Hz	IRQ6_2KHZ	Low
1024Hz	IRQ6_1KHz	Low
4Hz	IRQ7_4Hz	Low
Time-base 1	IRQ7_TMB1	Low
Time-base 2	IRQ7_TMB2	Low
Key change wakeup	IRQ7_KEY	Low

5.6. I/O

Three I/O ports are built in GPF16128B, PortA, PortB and PortC. The PortA, B, C is an ordinary I/O with programmable wakeup capability. In addition to the regular IO function, the PortB can also perform some special functions in certain pins.

The following diagram is an I/O schematic.



Although data can be written into the same register through Port_Data and Port_Buffer, they can be read from different places, Buffer (R) and Data (R). The GPIO is the key wakeup port. To activate key wakeup function, latch data on PORT Latch and enable the key wakeup function. Wakeup is triggered when the GPIO state is different from at the time latched. In addition to an ordinary I/O port, PortB carries some special functions. A summary of PortB special functions is listed as follows:

Special function in PortB

PortB	Special Function	Function Description	Note
IOB2	TMB2	Timebase output 2	Output
IOB3	TMB1	Timebase output 1	Output
IOB4	TBPWM	TimeB, Pulse Width Modulation	Output
IOB5	TAPWM	TimeA, Pulse Width Modulation	Output
IOB6	Ext1	External clock source of timer	Input
IOB7	Ext2	Extternal clock source of timer	Input

Default state: Pull Low

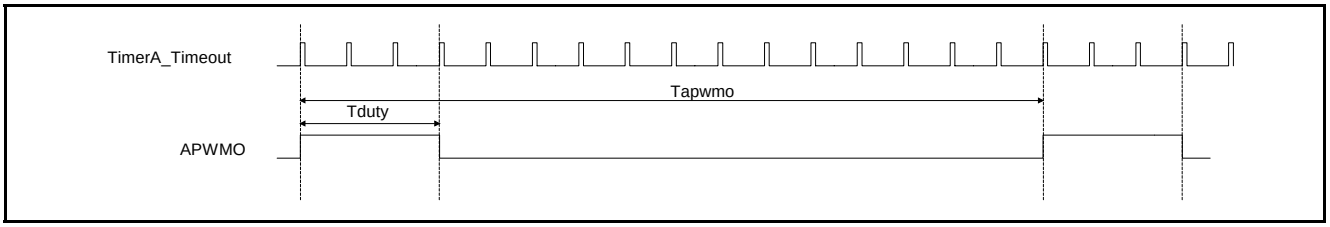
5.7. Timer / Counter

The GPF16128B provides two 16-bit timers/counters, TimerA and TimerB. The TimerA is called a universal counter. TimerB is a general-purpose counter. The clock source of TimerA comes from the combination of clock source A and clock source B. In TimerB, the clock source is given from source C. When timer overflows, an INT signal is sent to CPU to generate a time-out signal.

Clock of Source A	Clock of Source B	Clock of Source C
Fosc/2	2048Hz	Fosc/2
Fosc/256	1024Hz	Fosc/256
32768Hz	256Hz	32768Hz
8192Hz	TMB1	8192Hz
4096Hz	4Hz	4096Hz
1	2Hz	1
0	1	0
EXT1	EXT2	EXT1

Initially, write a value of N into a timer and select a desired clock source, timer will start counting from N, N+1, N+2, ... through FFFF. An INT (TimerA/TimerB) signal is generated at the next clock after reaching “FFFF” and the INT signal is transmitted to INT controller for further processing. At the same time, N will be reloaded into timer and start all over again. The clock source A is a high frequency source and clock source B is a low frequency source. The combination of clock source A and B provides a variety of speeds to TimerA. A “1” represents pass signal and not gating. In contrast, “0” indicates deactivating timer. The EXT1 and EXT2 are the external clock sources. Moreover, counter can generate time-out signal for input clock source to a four bits (16 levels) PWM pulse width counter. A variety of clock duration can be generated and exported from IOB5 (APWMO) and IOB4 (BPWMO).

The following example is a 3/16-duration cycle. The APWMO waveform is made by selecting a pulse width through Port_TimerA_Ctrl (W) [9:6]. As a result, each 16 cycles will generate a pulse width defined in control port. These PWM signals can be applied for controlling the speed of motor or other devices.



Generally speaking, the clock source A and C are fast clock sources and source B comes from RTC system (32768Hz). Therefore, clock source B can be utilized as a precise counter for time counting, e.g., the 4Hz clock can be used for real time counting.

5.7.1. Timebase

Timebase, generated by 32768Hz, is a combination of frequency selections. The outputs of timebase block are named to TMB1 and TMB2. TMB1 is frequency for TimerA (Clock source B). The TMB1 and TMB2 are the sources for Interrupt (IRQ7). Furthermore, timebases generates additional 4Hz to 4096Hz interrupt sources (IRQ6 and IRQ7) for Real-Time-Clock (RTC).

TMB2	TMB1
128Hz	8Hz
256Hz	16Hz
512Hz	32Hz
1024Hz	64Hz
Default: 128Hz	Default: 8Hz

5.8. Sleep, Wakeup and Watchdog

5.8.1. Wakeup and sleep

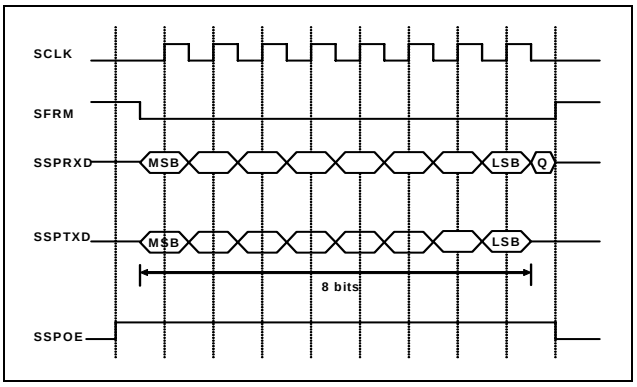
1) Sleep: After power-on reset, IC starts running until a sleep command occurs. When a sleep command is accepted, IC will turn the system clock (PLL) off. After all, it enters sleep mode.
2) Wakeup: CPU waking up from sleep mode requires a wakeup signal to turn the system clock (PLL) on. The IRQ signal makes CPU to complete the wakeup process and initialization.

5.8.2. Watchdog

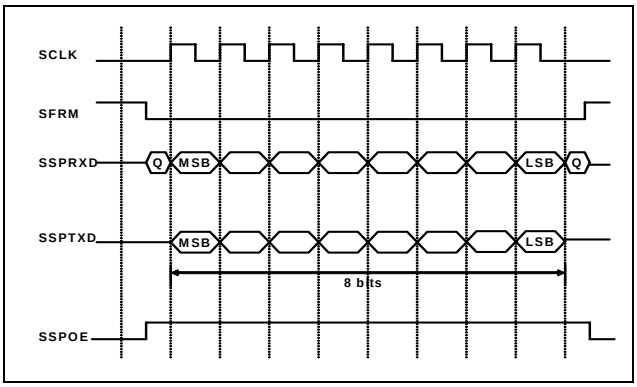
The purpose of watchdog is to monitor if the system operates normally. Within a certain period, watchdog must be cleared. If watchdog is not cleared, CPU assumes the program has been running in an abnormal condition. As a result, the CPU will reset the system to the initial state and start running the program all over again. In GPF16128B, the clear period is 0.75 seconds. If watchdog is cleared within each 0.75 seconds, the system will not be reset. The watchdog function remains enabled during standby mode if the 32768Hz.

5.9. Serial Peripheral Interface (SPI)

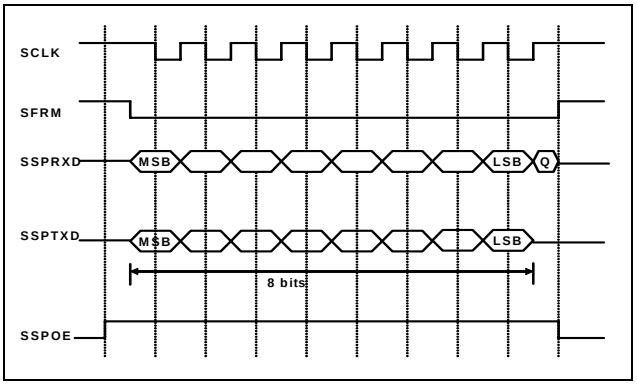
The SPI interface is a master-only interface that enables synchronous serial communication with slave peripherals.



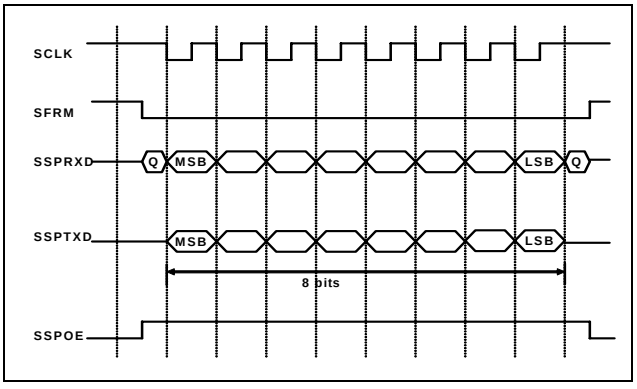
Single transfer Data Change at Falling, Latch at Rising.



Continuous transfer



Single transfer Data Change at Rising, Latch at Falling



Continuous transfer

5.10. IDE Tools Function

The functions of IDE include the follows:

1). C compiler, Assembly, and Linker.

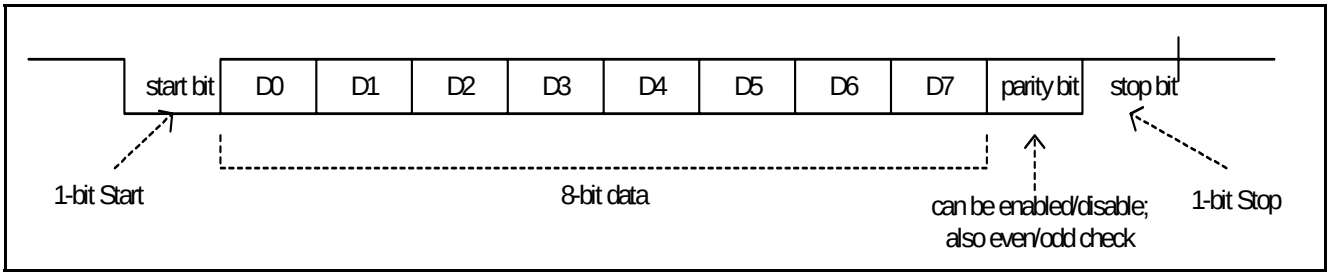
2). Single step trace

3). Break point (break point for debugging)

4). Run (execute)

5.11. UART Function

UART block provides a full-duplex standard interface that facilitates the communication with other devices. With this interface, GPF16128B can transmit and receive simultaneously. The maximum baud-rate can be up to 57600bps. The Rx and Tx of UART are shared with IOA14 and IOA15.



6.ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Rating

Rating	Symbol	Value	Unit
Supply Voltage	VDD	0 to 3.6	V
Input Voltage	V_{IN}	-0.3 to VDD + 0.3	V
Operating Temperature	T_A	0 to 85	℃
Storage Temperature	T_{STG}	-55 to + 125	℃

6.2. DC Characteristics

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	3.3	3.6	V	-
Operating Current	I_{OP}	22	32	37	mA	F_{OSC} = 27MHz, AD, DAC disable, no loading
Standby Current	I_{STB}	-	-	13.5	μA	Enable 32Khz, Disable PLL (F_{OSC})
Input High Level	V_{IH}	0.7VDD	-	-	V	VDD = 3.3V
Input Low Level	V_{IL}	-	-	0.3VDD	V	VDD = 3.3V
Output High Current	I_{OH}	6.0	10	12	mA	V_{OH} = 2.6V
Output Low Current	I_{OL}	8.0	10	11	mA	V_{OL} = 0.7V
Input Pull-Low Resister	R_{PL}	99	68	62	KΩ	V_{IN} = VDD
Input Pull-High Resister	R_{PH}	90	58	53	KΩ	V_{IN} = VSS

6.3. DAC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	-	16	-	Bit	-
Full Scale Output Voltage	-	2.0	-	Vp-p	-
THD+N (f = 1kHz)	-	-	0.01	%	-
SNR	-	90	-	dBv	-
Frequency Response (f = 50Hz to 20 kHz)	-6.0	-	0.1	dB	-
Driving Strength	10	-	-	KΩ	-

6.4. ADC Characteristics (VDD = 3.3V, T_A = 25℃)

Characteristics	Symbol	Unit			Unit
		Min.	Typ.	Max.	
ADC Power Dissipation	IADC	-	1.8	-	mA
ADC Input Voltage Range	VINL (Note 1)	VSS - 0.3	-	VDD + 0.3	V
Resolution of ADC	RESO	-	-	10	bits
Signal-to-noise Plus Distortion of ADC from Line in	SINAD (Note 3)	-	56	-	dB
Effective Number of Bit	ENOB (Note 4)	8.0	9.0	-	bits
Integral Non-Linearity of ADC	INL	-	±4.0	-	LSB (Note 2)
Differential Non-Linearity of ADC	DNL (Note 5)	-	±0.5	-	LSB
AD Conversion Rate	F_{CONV}	F_{CPU} / 2048	-	F_{CPU} / 256	Hz

Note1: Internal protection diodes clamp the analog input to VDD and VSS. These diodes allow the analog input to swing from (VSS - 0.3V) to (VDD + 0.3V) without causing damage to the devices.

Note2: LSB means Least Significant Bit. With VINL = 2.0V, 1LSB = 2.0V / 2^10 = 1.953mV.

Note3: The SINAD testing condition at VINLp-p = 0.8 * VDD, F_{CONV} = F_{CPU} / 512 = 27MHz / 256 = 105KHz, Fin = 1.0KHz Sine waves at VDD = 3.0V from the ADC input.

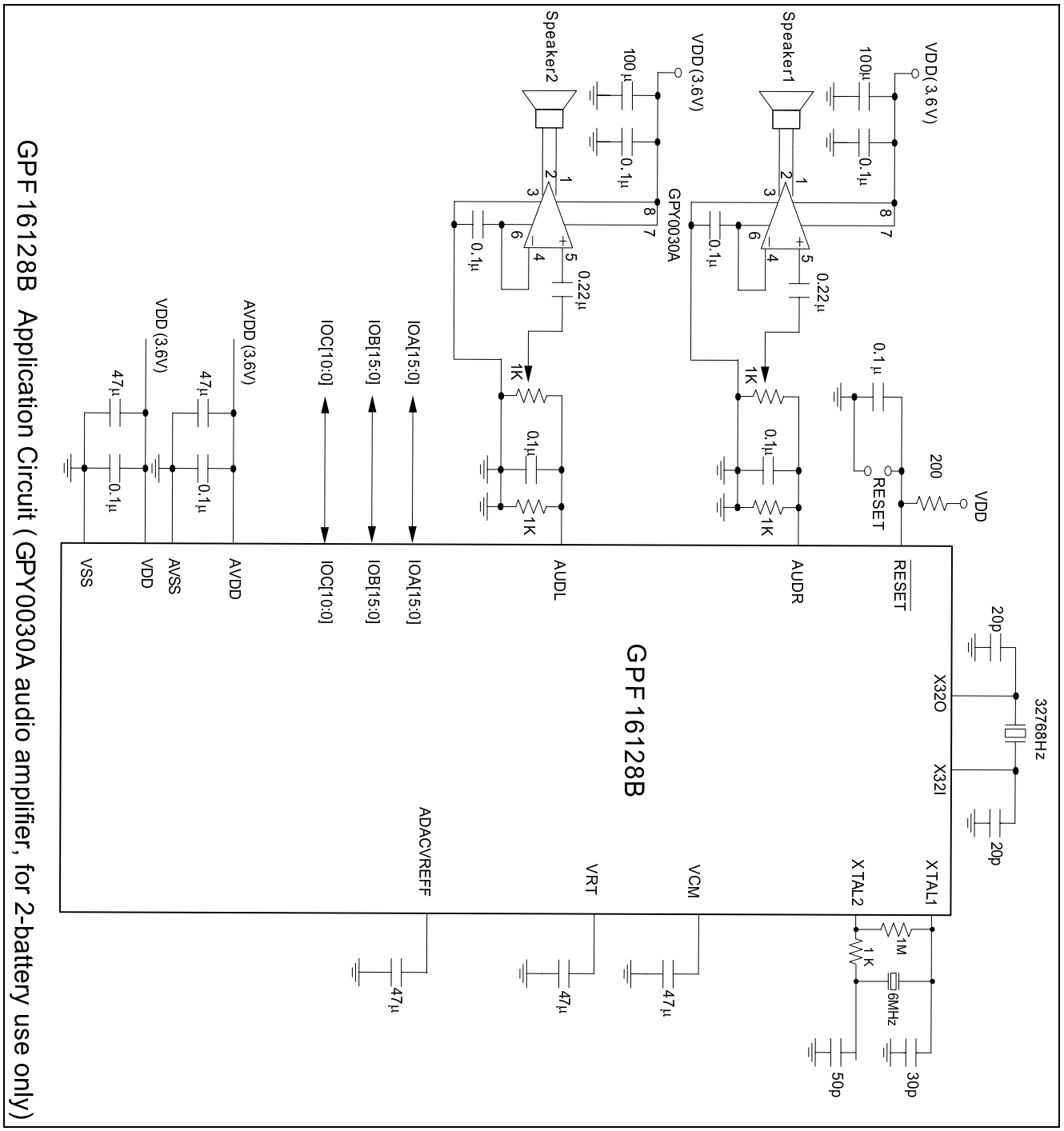
Note4: ENOB = (SINAD - 1.76) / 6.02.

Note5: This ADC can guarantee no missing code.

6.5. LVR Characteristics (VDD = 3.3V, T_A = 25℃)

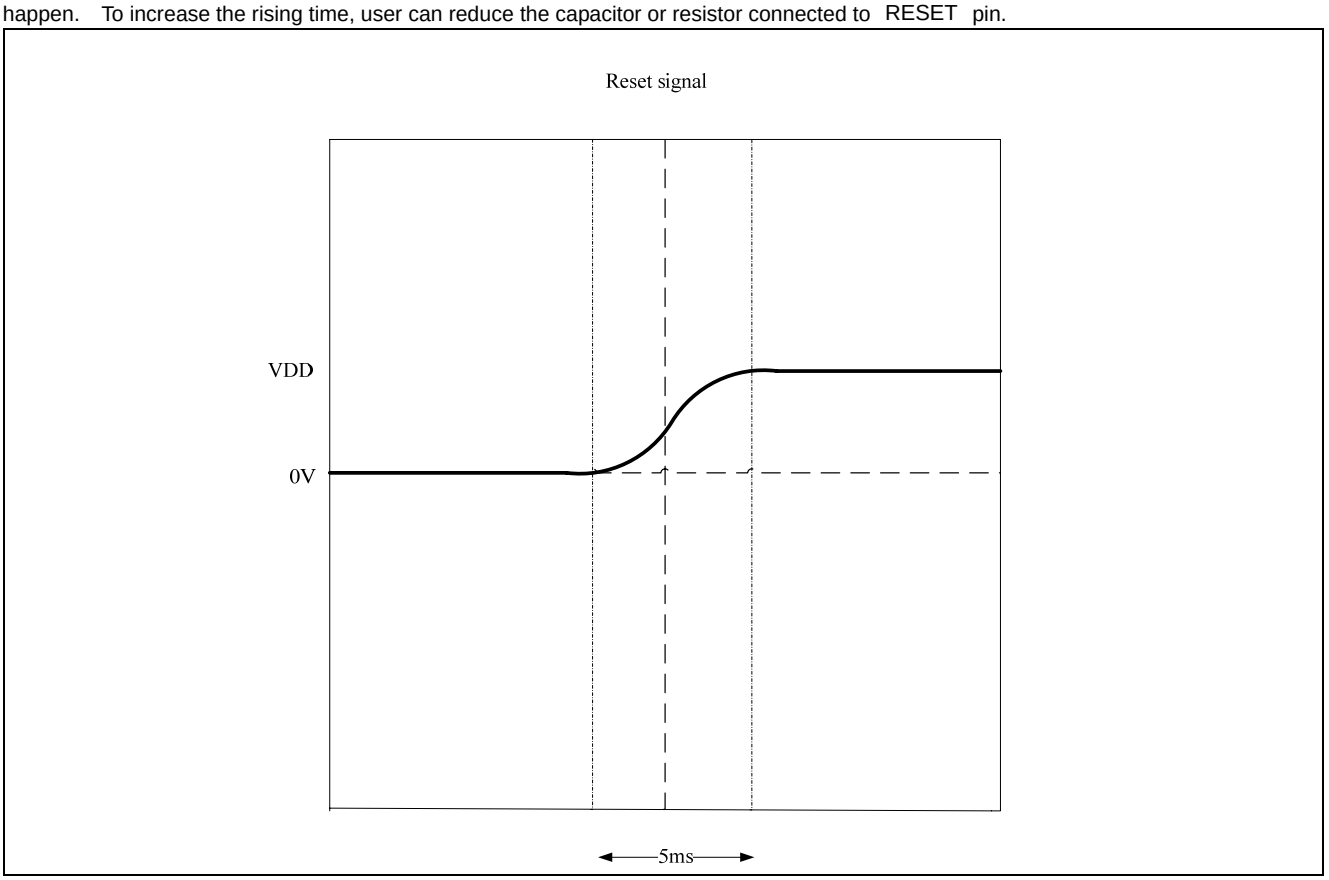
Name	Characteristics	Item	Unit	Min.	Typ.	Max.	Condition
LVR	Threshold Voltage	V_{LVR}	V	2.0	2.2	2.4	-

7.APPLICATION CIRCUIT

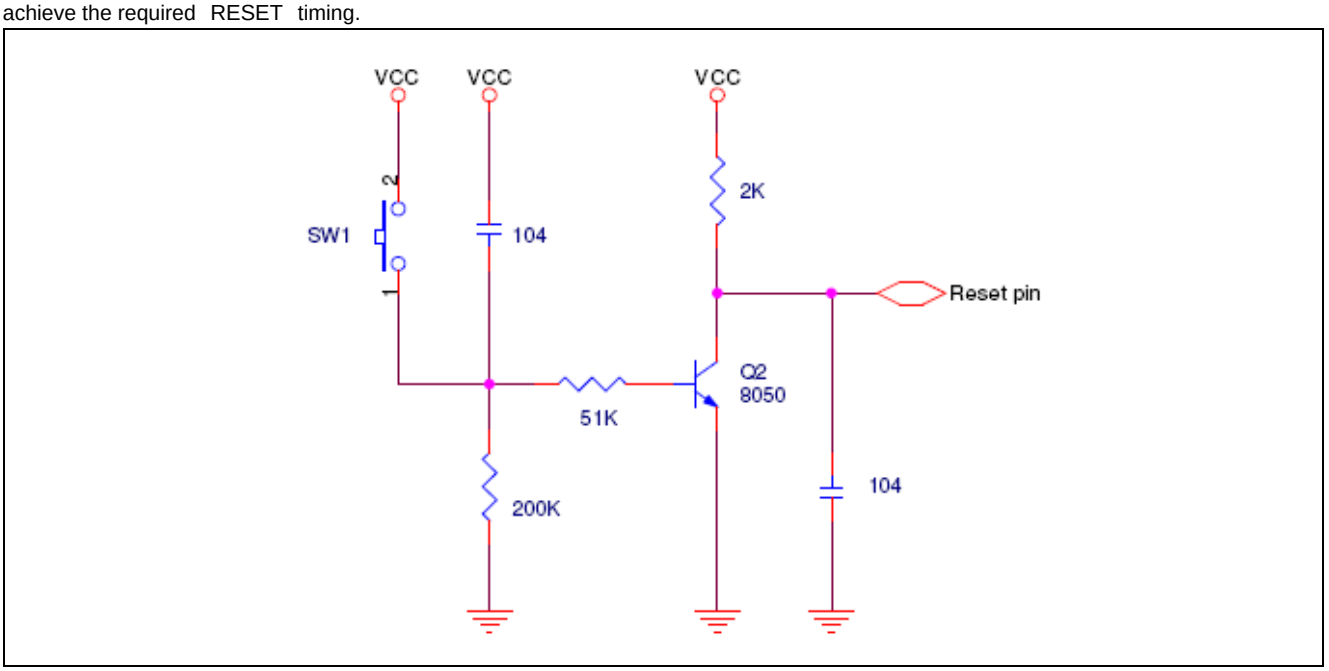


8. RESET SIGNAL

Care must be taken on the $\overline{\text{RESET}}$ signal. The $\overline{\text{RESET}}$ signal's rising time must be less than 5 ms, otherwise the system crash may happen. To increase the rising time, user can reduce the capacitor or resistor connected to $\overline{\text{RESET}}$ pin.



If the $\overline{\text{RESET}}$ signal is not able to achieve the above timing diagram, we suggest add the supper reset circuit in the following diagram to achieve the required $\overline{\text{RESET}}$ timing.



The resister and capacitor value is depend on the switch type, please contact Generalplus FAE for detailed.

9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

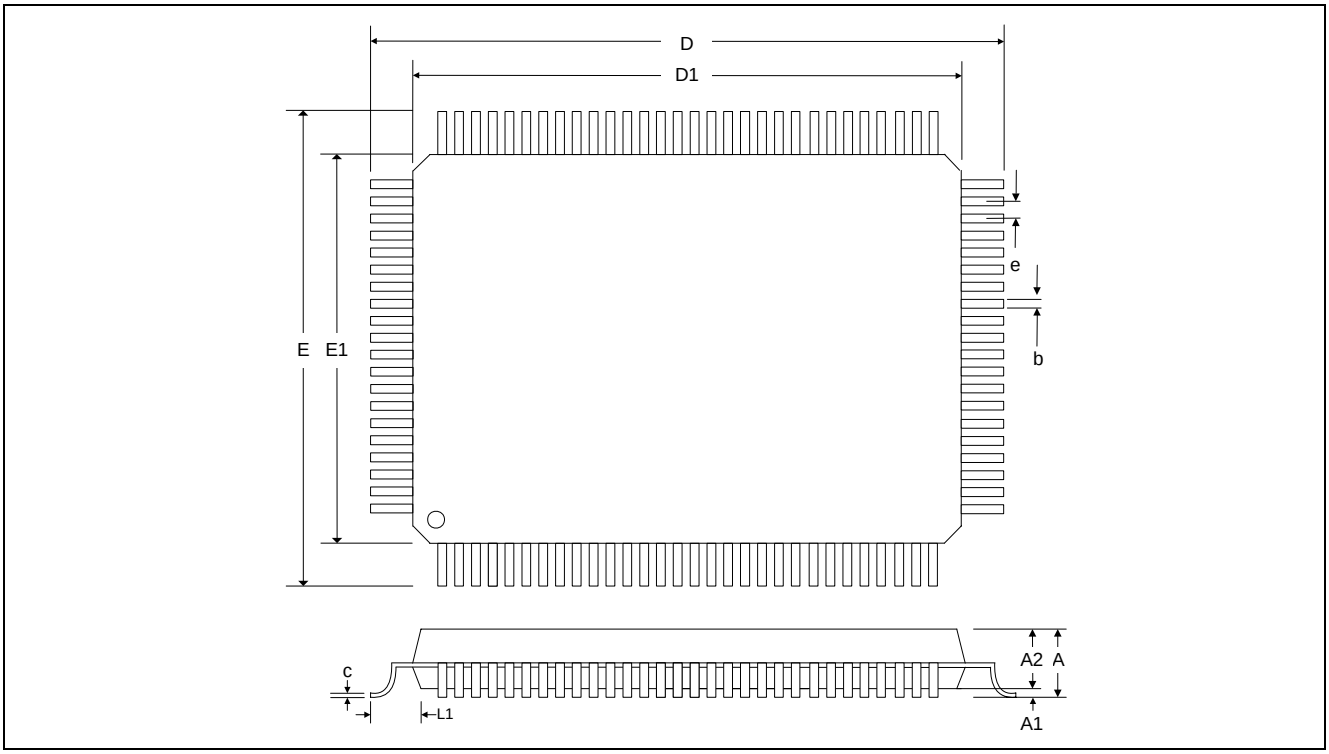
Product Number	Package Type
GPF16128B-NnnV-C	Chip form
GPF16128B-NnnV-HQ06x	Green Package form - QFP 100

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 0 - 9, serial number).

9.2. Package Information



Symbol	Dimension in inch		
	Min.	Typ.	Max.
A	-	-	0.134
A1	0.010	-	-
A2	0.098	0.107	0.114
b	0.009	0.012	0.015
c	0.004	0.006	0.009
D	0.913 BSC.		
D1	0.787 BSC.		
E	0.677 BSC.		
E1	0.551 BSC.		
e	0.026 BSC.		
L1	0.063 BSC.		

10. DISCLAIMER

The information appearing in this publication is believed to be accurate.

Integrated circuits sold by Generalplus Technology are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. GENERALPLUS makes no warranty, express, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHERMORE, GENERALPLUS MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. GENERALPLUS reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by GENERALPLUS for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

11. REVISION HISTORY

Date	Revision #	Description	Page
NOV. 01, 2011	1.4	Modify section 4.1 Pad Assignment.	5
MAY 16, 2011	1.3	Modify section 7. APPLICATION CIRCUIT.	13
MAY 10, 2007	1.2	Add super reset application circuit in section 8.	13
NOV. 30, 2006	1.1	1. Add “RESET SIGNAL” in section 8. 2. Modify the “Ordering Information” in section 9.2.	13 14
JAN. 17, 2006	1.0	Original Note: The GPF16128B data sheet v1.0 is a continued version of SPF16128B data sheet v0.3.	16