DATA SHEET

GPFA64D1

64K Music Synthesizer

Oct. 21, 2015

Version 1.1

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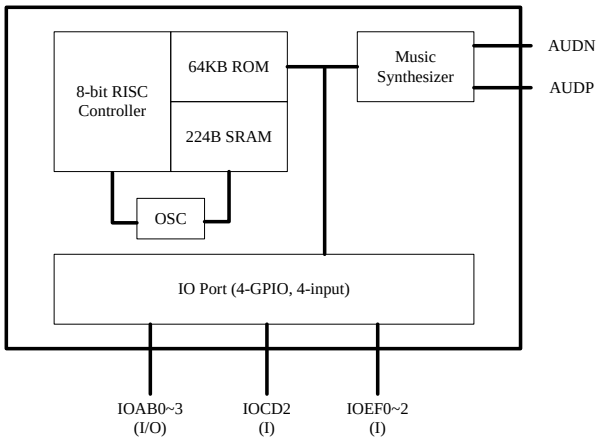
64K MUSIC SYNTHESIZER

1. GENERAL DESCRIPTION

The GPFA64D1, a fully CMOS integrated circuit, adopts advanced design and process technology to combine an 8-bit RISC processor, an 8-channel music synthesizer, 64K bytes program ROM, 224 bytes working SRAM, timer/counter and I/Os interface in a single chip. The sound processing logic is a unique design to achieve high quality melody effect. It can simulate all types of musical instruments by programming the tone ROM and controlling the envelope slope of each channel. Every channel can also be defined as a speech channel to provide percussion, animal sounds, gun-fire, explosions and other special sound effects in PCM to accompany the main music rhythm.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- 8-channel speech / melody
- Operating voltage: 2.2V - 5.5V
- Four general inputs / outputs, IOAB0~3
- Four input pins, IOCD2 and IOEF0~2
- Two audio output pins drive speaker directly
- Watchdog mode (code option)
- 224 bytes SRAM
- 64K bytes program ROM
- Power down mode with system and auto wake-up clock stop
- Halt mode with system clock stop, but keeping auto-wakeup clock working
- Built-in max. 14.318MHz R_{OSC}
- Power-on reset
- Volume adjustment by 3-bit software control or external resistor
- Key-change and system auto wakeup capability
- Low voltage reset

4. APPLICATION FIELDS

- Electronic piano
- Music clock
- Music box
- Children's storybook

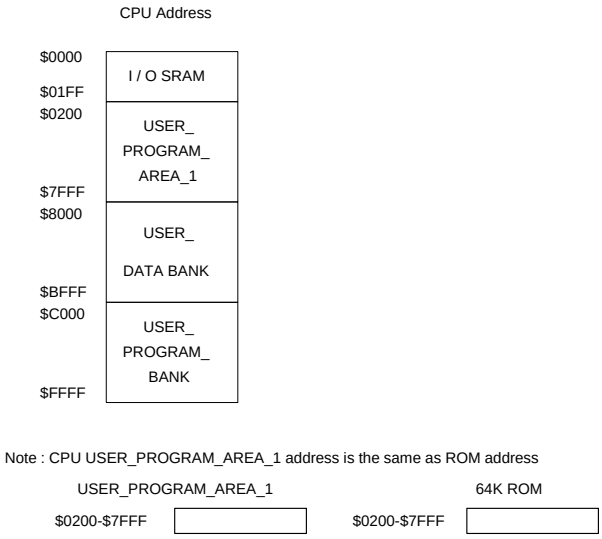
5. PAD ASSIGNMENT AND SIGNAL DESCRIPTIONS

5.1. Signal Description

Mnemonic	PIN No.	Type	Description
VDD	1	I	Positive supply voltage
VSS	11	I	Ground input
RESETB	10	I	Reset input, active low, internal pull high
VM	17	I	Capacitor input ,should connect it with 0.1uF capacitor to AVSS
LFC	18	I	Capacitor input, should connect it with 50nF capacitor to AUDN
AUDN AUDP	15 13	O	Audio output
IOCD2 IOEF2 - 0	5 4 - 2	I	Data input pins
IOAB3 - 0	9 - 6	I/O	Programmable input/output pins
AVSS1 AVSS2	16 12	I	Analog VSS
AVDD	14	I	Analog VDD

6. FUNCTION DESCRIPTION

6.1. Memory Mapping



6.2. CPU

The 8-bit micro-processor of GPFA64D1 is a high performance processor equipped with Accumulator, Program Counter, X Register, Stack pointer, and Processor Status Register (this is the same as the 6502 instruction structure). GPFA64D1 is able to reach 7.16MHz (max.) performing speed depending on the application specifications.

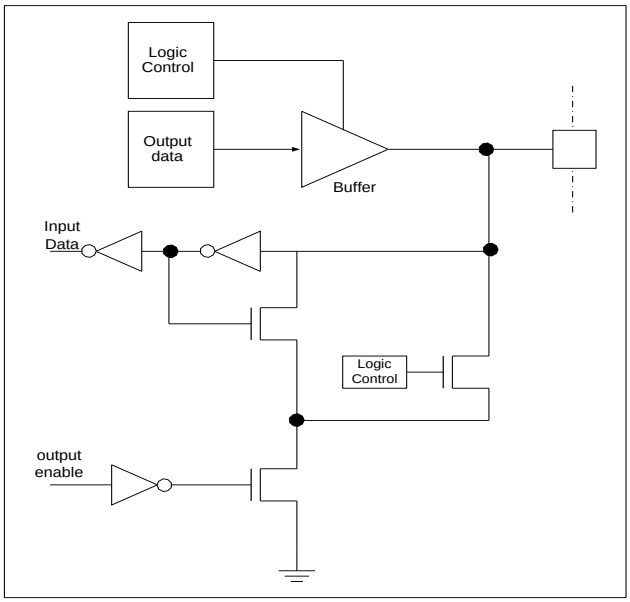
6.3. Oscillator

The GPFA64D1 provides an internal 14.318MHz ROSC for system clock source and it takes less cost and component for user's system. In addition to 14.318Mhz system clock, GPFA64D1 also equips a 41KHz ROSC that will be the auto wakeup clock source. The wakeup frequency can be 2.5Hz, 5Hz, 10Hz and 20Hz depending on bit-2&3 in P_07H_SleepWakeup. Note that the 41KHz ROSC can be activated only when system is under sleep mode and the relevant control register, P_07_SleepWakeup, in which bit-1 is written as "1".

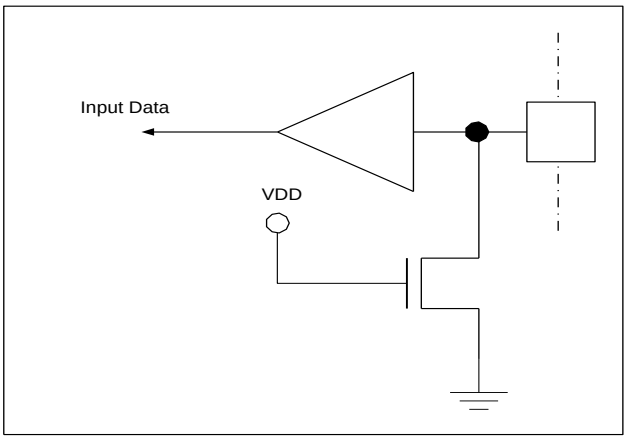
**Note: ***The frequency deviation for auto wakeup clock may be +-30%.
**Note: ****The frequency deviation for internal ROSC is +-3.5%.

6.4. I/O Port Configuration

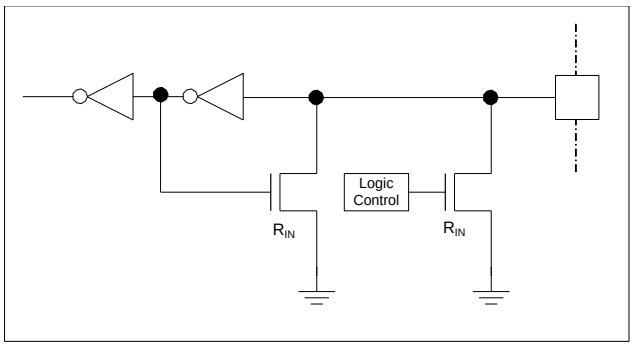
IOAB.0-3: Input/Output Port



IOCD.2: Input Port



IOEF.0-2: Input Port



6.5. Key and Auto-Wakeup

CPU waking up from sleep mode requires a wakeup signal to turn the system clock on. The wakeup sources of GPFA64D1 include IOEF.0-2 key change and auto wakeup.

6.6. Interrupt

The GPFA64D1 has two interrupt modes: FIQ (Fast Interrupt Request) and IRQ (Interrupt Request). The priority of FIQ is higher than IRQ. FIQ is the high-priority interrupt while IRQ is low-priority. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt source. The interrupt controller handles 7 INTs sources, which are depicted in the following table:

Interrupt Source	Priority
Channel 3 interrupt	IRQ
Channel 2 interrupt	IRQ
Channel 1 interrupt	IRQ
Channel 0 interrupt	FIQ/IRQ (by program)*
T11 interrupt (system CLK/4096)	IRQ
T8 interrupt (system CLK/512)	IRQ
External interrupt	IRQ

Note: *User can assign the priority to FIQ or IRQ via programming.

6.7. Generation of Speech and Melody

The fixed address of RAM area $0020 - $005F is designed as address pointers and a data buffer for the 8 channel speech/melody generation. When a channel is defined as speech, the user sets the 16-bit address pointer to point to the ROM area. The data can directly be sent to DA in direct output mode. The EA register is used to control the volume of the speech at AUD output. If the channel is defined as a melody channel, user should set it to normal speech mode, fetch the chord and decode the note first. After that, the user should set the channel to melody mode, which selects the tone ROM for programming and controlling the envelope to choose an instrument. Then play the data to DA buffer in synchronous rhythm with the change of the time base (tempo).

6.8. Power Down and Halt Mode

GPFA64D1 supports a power saving mode for those applications that need very low standby current. Simply enable the wakeup sources and then stop the CPU clock by writing the SLPSTAR register. Thus, CPU will enter standby mode, and all RAM and I/Os will retain at their previous states until wakeup. If auto wakeup is needed, the 41KHz ROSC enable bit, P_07H_SleepWakeup bit-1, should be written as "1". It will stop the CPU clock but keep auto wakeup clock working by writing the SLPSTAR register.

6.9. Main Volume Control Function

The main volume adjustment of GPFA64D1 provides 3-bit (8 level) software control to adjust D/A output voltage. The software volume control register is P_09_Vol_Ctrl bit0-2 and its default value is #05H that is about 60% of maximum volume. Users can adjust volume by writing different values into P_09_Vol_Ctrl bit0-2. The larger value written, the larger volume is implemented.

6.10. AUD Control Function

GPFA64D1 facilitates AUD output to drive speaker directly. In order to eliminate the start-up noise, it is not allowed turning on the AUD enable control registers, P_00H_DACOP_EN bit0-1, at the same time. User should write the control registers with an interval, which is not less than 10us. The AUD turn-on procedure should be as follows:

1. Set envelope data=00H, DAC data=80H.
2. Set P_00H_DACOP_EN = 01H.
3. Delay 10us.
4. Set P_00H_DACOP_EN = 03H.

If user disables AUD output, it is also not allowed turning off the AUD control register at the same time, or the unexpected noise might be generated. The AUD turn-off procedure should be as followings:

1. Set envelope data=00H, DAC data=80H.
2. Set P_00H_DACOP_EN = 01H.
3. Delay 10us.
4. Set P_00H_DACOP_EN = 00H.

Low Voltage Reset

The Low Voltage Reset (LVR), preventing system from running into malfunction state, will intend to reset all functions back to the initial states if the system power drops too low.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	VDD	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to VDD + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Ratings table may cause permanent damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

7.2. DC Characteristics (TA=25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.2	-	5.5	V	-
Operating Current-1 (internal DAC and Amplifier active)	I_{OP1}	-	15.7	-	mA	F_{CPU} = 7.16MHz @ 5.0V, no load
		-	8.5	-	mA	F_{CPU} = 7.16MHz @ 3.0V, no load
Operating Current-2 (internal DAC and Amplifier inactive)	I_{OP2}	-	6.3	-	mA	F_{CPU} = 7.16MHz @ 5.0V, no load
		-	2.5	-	mA	F_{CPU} = 7.16MHz @ 3.0V, no load
Standby Current	I_{STBY}	-	-	3.0	μA	VDD = 5.0V
OSC Frequency	F_{OSC2}	-	14.318	-	MHz	VDD = 5.0V
Frequency lot deviation	$\triangle F_{OSC2}/F_{OSC2}$	-3.5	-	3.5	%	(F_{OSC2} (VDD_CORE)-14.318MHz) /14.318MHz, VDD_CORE =3.3V, For Internal OSC
Input High Level	V_{IH}	0.7*VDD	-	-	V	-
Input Low Level	V_{IL}	-	-	0.3*VDD	V	-
Output High Current (IOAB[3:0])	I_{OH}	-	17.0	-	mA	VDD = 5.0V, V_{OH} = 0.8xVDD
		-	7.0	-	mA	VDD = 3.0V, V_{OH} = 0.8xVDD
Output Sink Current (IOAB[2:0])	I_{OL}	-	-42.0	-	mA	VDD = 5.0V, V_{OL} = 0.2xVDD
		-	-19.0	-	mA	VDD = 3.0V, V_{OL} = 0.2xVDD
Output Sink Current (IOAB[3])	I_{OL}	-	-60.0	-	mA	VDD = 5.0V, V_{OL} = 0.2xVDD
		-	-28.0	-	mA	VDD = 3.0V, V_{OL} = 0.2xVDD
Input Pull-Low Resistor (IOEF[2:0])	R_{PL}	-	100	-	Kohm	VDD = 5.0V, VIN = VDD
		-	205	-	Kohm	VDD = 3.0V, VIN = VDD
Input Pull-Low Resistor (IOCD2)	R_{PL}	-	100	-	Kohm	VDD = 5.0V, VIN = VDD
		-	205	-	Kohm	VDD = 3.0V, VIN = VDD
CPU Clock	F_{CPU}	-	7.16	-	MHz	F_{CPU} = F_{OSC2} /2

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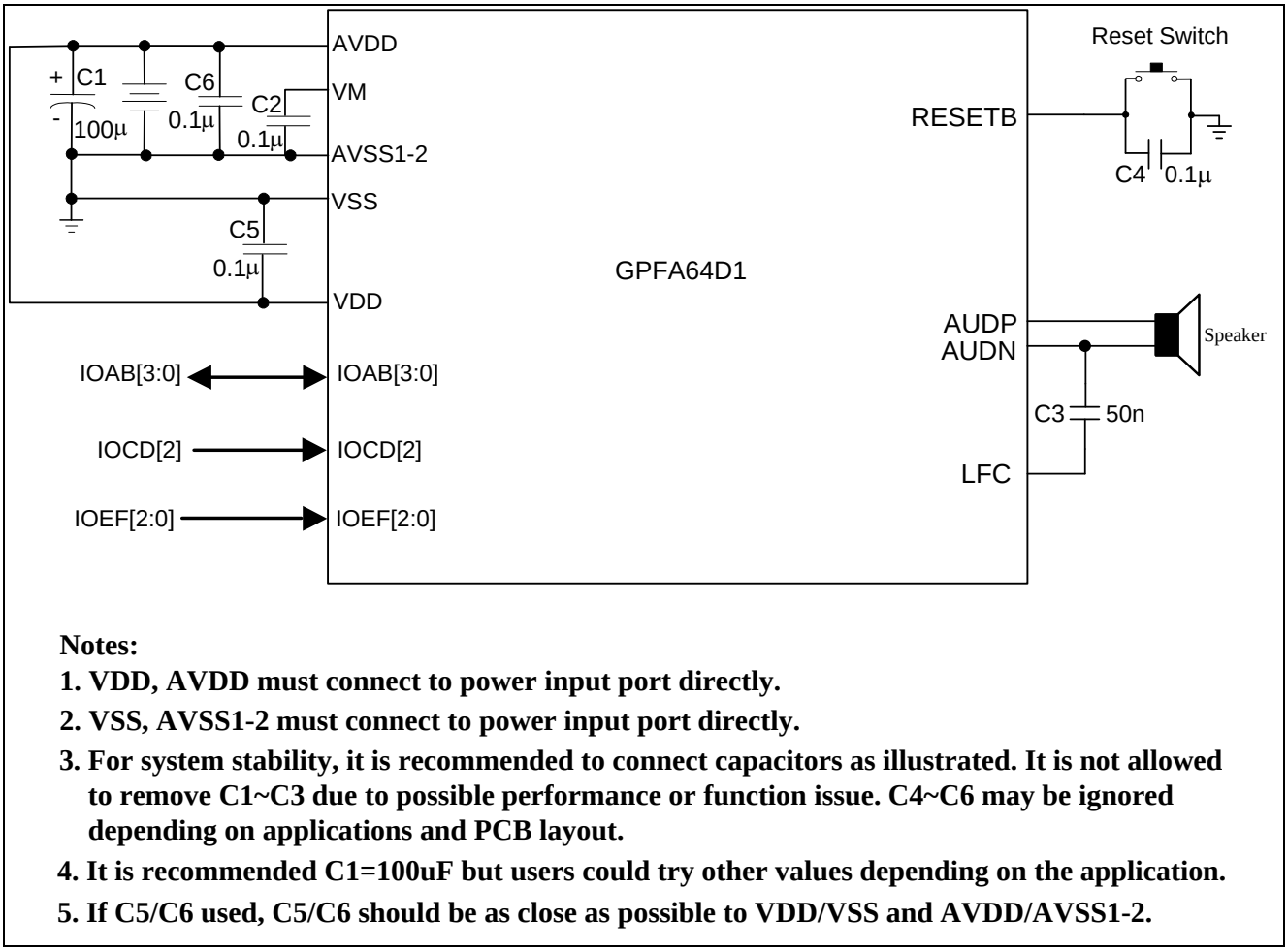
8. APPLICATION CIRCUIT

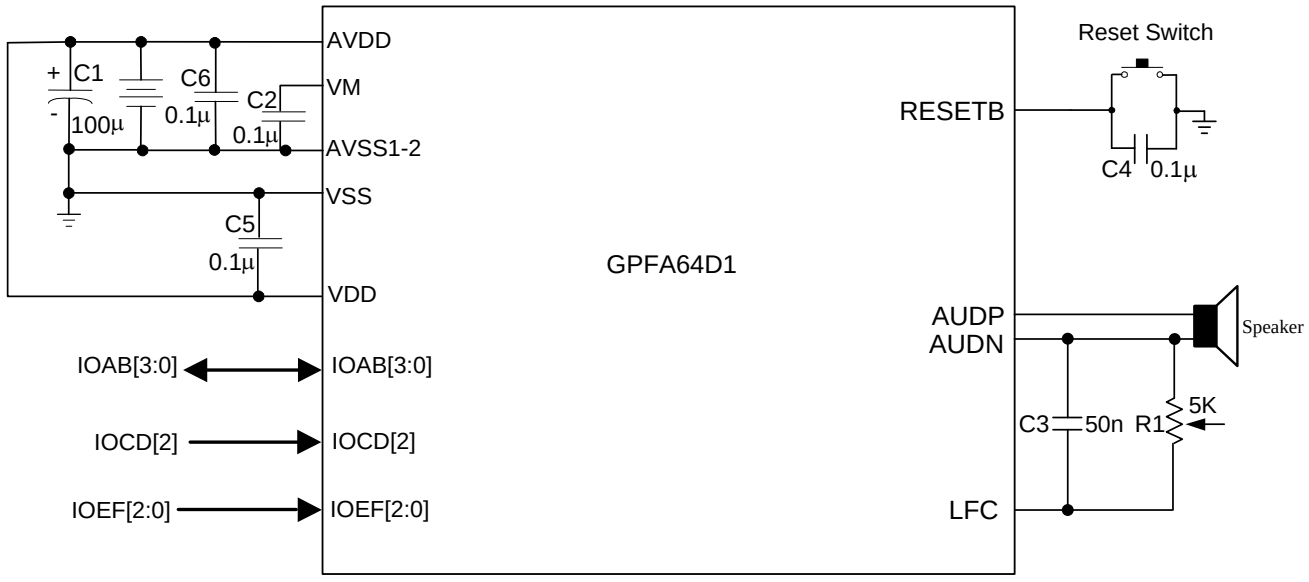
8.1. GPFA64D1 Application Circuits-(1): Application Circuit without External Resistor for Volume Control



Notes:

1. **VDD, AVDD must connect to power input port directly.**
2. **VSS, AVSS1-2 must connect to power input port directly.**
3. **For system stability, it is recommended to connect capacitors as illustrated. It is not allowed to remove C1~C3 due to possible performance or function issue. C4~C6 may be ignored depending on applications and PCB layout.**
4. **It is recommended C1=100uF but users could try other values depending on the application.**
5. **If C5/C6 used, C5/C6 should be as close as possible to VDD/VSS and AVDD/AVSS1-2.**

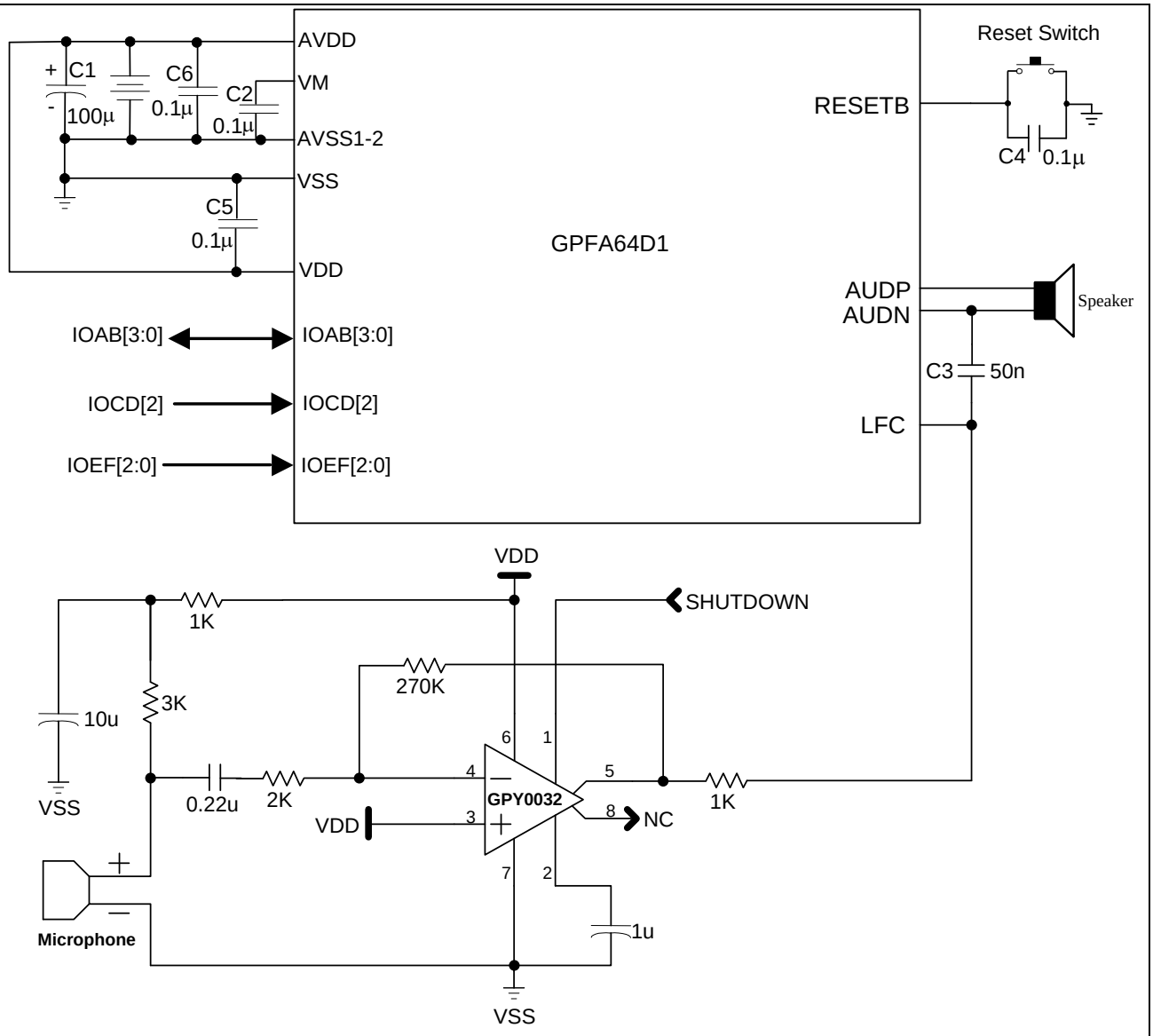
8.2. GPFA64D1 Application Circuits-(2): Application Circuit with External Resistor for Volume Control



Notes:

1. **VDD, AVDD must connect to power input port directly.**
2. **VSS, AVSS1-2 must connect to power input port directly.**
3. **For system stability, it is recommended to connect capacitors as illustrated. It is not allowed to remove C1~C3 due to possible performance or function issue. C4~C6 may be ignored depending on applications and PCB layout.**
4. **It is recommended C1=100uF but users could try other values depending on the application.**
5. **If C5/C6 used, C5/C6 should be as close as possible to VDD/VSS and AVDD/AVSS1-2.**
6. **Connecting variable resistor, R1(max.=5K), between LFC and AUDN for volume control**

8.3. GPFA64D1 Application Circuits-(3): Application Circuit for Microphone Audio Input



Notes:

1. **VDD, AVDD must connect to power input port directly.**
2. **VSS, AVSS1-2 must connect to power input port directly.**
3. **For system stability, it is recommended to connect capacitors as illustrated. It is not allowed to remove C1~C3 due to possible performance or function issue. C4~C6 may be ignored depending on applications and PCB layout.**
4. **It is recommended C1=100uF but users could try other values depending on the application.**
5. **If C5/C6 used, C5/C6 should be as close as possible to VDD/VSS and AVDD/AVSS1-2.**
6. **For microphone audio input application, external circuit is as illustrated. The SHUTDOWN signal to GPY0032 could be GPFA64D1 GPIO.**

9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPFA64D1-NnnV-A	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
Oct. 21, 2015	1.1	Modify Internal OSC SPEC in section 6.3 & 7.2	5, 7
Sep. 01, 2015	1.0	Add DC Characteristics in section 7.2	7
Jul. 20, 2015	0.1	Original	13