DATA SHEET

GPFA64F1

8-ch 64KB ROM Music Synthesizer

Oct. 12, 2015

Version 1.0

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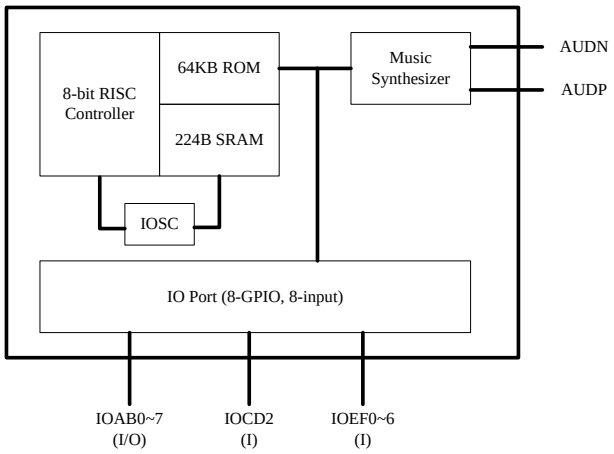
8-CH 64KB ROM MUSIC SYNTHESIZER

1. GENERAL DESCRIPTION

The GPFA64F1, a fully CMOS integrated circuit, adopts advanced design and process technology to combine an 8-bit RISC processor, an 8-channel music synthesizer, 64K bytes program ROM, 224 bytes working SRAM, timer/counter and I/Os interface in a single chip. The sound processing logic is a unique design to achieve high quality melody effect. It can simulate all types of musical instruments by programming the tone ROM and controlling the envelope slope of each channel. Every channel can also be defined as a speech channel to produce percussion, animal sounds, gun-fire, explosions and other special sound effects in PCM to accompany the main music rhythm.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- Features 8 channel speech / melody
- Operating voltage: 2.2V - 5.5V
- Eight general inputs / outputs, IOAB0~7(IOAB3 is high sink)
- Eight input pins, IOCD2 and IOEF0~6
- Sleep signal output
- Two audio output pins drive speaker directly
- Watchdog mode (code option)
- 224 bytes SRAM
- 64K bytes program ROM
- Power down mode with system and auto wake-up clock stop
- Halt mode with system clock stop but auto wake-up clock working
- Built-in 14.318MHz R_{OSC}
- Power-on reset
- Volume adjustment by 3-bit software control or external resistor
- Key-change and auto wakeup capability
- Low voltage reset

4. APPLICATION FIELDS

- Electric piano
- Music clock
- Music box
- Children's storybooks

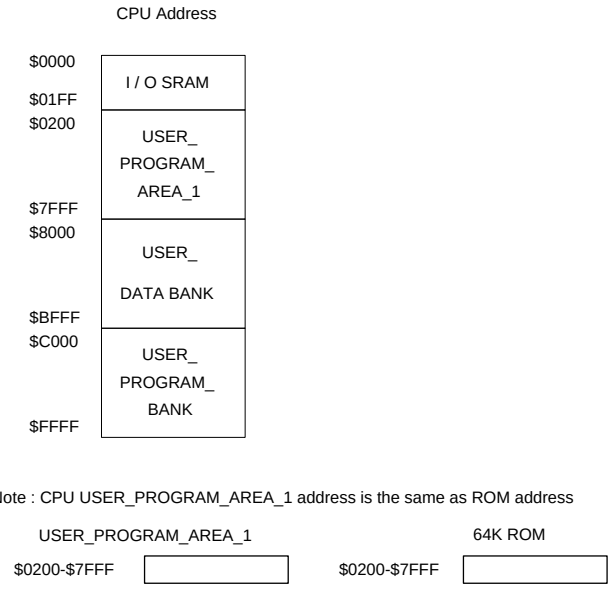
5. SIGNAL DESCRIPTION

Mnemonic	Type	Description
VDD1 VDD2 VDD3	I I I	Positive supply voltage
VSS1 VSS3	I I	Ground input
RESETB	I	Reset input, active low, internal pull high
VM	I	Capacitor input ,should connect it with 0.1uF capacitor to AVSS
LFC	I	Capacitor input, should connect it with 50nF capacitor to AUDN
AUDN AUDP	O	Audio output
IOCD2 IOEF0-6	I I	Data input pins
IOAB0-7	I/O	Programmable input/output pins
SLEEP	O	Sleep output signal
AVSS1 AVSS2	I	Analog VSS
AVDD	I	Analog VDD

Note: AVDD/AVSS1-2/AUDN/AUDP pads are highly recommended to be double-bonded.

6. FUNCTIONAL DESCRIPTIONS

6.1. Memory Mapping



Note : CPU USER_PROGRAM_AREA_1 address is the same as ROM address

6.2. CPU

The 8-bit microprocessor in GPFA64F1 is a high performance processor equipped with Accumulator, Program Counter, X Register, Stack pointer and Processor Status Register (this is the same as the 6502 instruction structure). GPFA64F1 is able to perform with 7.16MHz (max.) depending on the application specifications.

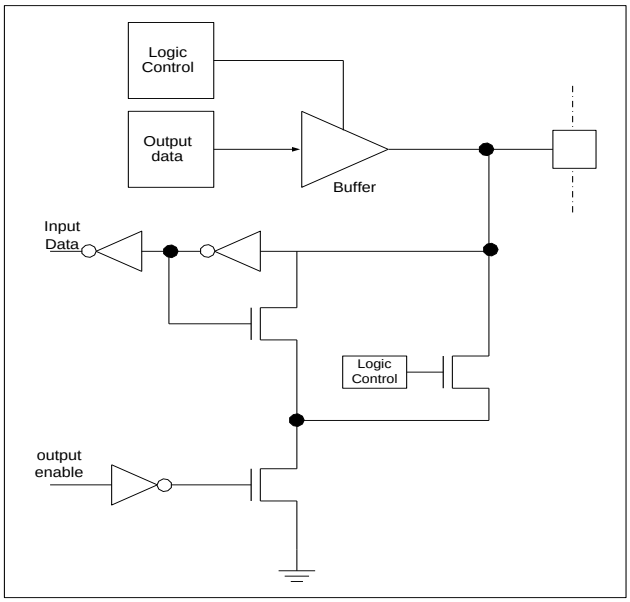
6.3. Oscillator

The GPFA64F1 features an internal 14.318MHz ROSC for system clock source and it will take less cost and component for user's systems. In addition to 14.318MHz system clock, GPFA64F1 also features a 41KHz-ROSC that will be the auto wakeup clock source. The wake-up frequency can be 2.5Hz, 5Hz, 10Hz and 20Hz based on the settings of bit2 and bit3 in P_07H_SleepWakeup. Note that the 41KHz ROSC can be activated only when the system is under sleep mode and the related control register, P_07_SleepWakeup, bit-1 is written as "1".

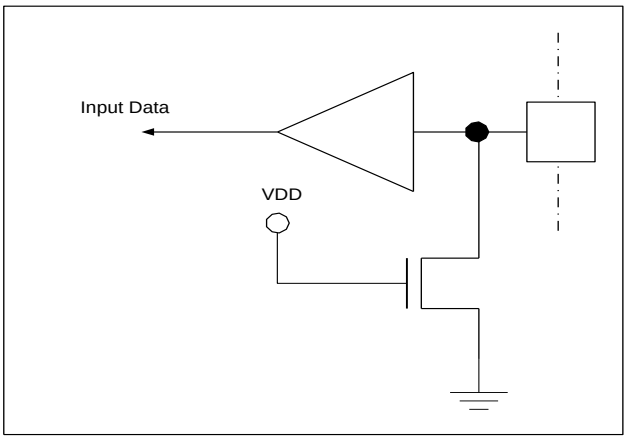
Note: *The frequency deviation for auto wake-up clock may be +-30%

6.4. I/O Port Configuration

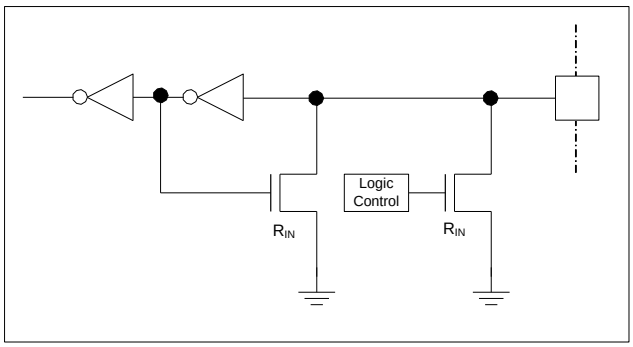
IOAB.0-7: Input/Output Port



IOCD.2: Input Port



IOEF.0-6: Input Port



6.5. Key and Auto Wake-up

CPU waking up from sleep mode requires a wake-up signal to turn the system clock on. The wake-up sources of GPFA64F1 include IOEF.0-6 key change and auto wake-up.

6.6. Interrupt

The GPFA64F1 has two interrupt modes: FIQ (Fast Interrupt Request) and IRQ (Interrupt Request). The priority of FIQ is higher than IRQ. FIQ is the high-priority interrupt while IRQ is the low-priority one. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt source. The interrupt controller handles 7 INTs sources as follows:

Interrupt Source	Priority
Channel 3 interrupt	IRQ
Channel 2 interrupt	IRQ
Channel 1 interrupt	IRQ
Channel 0 interrupt	FIQ/IRQ (by program)*
T11 interrupt (system CLK/4096)	IRQ
T8 interrupt (system CLK/512)	IRQ
External interrupt	IRQ

Note: *User can set the priority to be FIQ or IRQ by program.

6.7. Generation of Speech and Melody

The fixed address of RAM area $0020 - $005F is designed as address pointers and a data buffer for the 8-channel speech/melody generation. When a channel is defined as speech, user sets the 16-bit address pointer pointing to the ROM area. The data can directly be sent to DA in direct output mode. The EA register is used to control the volume of the speech at AUD output. If a channel is defined as a melody channel, user should set the channel to normal speech mode, fetch the chord and decode the note first. After that, user should set that channel to melody mode and select the tone ROM for programming and controlling the envelope to choose an instrument. Then, play the data to DA buffer in synchronous rhythm with the change of the time base (tempo).

6.8. Power Down and Halt Mode

GPFA64F1 supports a power saving mode for those applications requiring very low stand-by current. Simply enables the wake-up sources, and then stops the CPU clock by writing the SLPSTAR register. Thus, CPU will enter standby and the RAM and I/O retain in their previous state until being awakened. If auto wake-up is needed, the 41KHz ROSC enable bit, P_07H_SleepWakeup bit-1, should be written as “1” then stop the CPU clock but keep auto wake-up clock source activating by writing the SLPSTAR register.

6.9. Main Volume Control Function

The main volume adjustment of GPFA64F1 provides 3-bit (8 level) software control to adjust D/A output voltage. The software volume control register is P_09_Vol_Ctrl bit0-2 and its default value is #05H that is about 60% of maximum volume. Users can adjust volume by writing different values into P_09_Vol_Ctrl bit0-2. The larger value written, the larger volume is implemented.

6.10. AUD Control Function

GPFA64F1 facilitates AUD output to drive speaker directly. In order to eliminate the start-up noise, it is not allowed to turn on the AUD enable control registers, P_00H_DACOP_EN bit0-1, at the same time. Users should write the control registers with an interval which is not less than 10us. The AUD turn-on procedure should be as followings:

1. Set envelope data=00H, DAC data=80H.
2. Set P_00H_DACOP_EN = 01H.
3. Delay 10us.
4. Set P_00H_DACOP_EN = 03H.

If users disable AUD output, it is also not allowed to turn-off the AUD control register at the same time, or the unexpected noise might be generated as well. The AUD turn-off procedure should be as follows:

1. Set envelope data=00H, DAC data=80H.
2. Set P_00H_DACOP_EN = 01H.
3. Delay 10us.
4. Set P_00H_DACOP_EN = 00H.

6.11. Low Voltage Reset

The Low Voltage Reset (LVR), prevents system running into malfunction state, will intend to reset all functions back to the initial states if the system power drops extremely low.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	VDD	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to VDD + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

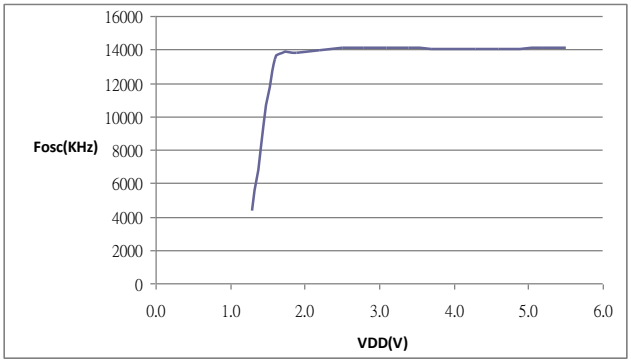
Note: Stresses beyond those given in the Absolute Maximum Ratings table may cause permanent damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. DC Characteristics

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.2	-	5.5	V	-
Operating Current-1 (internal DAC and Amplifier active)	I_{OP1}	-	12.1	-	mA	F_{CPU} = 7.16MHz @ 5.0V, no load
		-	6.2	-	mA	F_{CPU} = 7.16MHz @ 3.0V, no load
Operating Current-2 (internal DAC and Amplifier inactive)	I_{OP2}	-	6.0	-	mA	F_{CPU} = 7.16MHz @ 5.0V, no load
		-	2.3	-	mA	F_{CPU} = 7.16MHz @ 3.0V, no load
Standby Current	I_{STBY}	-	-	3.0	μA	VDD = 5.0V
OSC Frequency	F_{OSC2}	-	14.318	-	MHz	VDD = 3.3V@25℃
Frequency lot deviation	$\Delta F_{OSC2}/F_{OSC2}$	-3.5	-	3.5	%	(F_{OSC2} (VDD_CORE)-14.318Mhz) /14.318MHz, VDD_CORE =3.3V, For Internal OSC
Input High Level	V_{IH}	0.7*VDD	-	-	V	-
Input Low Level	V_{IL}	-	-	0.3*VDD	V	-
Output High Current (IOAB[7:0])	I_{OH}	-	15.7	-	mA	VDD = 5.0V, V_{OH} = 4.0V
		-	6.7	-	mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink Current (IOAB[7:4,2:0])	I_{OL}	-	40.0	-	mA	VDD = 5.0V, V_{OL} = 1.0V
		-	18.0	-	mA	VDD = 3.0V, V_{OL} = 0.6V
Output Sink Current (IOAB[3])	I_{OL}	-	55.1	-	mA	VDD = 5.0V, V_{OL} = 1.0V
		-	25.6	-	mA	VDD = 3.0V, V_{OL} = 0.6V
Input Pull-Low Resistor (IOEF[6:0])	R_{PL}	-	110	-	Kohm	VDD = 5.0V, VIN = VDD
		-	225	-	Kohm	VDD = 3.0V, VIN = VDD
Input Pull-Low Resistor (IOCD2)	R_{PL}	-	110	-	Kohm	VDD = 5.0V, VIN = VDD
		-	225	-	Kohm	VDD = 3.0V, VIN = VDD
CPU Clock	F_{CPU}	-	7.16	-	MHz	VDD = 3.3V@25℃

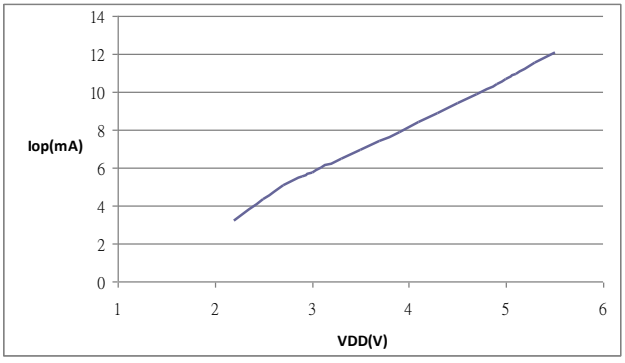
7.3. The Relationships between the F_{OSC} and the VDD

7.3.1. TA=25℃



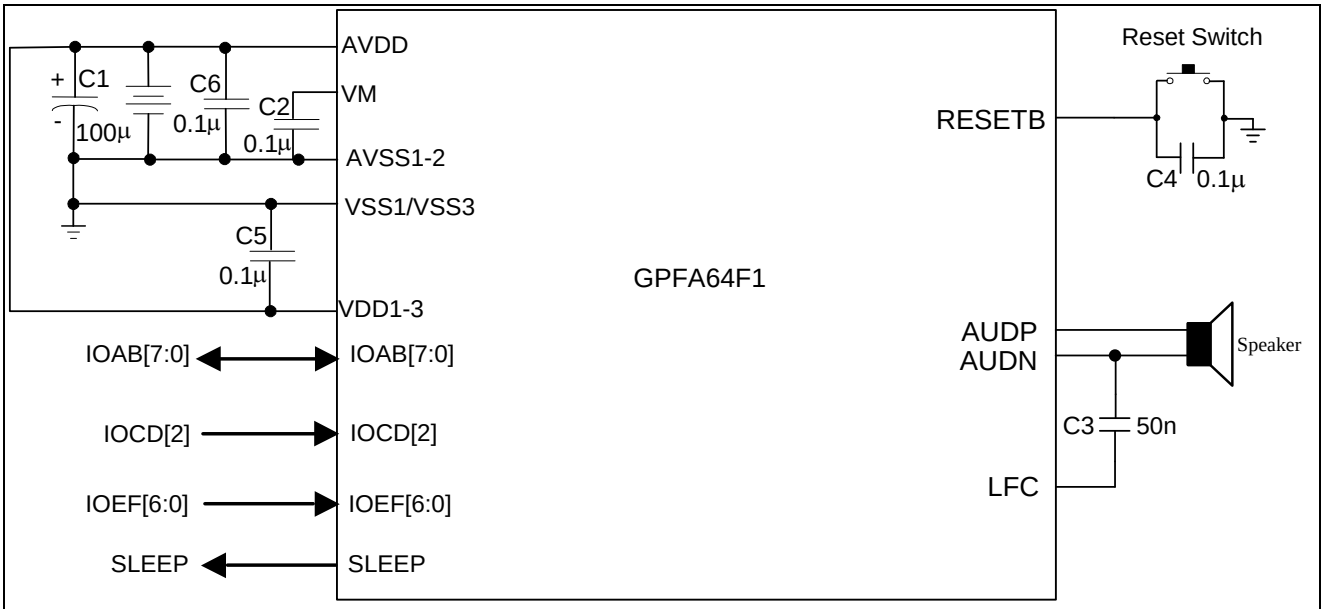
7.4. The Relationships between the VDD and the I_{OP}

7.4.1. TA=25℃(internal DAC and Amplifier active)



8. APPLICATION CIRCUIT

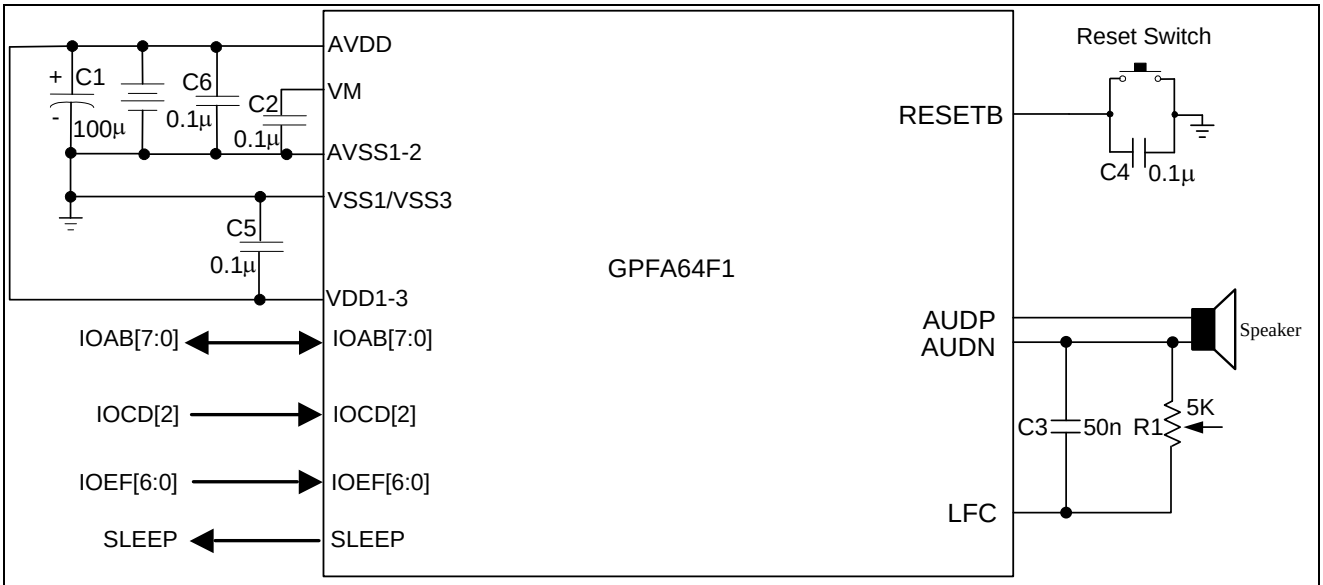
8.1. GPFA64F1 Application Circuits-(1): Application Circuit without External Resistor for Volume Control



Notes:

1. **VDD1-3, AVDD must connect to power input port directly.**
2. **VSS1/VSS3, AVSS1-2 must connect to power input port directly.**
3. **For system stability, it is recommended to connect capacitors as illustrated. It is not allowed to remove C1~C3 due to possible performance or function issue. C4~C6 may be ignored depending on applications and PCB layout.**
4. **It is recommended C1=100uF but users could try other values depending on the application.**
5. **If C5/C6 used, C5/C6 should be as close as possible to VDD1-3、VSS1/VSS3 and AVDD、AVSS1-2**

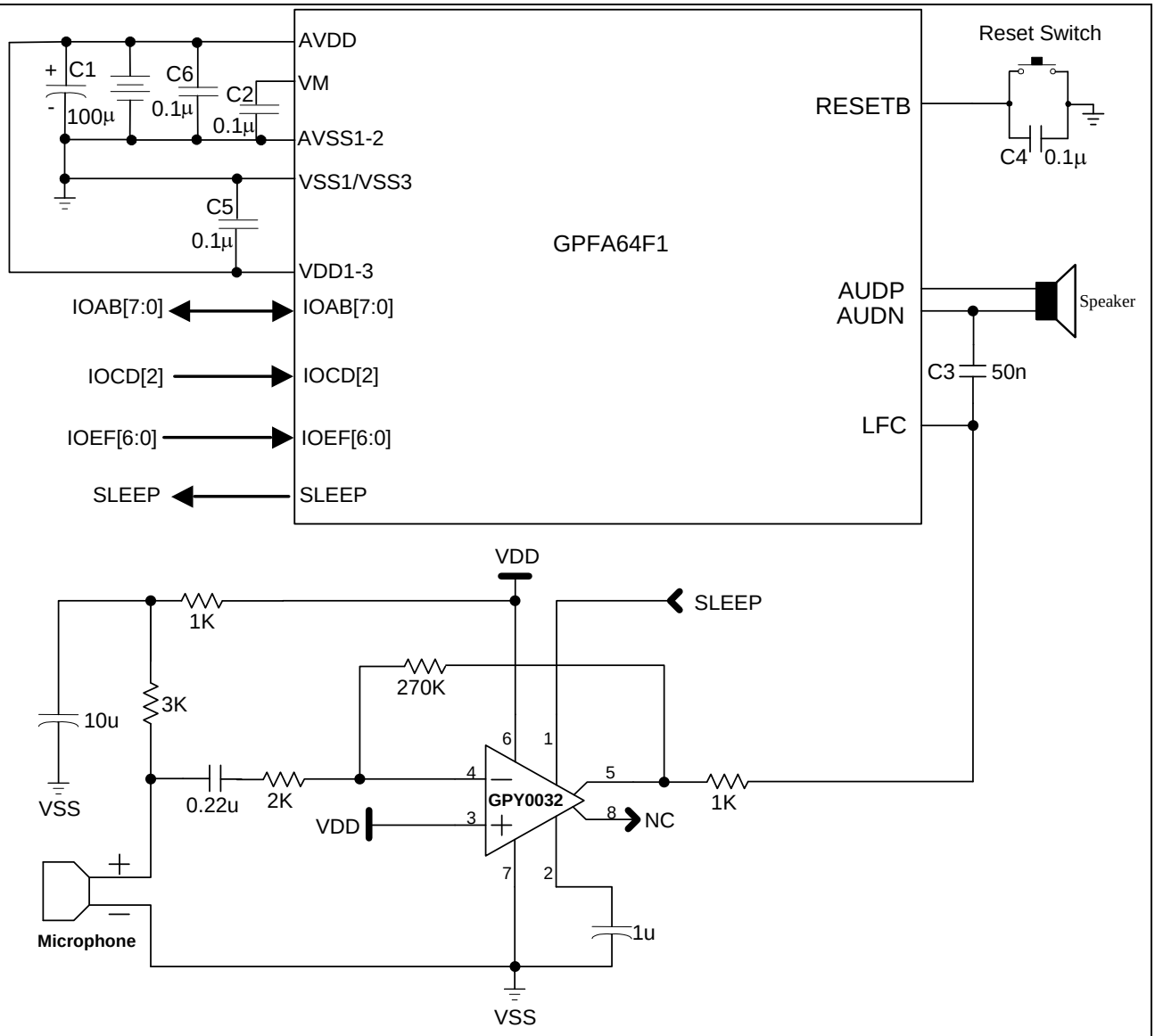
8.2. GPFA64F1 Application Circuits-(2): Application Circuit with External Resistor for Volume Control



Notes:

1. **VDD1-3, AVDD must connect to power input port directly.**
2. **VSS1/VSS3, AVSS1-2 must connect to power input port directly.**
3. **For system stability, it is recommended to connect capacitors as illustrated. It is not allowed to remove C1~C3 due to possible performance or function issue. C4~C6 may be ignored depending on applications and PCB layout.**
4. **It is recommended C1=100uF but users could try other values depending on the application.**
5. **If C5/C6 used, C5/C6 should be as close as possible to VDD1-3、VSS1/VSS3 and AVDD、AVSS1-2.**
6. **Connecting variable resistor, R1(max.=5K), between LFC and AUDN for volume control**

8.3. GPFA64F1 Application Circuits-(3): Application Circuit for Microphone Audio Input



Notes:

1. **VDD1-3, AVDD must connect to power input port directly.**
2. **VSS1/VSS3, AVSS1-2 must connect to power input port directly.**
3. **For system stability, it is recommended to connect capacitors as illustrated. It is not allowed to remove C1~C3 due to possible performance or function issue. C4~C6 may be ignored depending on applications and PCB layout.**
4. **It is recommended C1=100uF but users could try other values depending on the application.**
5. **If C5/C6 used, C5/C6 should be as close as possible to VDD1-3、VSS1/VSS3 and AVDD、AVSS1-2.**
6. **For microphone audio input application, external circuit is as illustrated. The SHUTDOWN signal to GPY0032 could be GPFA120F1 SLEEP output.**

9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPFA64F1-NnnV-A	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

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