DATA SHEET

GPL02E5

19.5KB LCD CONTROLLER/DRIVER

Oct. 19, 2017

Version 1.0

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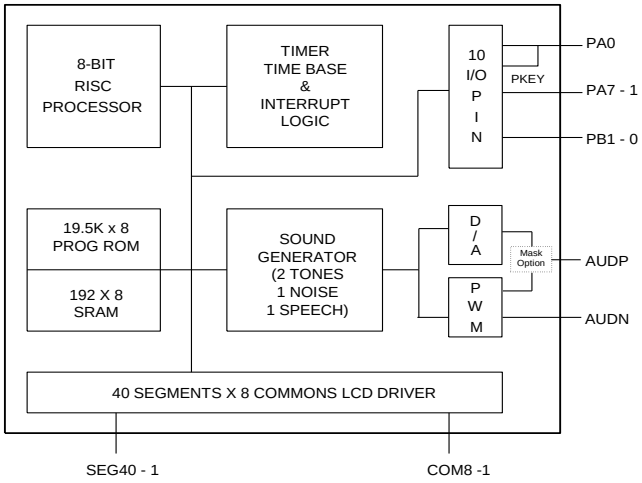
19.5KB LCD CONTROLLER/DRIVER

1. GENERAL DESCRIPTION

GPL02E5, a CMOS 8-bit single chip micro-processor, contains RAM, ROM, I/Os, one interrupt controller, two tone-generator, one noise generator, and one automatic display controller/driver. Based on application needs, users are welling to select either DAC or PWM for audio output through mask option. To reduce power consumption, a software controllable standby switch is built-in to render power management more efficiently.

2. BLOCK DIAGRAM



3. FEATURES

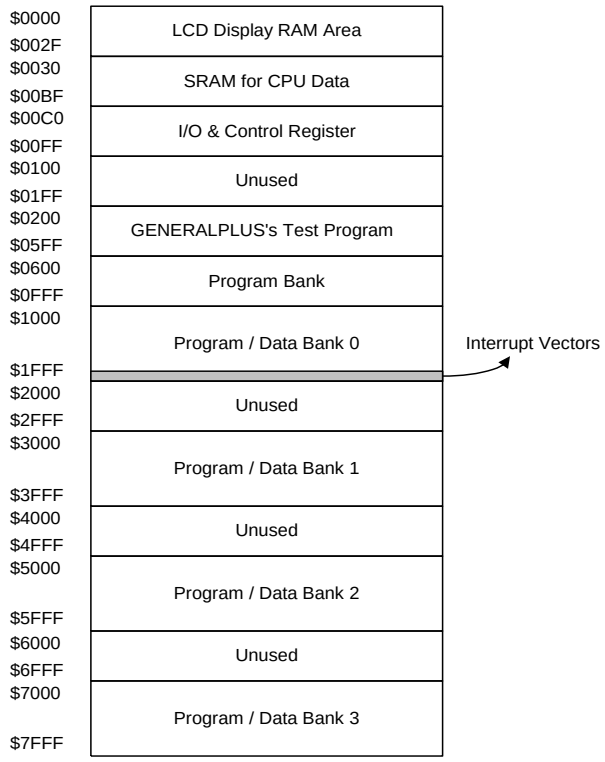
- Built-in 8-bit RISC processor
- 192-byte SRAM
- 19.5K-byte ROM
- Max. CPU clock: 1.5MHz @ 2.4V - 5.5V
- Operating voltage: 2.4V - 5.5V
- Built-in RC oscillator (only one resistor is needed)
- One 7-bit D/A for audio output or PWM audio output (mask option)
- Standby function available
- Operating current (enable LVRST)
  PWM: 480μA (700KHz @ 4.5V)
  DAC: 720μA (700KHz @ 4.5V)
- Extremely low standby current
  In standby mode: I_{STBY} < 1.0μA
- LCD matrix: 40 segments x 8 commons
  LCD bias: 1/4, 1/5
  LCD duty: 1/4, 1/8
- Two tone-channels and one noise channel for coding audio sound
- 10 general I/O pins for key input

4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
SEG40 - 23 SEG22 - 1	18 - 1 64 - 43	O	LCD driver segment output
COM8 - 1	26 - 19	O	LCD driver common output
PA7 - 0	34 - 41	I/O	I/O port
PB1 - 0	32 - 33	I/O	I/O port
ROSC	42	I	R-osc input, connect to VDD through resistor
RESET	27	I	System reset input
AUDP	29	O	Current DAC audio output, or PWM audio output (Mask Option)
AUDN	31	O	PWM audio output
VDD	30	I	Power input
VSS	28	I	Ground input

5. FUNCTIONAL DESCRIPTIONS

5.1. ROM Area



To access ROM area, users should program the BANK SELECT Register ($D7) first and then access bank #1, #2, or bank #3 by addressing the higher bank to fetch data.

5.2. System Operation Mode (R/W)

GPL02E5 provides normal mode and standby mode for user's options.

5.3. Interrupt (R/W)

GPL02E5 has three interrupt sources: 2Hz interrupt, Sound generator, and Power key

5.4. Low Voltage Reset (LVRST)

GPL02E5 features a low voltage reset function. Once LVRST function is enabled (by mask option), entire system will enter RESET state if and only if the power supply voltage VDD is lower than 2.2V (typical).

5.5. I/O Port

5.5.1. IOA (R/W)

b7, 6, 5, 4 -nibble 1

b3, 2, 1, 0 -nibble 0

5.5.2. IOB (R/W)

b1, 0 -nibble 2

5.6. LCD Display Controller

There are total of 8 commons and 40 segments available in GPL02E5. The 40-byte SRAM are allocated at $00-$2Fh for displaying LCD data.

5.7. Control Byte of I/O Port and LCD Duty Rate Port (W)

1). Set IOA, IOB as input status or output status

2). Set LCD duty

3). Set CPU clock rate: non-divided or divided-by-8

5.8. Tone and Noise

GPL02E5 equips two tone-generator and one noise-generator. Totally, 10 bits are used for programming the tone frequency, and two registers for controlling the amplitude of ToneA and ToneB. Two types of noise can be chosen and one register can be used to control the amplitude of noise.

5.9. Speech Play Control Port (W)

b0 = 0: non play mode

1: speech play mode

5.10. Speech Port (R/W)

In speech play mode, once data is written to the speech port, it is pumped to speaker through D/A or PWM (mask option) converter. The bit7 is a sign bit, '0' representing for positive data and '1' for negative data. Both bit0 to bit5 are magnitude bits.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics (VDD = 3.0V, T_A = 25℃)

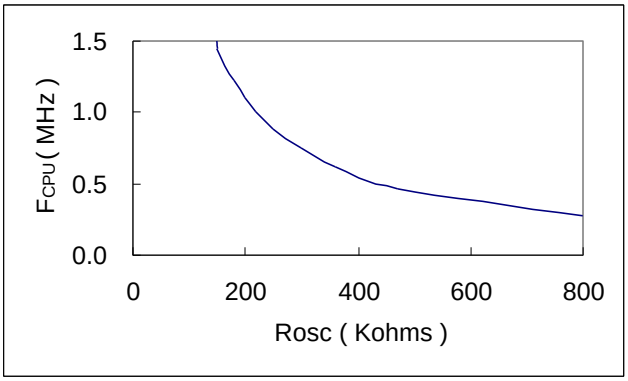
Characteristics	Symbol	Limit			Unit	Test condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery application
Operating Current	I_{OP}	-	380	-	μA	VDD = 3.0V, F_{CPU} = 700KHz
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 3.0V
Audio output current	I_{OH}	-	-35	-	mA	VDD = 3.0V, V_{OH} = 2.0V
	I_{OL}	-	40	-	mA	VDD = 3.0V, V_{OL} = 0.8V
Input High Level	V_{IH}	-	0.5*VDD	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	0.5*VDD	-	V	VDD = 3.0V
Output High I	I_{OH}	-	-1.0	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Output Sink I	I_{OL}	-	1.1	-	mA	VDD = 3.0V, V_{OL} = 0.8V

6.3. DC Characteristics (VDD = 4.5V, T_A = 25℃)

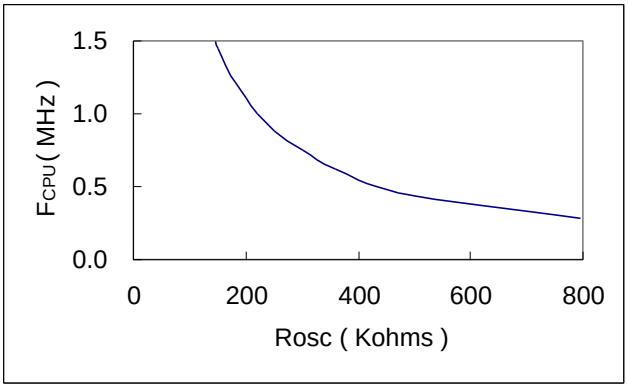
Characteristics	Symbol	Limit			Unit	Test condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery application
Operating Current	I_{OP}	-	720	-	μA	VDD = 4.5V, F_{CPU} = 700KHz
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 4.5V
Audio output current	I_{OH}		- 45	-	mA	VDD = 4.5V, V_{OH} = 3.5V
	I_{OL}	-	50	-	mA	VDD = 4.5V, V_{OL} = 0.8V
Input High Level	V_{IH}	-	0.5*VDD	-	V	VDD = 4.5V
Input Low Level	V_{IL}	-	0.5*VDD	-	V	VDD = 4.5V
Output High I	I_{OH}	-	-1.3	-	mA	VDD = 4.5V, V_{OH} = 3.5V
Output Sink I	I_{OL}	-	1.4	-	mA	VDD = 4.5V, V_{OL} = 0.8V

6.4. The Relationships between the R_{OSC} and the F_{OSC}

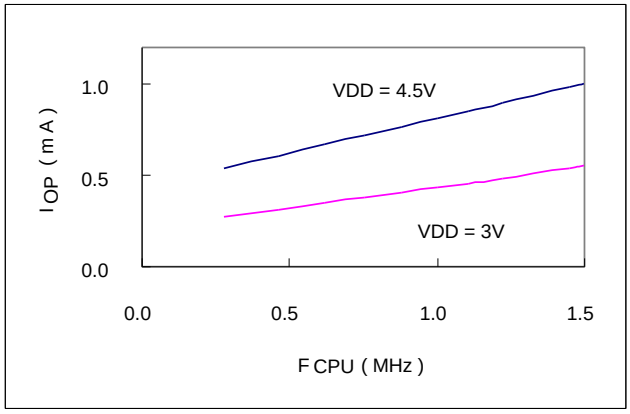
6.4.1. VDD = 3.0V, T_A = 25℃



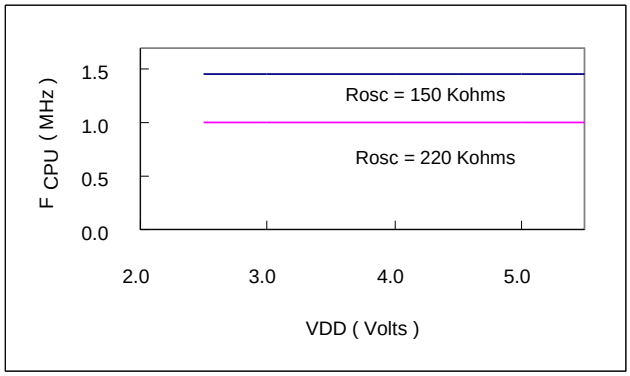
6.4.2. VDD = 4.5V, T_A = 25℃



6.5. The Relationships between the F_{CPU} and the I_{OP}

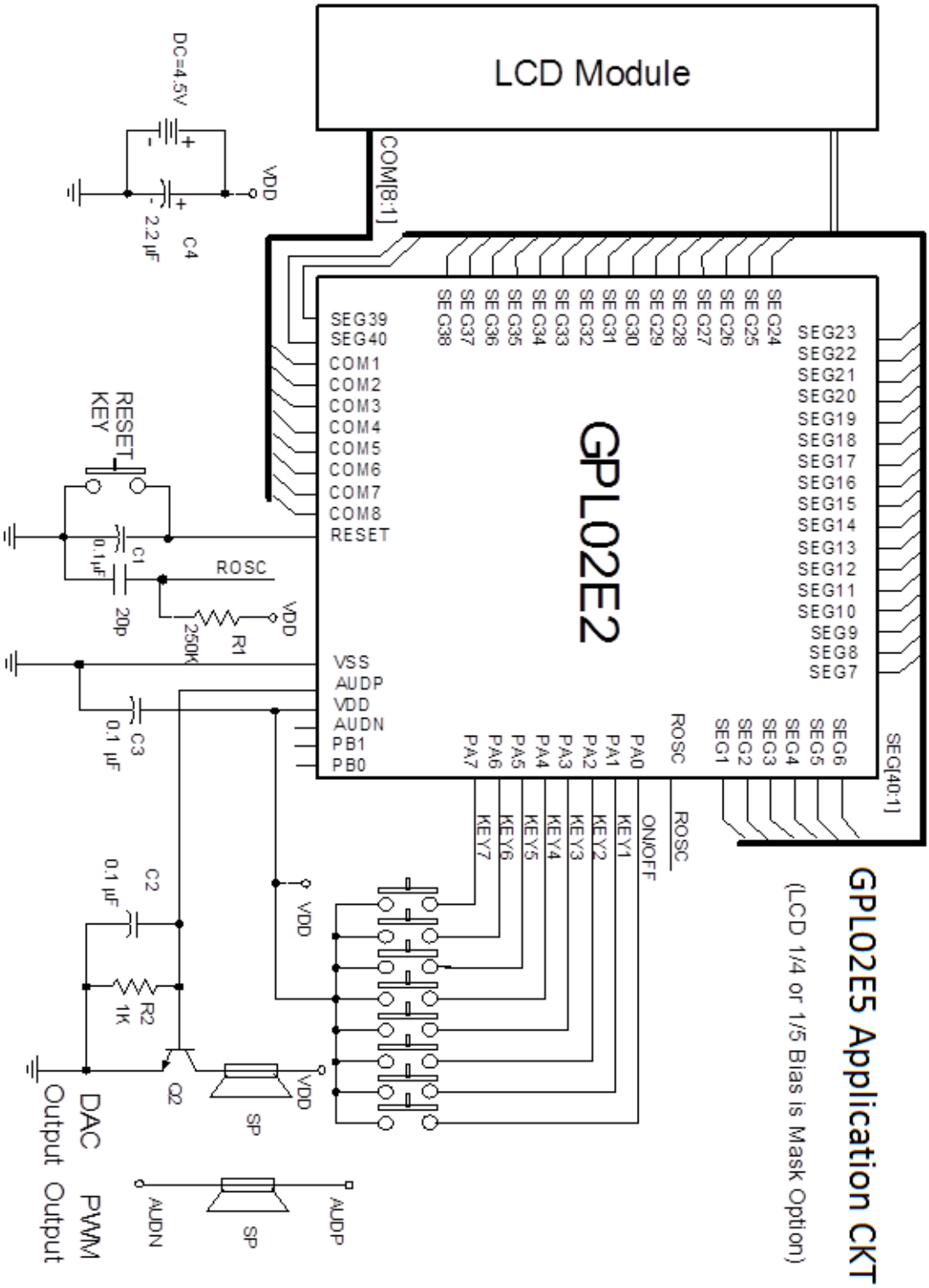


6.6. The Relationships between the F_{CPU} and the VDD



7. APPLICATION CIRCUITS

7.1. Application Circuit



7.2. Current Mode DAC Speaker Driver

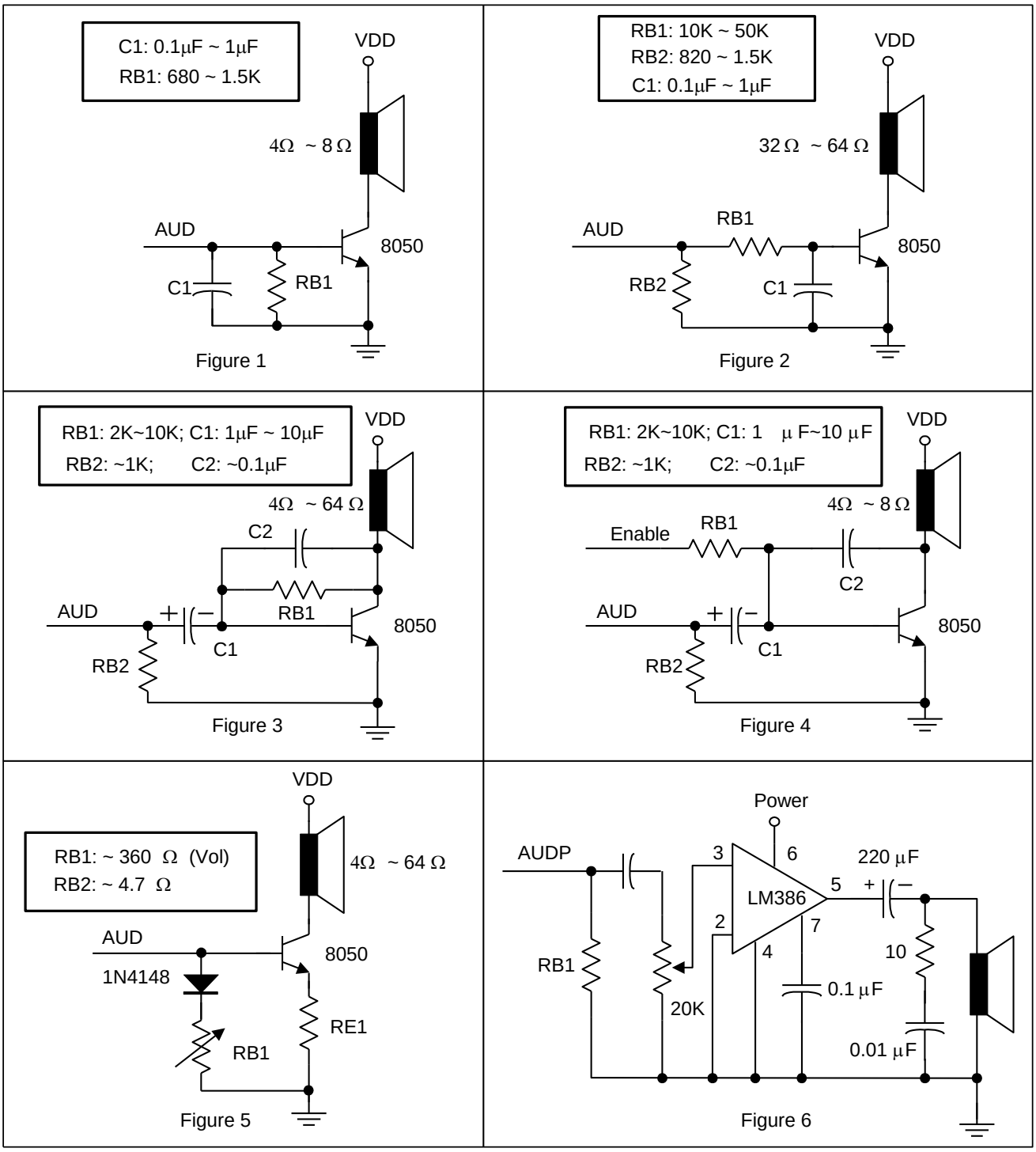
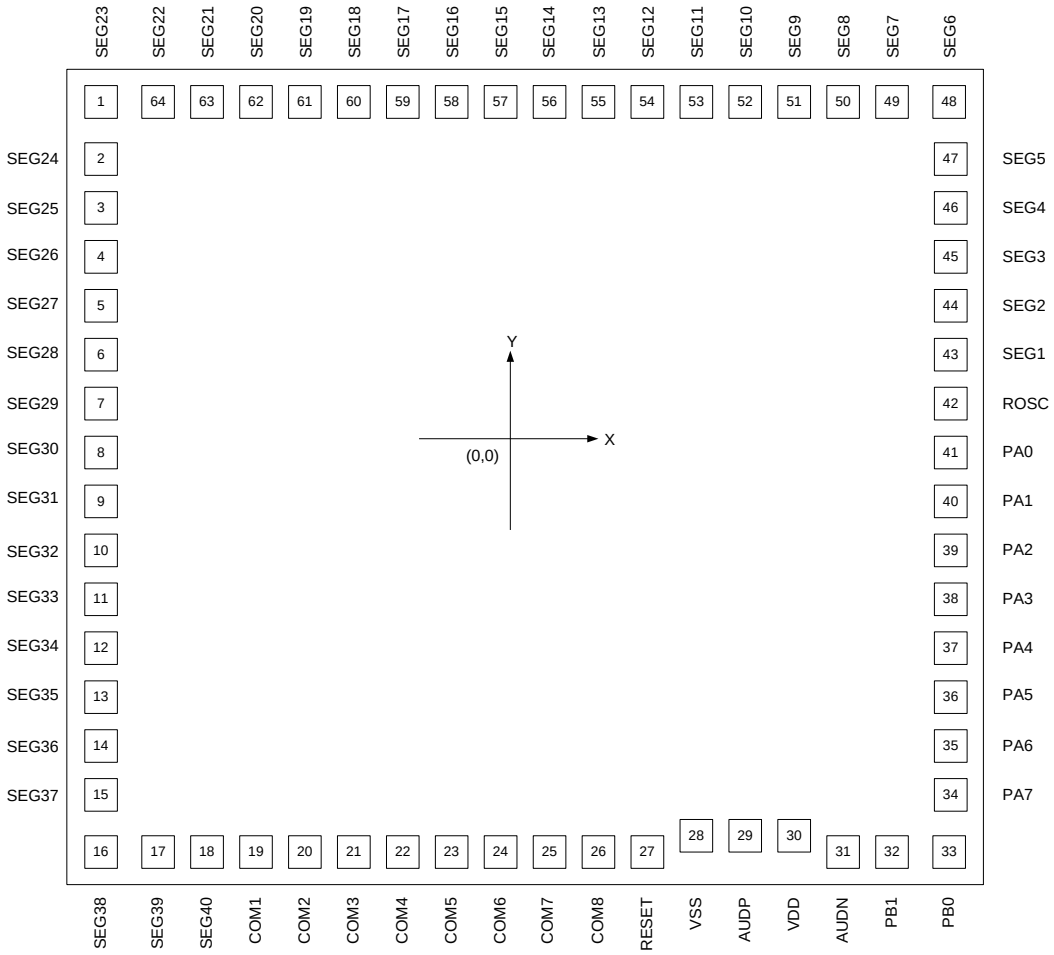


Figure 1: The simplest CKT uses a low impedance speaker. It has high operation current, but the cost is the cheapest.
Figure 2: It is the same as Figure 1 but a high impedance speaker is used.
Figure 3: The CKT contains a low pass filter. It is capable of providing higher speech quality, but it always takes higher operation current.
Figure 4: Improved version of Figure 3. The standby current can be controlled by the enable pin.
Figure 5: The current mirror mode. It is able to control the volume. In addition, it is more stable and has lower operation current than Figure 1-3.
Figure 6: High quality, low operation current CKT, but more expensive.

8. PACKAGE/PAD LOCATIONS

8.1. PAD Assignment



This IC substrate should be connected to VSS

Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.
Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

8.2. Ordering Information

Product Number	Package Type
GPL02E5-NnnV-C	Chip form

Note1: Code number is assigned for customer.
Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

8.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	SEG23	-879.97	782.24	33	PB0	882.52	-779.89
2	SEG24	-879.97	662.19	34	PA7	882.52	-659.82
3	SEG25	-879.97	552.11	35	PA6	882.52	-549.76
4	SEG26	-879.97	451.94	36	PA5	882.52	-449.58
5	SEG27	-879.97	351.78	37	PA4	882.52	-349.42
6	SEG28	-879.97	251.60	38	PA3	882.52	-249.24
7	SEG29	-879.97	151.43	39	PA2	882.52	-149.08
8	SEG30	-879.97	51.27	40	PA1	882.52	-48.91
9	SEG31	-879.97	-48.91	41	PA0	882.52	51.27
10	SEG32	-879.97	-149.08	42	ROSC	882.52	151.43
11	SEG33	-879.97	-249.24	43	SEG1	882.52	251.60
12	SEG34	-879.97	-349.42	44	SEG2	882.52	351.78
13	SEG35	-879.98	-449.58	45	SEG3	882.52	451.94
14	SEG36	-879.97	-549.76	46	SEG4	882.52	552.11
15	SEG37	-879.97	-659.82	47	SEG5	882.52	662.19
16	SEG38	-879.97	-779.88	48	SEG6	882.52	782.24
17	SEG39	-759.91	-779.89	49	SEG7	762.45	782.24
18	SEG40	-649.84	-779.89	50	SEG8	652.38	782.24
19	COM1	-549.60	-779.89	51	SEG9	552.20	782.24
20	COM2	-449.49	-779.89	52	SEG10	452.04	782.24
21	COM3	-349.33	-779.89	53	SEG11	351.86	782.24
22	COM4	-249.16	-779.89	54	SEG12	251.69	782.24
23	COM5	-148.98	-779.89	55	SEG13	151.53	782.24
24	COM6	-48.82	-779.89	56	SEG14	51.35	782.24
25	COM7	51.35	-779.89	57	SEG15	-48.82	782.24
26	COM8	151.53	-779.89	58	SEG16	-148.98	782.24
27	RESET	251.69	-779.89	59	SEG17	-249.16	782.24
28	VSS	351.86	-749.36	60	SEG18	-349.33	782.24
29	AUDP	452.04	-749.36	61	SEG19	-449.49	782.24
30	VDD	552.20	-749.36	62	SEG20	-549.67	782.24
31	AUDN	652.38	-779.89	63	SEG21	-649.84	782.24
32	PB1	762.45	-779.89	64	SEG22	-759.91	782.24

9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
Oct. 19, 2017	1.0	Original	13