DATA SHEET

# GPL081A3

## Low Voltage 7KB LCD Controller

Sep. 28, 2011

Version 1.2

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# LOW VOLTAGE 7KB LCD CONTROLLER

## 1. GENERAL DESCRIPTION

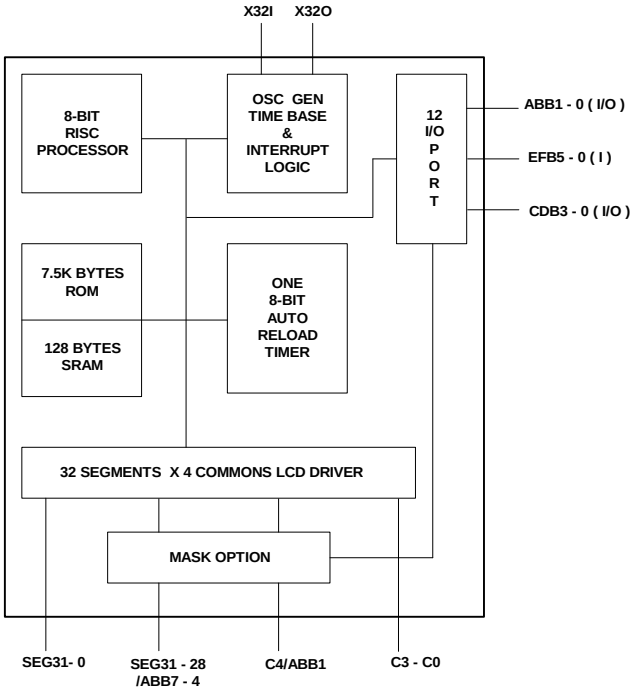
GPL081A3, a special designed CMOS 8-bit microprocessor by Generalplus, offers the best cost/performance ratio in the industry. It combines RAM, ROM, I/Os, an interrupt controller, and an automatic display controller/driver in a small package. One of its extraordinary features is the capability of operating in low voltage range, from 1.2V ~ 1.7V. The Power Down Mode keeps LCD being displayed when CPU is in standby mode, but consumes only less than 3.5μA. Not only GPL081A3 is capable of displaying LCD, but it also can process complex instructions and functions as well. The development team has designed GPL081A3 to cover many application fields such as calculator, watch and other LCD related products required only one battery supply.

## 2. FEATURES

- Built-in 8-bit RISC processor
- 128-byte SRAM
- 7.5K-byte ROM
- CPU frequency: 350KHz or 700KHz (mask option) @ 1.5V (dependent VDD)
- Built-in RC oscillator
- Built-in 32.768KHz oscillator circuit for real clock function
- Watch dog mode (1Hz or 0.5Hz)
- Low operating voltage: 1.2V - 1.7V
- Low standby current, $I_{STBY}$ < 1μA
- LCD matrix: 28 - 32 segments, 4 (or 5) commons
- 12 general I/O pins (segment 29, 30, 31, 32 can be defined as I/O; ABB1 can be optioned to 5$^{th}$ common)
- LCD 1/2, 1/3 bias, 1/2, 1/3, 1/4, 1/5 (mask option) duty
- One 8-bit timer
- 6 interrupt sources (Timer, T16Hz, T2Hz, 128Hz, 2KHz, external interrupt)
- Power down mode (wake-up source: key input, T2Hz, T16Hz, timer)

**Note1:** T16Hz: 32Hz, 16Hz, 8Hz or 4Hz
**Note2:** T2Hz: 2Hz or 1Hz

## 3. BLOCK DIAGRAM

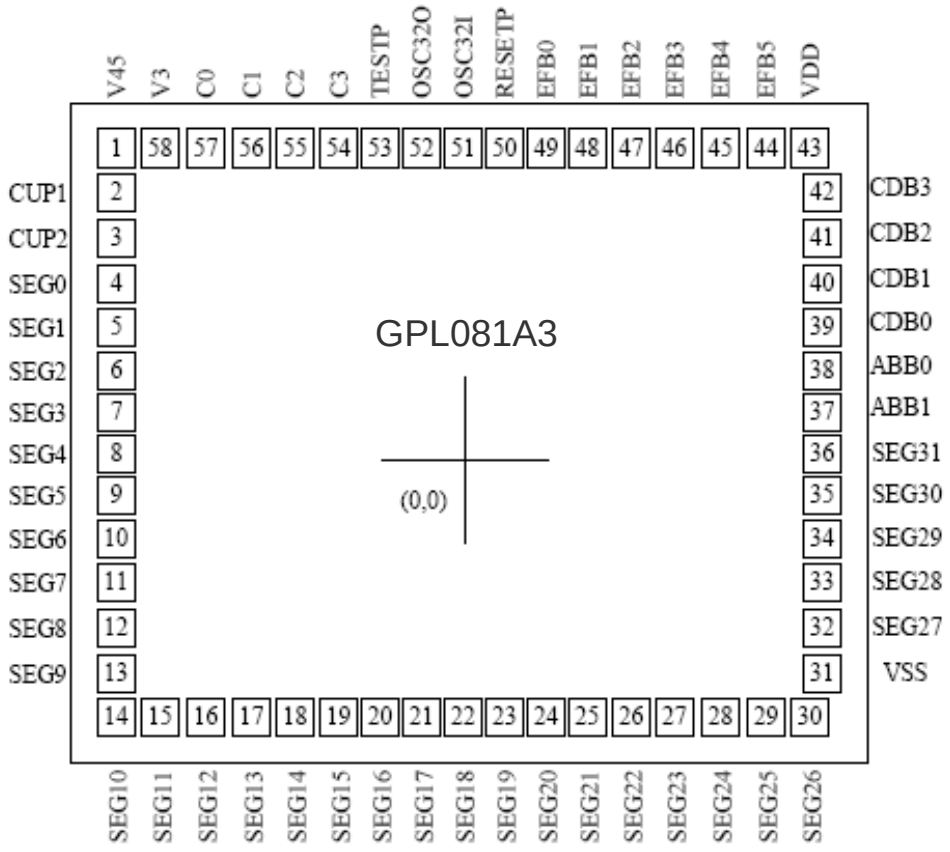



**Note1:** By mask option, SEG31 - 28 can be defined as either segment output or I/O. (SEG31 - 28 or ABB7 - 4)
**Note2:** By mask option, ABB1 can be defined as either I/O or common output (ABB1 or common4)

## 4. SIGNAL DESCRIPTIONS

| Mnemonic | PIN No. | Type | Description |
|---|---|---|---|
| SEG26 - 0<br>SEG31 - 27 | 30 - 4<br>36 - 32 | O | LCD driver segment output. SEG31 - 28 can be mask option for ABB7 - 4. |
| C3 - 0 | 54 - 57 | O | LCD driver common output. |
| ABB1 - 0 | 37 - 38 | I/O | I/O port (ABB1 can be mask option for COM4). |
| EFB5 - 0 | 44 - 49 | I | Input port (also for key wake up input). |
| CDB3 - 0 | 42 - 39 | I/O | I/O port is applicable for sensor. |
| RESET | 50 | I | System reset input. |
| X32I | 51 | I | 32.768KHz crystal input (provide LCD frequency). |
| X32O | 52 | O | 32.768KHz crystal output. |
| TEST | 53 | I | Test input. |
| VDD | 43 | I | Power input. |
| VSS | 31 | I | Ground input. |
| V3<br>V45 | 58<br>1 | I | Inputs for setting LCD bias. |
| CUP1<br>CUP2 | 2<br>3 | I | Inputs for setting LCD bias. |

### 4.1. PAD Assignment




This IC substrate should be connected to VSS

**Note1:** The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

## 5. FUNCTIONAL DESCRIPTIONS

### 5.1. ROM Area

The GPL081A3 provides 7.5K-byte ROM with a LCD driver that is capable of controlling 4(or 5) commons and 32 segments. (Basically, 7K byte of ROM is available for application program and data, 0.5K bytes is allocated for test program.)

### 5.2. Stop Clock Mode

The GPL081A3 provides a power saving mode for those applications required very low stand-by current. Users can simply enable the wake-up sources to stop the CPU clock by writing the STOP CLOCK Register ($09). By doing that, CPU will go to standby mode and the RAM and I/Os remain in their previous states until being woken up. There are three wake-up sources in the GPL081A3, Port EFB wake-up, TIMER wake-up and T2Hz or T16Hz wake-up. After the GPL081A3 is woken up, CPU will go to the next state of Sleep. Wake-up action will not affect RAM and I/Os.

**Note1:** T16Hz: 32Hz, 16Hz, 8Hz or 4Hz
**Note2:** T2Hz: 2Hz or 1Hz

### 5.3. Timer/Counter

The GPL081A3 contains an 8-bit timer. In the timer mode, TMA is a re-loadable up-counter. It will automatically be reloaded with the user's preset value and up-count again.

The clock source is selected as the following:

| Timer/Counter | | Addr. | Clock Source |
|---|---|---|---|
| TMA | 8-BIT TIMER | $0025 | CPU CLOCK (T) or CLK32K (32768Hz or CPU clock / 8) |

### 5.4. LCD Controller

GPL081A3 contains a LCD controller/driver that provides the capability of driving 5 commons and 32 segments LCD. To light the overhead of CPU, a display buffer is designed for mapping to LCD. A LCD dot/pattern is set ON or OFF by programming the corresponding bit of the display buffer. To make the chip more flexible, the pin SEG31, 30, 29, 28, can be selected as I/O pins by mask option. In addition, the LCD bias can be programmed as 1/2 or 1/3. The duty can be selected as 1/2, 1/3, 1/4 or 1/5.

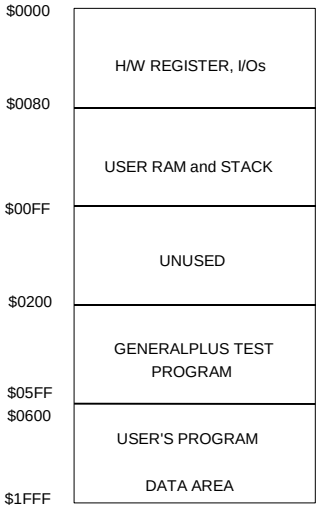
### 5.5. Map of Memory and I/Os

* I/O PORT:
  - PORT ABB $0002
    EFB $0003
    CDB $0005
  - I/O CONFIG $0000
    $0001
    $0006

* NMI SOURCE:
  - INT1 (from TIMER)

*INT SOURCE
  - INT0 (from TIMER)
  - 128 Hz
  - 2 KHz
  - TYHz (32Hz, 16Hz, 8Hz, 4Hz)
  - TXHz (2 Hz or 1Hz)
  - EXTERNAL (CDB1)

*MEMORY MAP



## 6. ELECTRICAL SPECIFICATIONS

### 6.1. Absolute Maximum Ratings

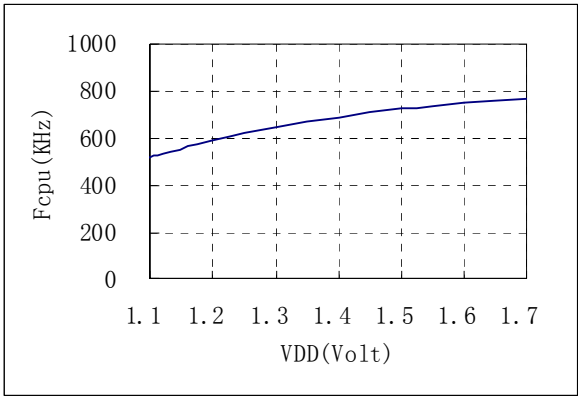
| Characteristics | Symbol | Ratings |
|---|---|---|
| DC Supply Voltage | $V_+$ | < 1.7V |
| Input Voltage Range | $V_{IN}$ | -0.5V to $V_+$ + 0.5V |
| Operating Temperature | $T_A$ | 0℃ to +60℃ |
| Storage Temperature | $T_{STO}$ | -50℃ to +150℃ |

**Note:** Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

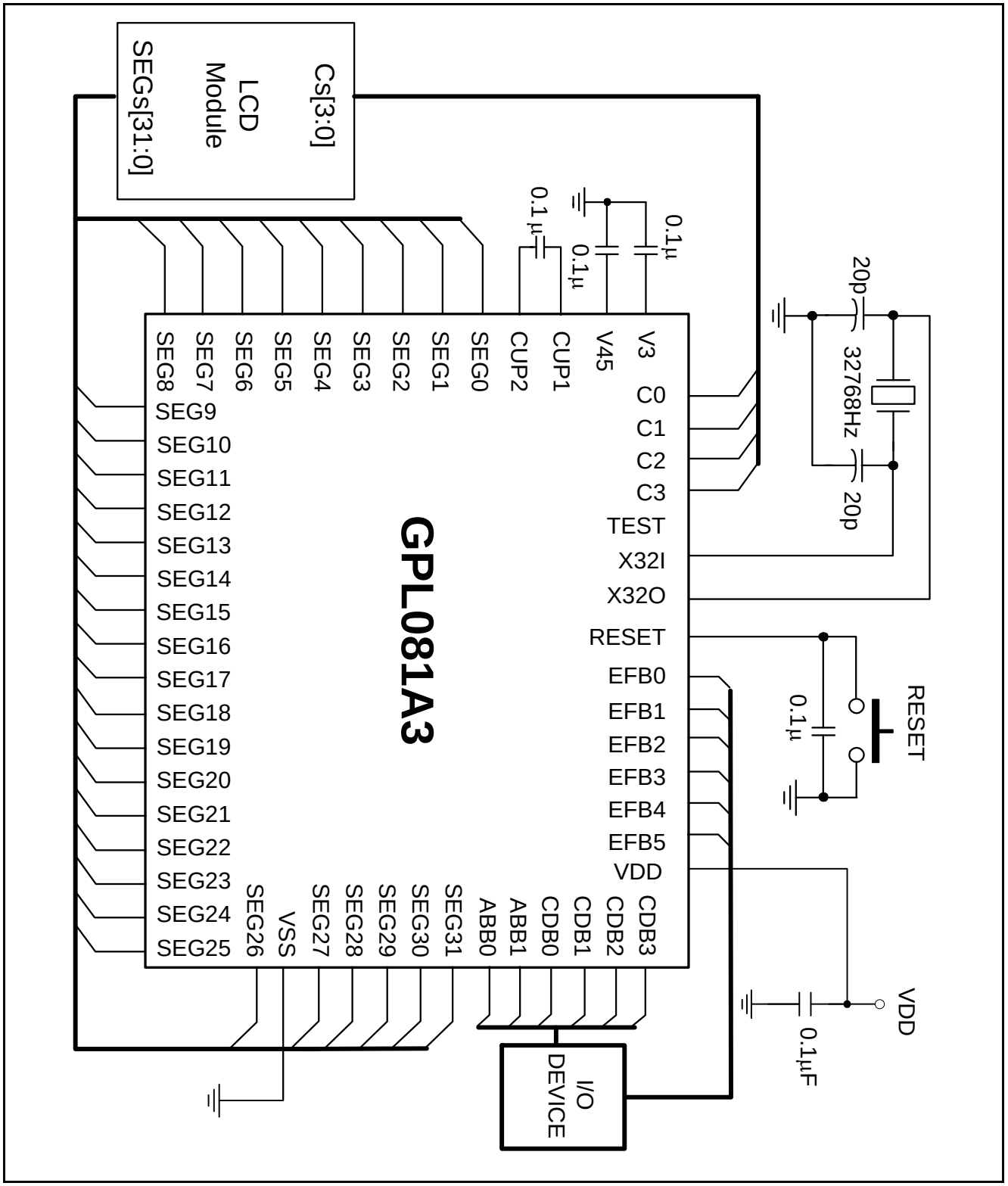
### 6.2. DC Characteristics

| Characteristics | Symbol | Limit | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operating Voltage | VDD | 1.2 | - | 1.7 | V | - |
| Halt Current 1 | $I_{HALT1}$ | - | 3.0 | - | μA | $F_{CPU}$ = 0.35MHz @ 1.5V, no load use 32768Hz crystal |
| Halt Current 2 | $I_{HALT2}$ | - | 16 | - | μA | $F_{CPU}$ = 0.35MHz @ 1.5V, no load no use 32768Hz crystal |
| Operating Current | $I_{OP}$ | - | 35 | - | μA | $F_{CPU}$ = 0.35MHz @ 1.5V, no load |
| Standby Current | $I_{STBY}$ | - | - | 1.0 | μA | VDD = 1.5V, 32768 Hz OFF |
| OSC Frequency | $F_{OSC2}$ | -15% | 0.7<br>1.4 | +15% | MHz | VDD = 1.5V |
| Input High Level | $V_{IH}$ | 1.1 | - | - | V | VDD = 1.5V |
| Input Low Level | $V_{IL}$ | - | - | 0.5 | V | VDD = 1.5V |
| Output High Current (I/O) | $I_{OH}$ | - | -1.0 | - | mA | VDD = 1.5V<br>$V_{OH}$ = 1.0V |
| Output Sink Current (I/O) | $I_{OL}$ | - | 2.5 | - | mA | VDD = 1.5V<br>$V_{OL}$ = 0.5V |
| CPU Clock | $F_{CPU}$ | -15% | 0.35<br>0.7 | +15% | MHz | 0.35, 0.7MHz by code option<br>$F_{CPU}$ = $F_{OSC}$/2 @ 1.5V |

#### 6.2.1. Frequency vs. VDD



## 7. APPLICATION CIRCUIT




**Note:** The 0.1µF capacitor between VDD and VSS should be placed to IC as close as possible.

## 8. PACKAGE/PAD LOCATIONS

### 8.1. Ordering Information

| Product Number | Package Type |
|---|---|
| GPL081A3 - NnnV - C | Chip form |

**Note1:** Code number is assigned for customer.

**Note2:** Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

## 9. DISCLAIMER

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## 10. REVISION HISTORY

| Date | Revision # | Description | Page |
|---|---|---|---|
| SEP. 28, 2011 | 1.2 | Modify the descriptions in section 2 and 6.2. | 7 |
| FEB. 20, 2006 | 1.1 | Modify the descriptions in section 6.2. | 4 |
| NOV. 07, 2005 | 1.0 | Original | 8 |