DATA SHEET

GPL082A

Low Power 7KB LCD Controller

AUG. 28, 2007

Version 1.0

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LOW POWER 7KB LCD CONTROLLER

1. GENERAL DESCRIPTION

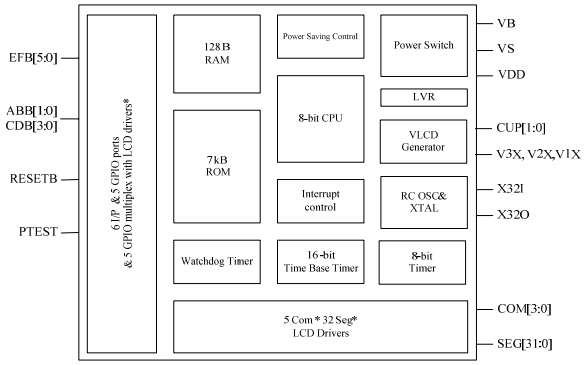
GPL082A, a special designed CMOS 8-bit microprocessor by Generalplus, offers the best cost/performance ratio in the industry. It combines RAM, ROM, I/Os, an interrupt controller, and an automatic display controller/driver in a small device. Its extraordinary features is the capability of operating in low voltage range from 1.2V ~ 1.7V and also operating under low power that is suitable for solar cell environment. It also builds in internal power switch to select two way power sources and facilitates user applying for solar cell and battery co-operation application. This device is capable for many application fields such as low power calculator, watch and other LCD related products required either only one solar cell or battery application, or even two way power source .

2. FEATURES

- Built-in 8-bit high performance processor
- 128-byte SRAM
- 7K-byte ROM
- Built-in 150k/300k/600kHz RC oscillator for system operation (mask option)
- Built-in 32.768KHz oscillator circuit for real clock function
- Watch dog mode (1Hz)
- Low operating voltage: 1.2V – 1.7V
- Low standby current, I_{STBY} < 1μA
- LCD matrix: 28 - 32 segments, 4 (or 5) commons
- 12 general I/O pins (segment 28,29,30,31 can be defined as I/O; ABB1 can be optioned to 5th common)
- LCD 1/2, 1/3 bias, 1/2, 1/3, 1/4, 1/5 (mask option) duty
- One 8-bit timer
- 6 interrupt sources
  (Timer, T16Hz, T2Hz, 128Hz, 2KHz, external interrupt)
- Power down mode
  (wake-up source: key input, T2Hz, T16Hz, timer)
- Build-in power switch for two way power source.
- Build-in VLCD regulator V1X=1.5v

Note1: T16Hz: 32Hz, 16Hz, 8Hz or 4Hz
Note2: T2Hz: 2Hz or 1Hz

3. BLOCK DIAGRAM



Note1: By mask option, SEG[31:28] can be defined as either segment output or I/O. (SEG[31:28] or ABB[7:4])

Note2: By mask option, ABB1 can be defined as either I/O or common output (ABB[1] or COM[4])

4. SIGNAL DESCRIPTIONS

Mnemonic	Type	Description
SEG[27:0] SEG[31:28]	O	LCD driver segment output. SEG[31:28] can be mask option as ABB[7:4].
COM[3:0]	O	LCD driver common output.
ABB[1:0]	I/O	I/O port (ABB[1] can be mask option as COM[4]).
EFB[5:0]	I	Input port (also for key wake up input).
CDB[3:0]	I/O	I/O port.
RESETB	I	System reset input.(low active)
X32I	I	32.768KHz crystal input (provide LCD frequency).
X32O	O	32.768KHz crystal output.
PTEST	I	Test input.
VS	I	Solar cell power input.
VB	I	Battery power input.
VDD	I	Power input.
VSS	I	Ground input.
V1X V2X V3X	I	Inputs for setting LCD bias.
CUP1 CUP2	I	Inputs for setting LCD bias.

5. FUNCTIONAL DESCRIPTIONS

5.1. CPU

The 8-bit microprocessor in GPL082A is a high performance processor equipped with Accumulator, Program Counter, X Register Stack pointer and Processor Status Register (this is the same as the 6502 instruction structure).

5.2. Clock Source

The GPL082A equips with two internal RC Oscillators. One generates high frequency to support the whole system operation. It provides three frequency 150k/300k/600 kHz operation frequencies and can be selected by mask option that rely on user different application. The other one generates low frequency 32768Hz to control LCD frame rate and time base timer. In order to provide a precise timing source for 32768Hz clock, this device also provides 32768Hz crystal oscillator and user can select 32768Hz clock source in either RC oscillator or crystal oscillator by mask option.

5.3. ROM/RAM Area

The GPL082A provides 7K-byte ROM that can be defined as the program area and its address locate from $200 to $3FF and from $600 to $1FFF. Its RAM consists of 128 bytes (including Stack) at locations from $80 through $FF.

5.4. Stop Clock Mode

The GPL082A provides a power saving mode for those applications required very low stand-by current. Users can simply enable the wake-up sources and then to stop the CPU clock by writing the STOP CLOCK Register ($09). By doing that, CPU will go to standby mode and the RAM and I/Os remain in their previous states until being woken up. There are four wake-up sources in the GPL082A, Port EFB wake-up, TIMER wake-up and T2Hz or T16Hz wake-up. After the GPL082A is woken up, CPU will go to the next state of Sleep. Wake-up action will not affect RAM and I/Os.

Note1: T16Hz: 32Hz, 16Hz, 8Hz or 4Hz
Note2: T2Hz: 2Hz or 1Hz

5.5. Timer/Counter

The GPL082A contains an 8-bit timer. In the timer mode, TMA is a re-loadable up-counter. It will automatically be reloaded with the user's preset value and up-count again.

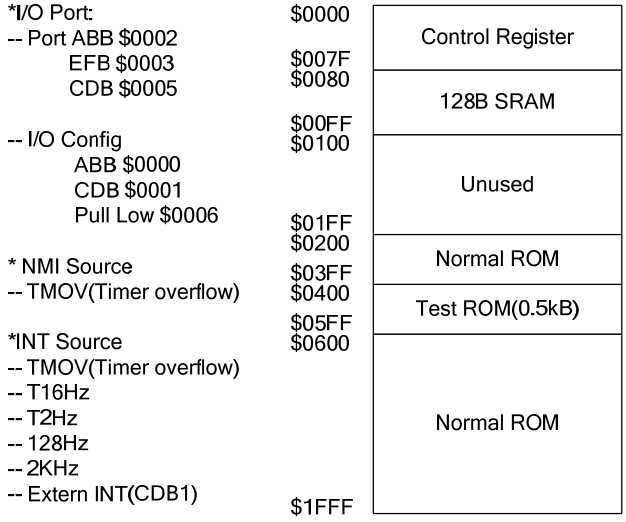
The clock source is selected as the following:

Timer/Counter		Addr.	Clock Source
TMA	8-BIT TIMER	$0025	CPU CLOCK (T) or CLK32K (32768Hz or CPU clock / 8)

5.6. LCD Controller

GPL082A contains a LCD controller/driver that provides the capability of driving 5 commons and 32 segments LCD. To light the overhead of CPU, a display buffer is designed for mapping to LCD. A LCD dot/pattern is set ON or OFF by programming the corresponding bit of the display buffer. To make the chip more flexible, the pin SEG31, 30, 29, 28, can be selected as I/O pins by mask option. In addition, the LCD bias can be programmed as 1/2 or 1/3. The duty can be selected as 1/2, 1/3, 1/4 or 1/5.

5.7. Map of Memory and I/Os



5.8. Control Register

Address	Function	Reset value	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$00	Port AB Ctrl	00h	W	AB7	AB6	AB5	AB4	-	-	AB1	AB0
	(P_00H_PortAB_Ctrl)			Port AB Direction control: 0: IN; 1:OUT							
$01	PortCD Ctrl	00h	W	-	-	CD123S	CD0S	CD3	CD2	CD1	CD0
	(P_01H_PortCD_Ctrl)			$1.[5:4]=Port CD[3:0] sensor enable ; $1.[3:0]=Port CD Direction control: 0: IN; 1:OUT							
$02	Port AB Data	xxh	R	AB7	AB6	AB5	AB4	-	-	AB1	AB0
	(P_02H_PortAB)		W	AB7	AB6	AB5	AB4	-	-	AB1	AB0
$03	Port EF Data (P_03H_PortEF)	xxh	R	-	-	EF5	EF4	EF3	EF2	EF1	EF0
$04	Port EF Latch (P_04H_DataLatch)	xxh	R	Read this port to latch the data of Port EF							
$05	Port CD Data	xxh	R	-	-	-	-	CD3	CD2	CD1	CD0
	(P_05H_PortCD)		W	-	-	-	-	CD3	CD2	CD1	CD0
$06	Pull Low Ctrl	00h	W	-	-	BUZO	EF[5:4]	EF[3:0]	CD[3:0]	AB[7:4]	AB[1:0]
	(P_06H_IOPullLowCtrl)			BUZO:Buzzer output enable;Others is pull low enable control.							
$07	LCD Configuration	20h	W	Duty1	Duty0	Bias	0	-	-	-	ScanEn
	(P_07H_LCDconfig)			Duty[1:0] =0 =>1/5 duty,1=>1/4 duty,2=>1/3 duty,3=>1/2 duty; Bias=0=> 1/2 bias,1=>1/3 bias							
$08	Wakeup Source	00h	W	-	-	-	-	T16Hz	TMOV	T2Hz	EF Key Chang
	(P_08H_SleepWakeup)			T16Hz depends on $A.[1:0], T2Hz depends on $A.7							
$09	Enter Sleep (P_09H_EnterSleep)	xxh	W	Writing any data into $09 to enter sleep mode							
$0A	Timer Selection	xxh	R	0.5Hz	1Hz	2Hz	4Hz	8Hz	16Hz	32Hz	64Hz
		00h	W	T2HzSel	-	-	-	-	-	T16HzSel	
	(P_0AH_TimerXSel)			0: 2Hz 1: 1Hz						00: 4Hz, 01: 8Hz 10:16Hz, 11:32Hz	
$0B	Timer Ctrl	00h	W	TimerEN	-	TMSRC	0	-	-	-	-
	(P_0BH_TimerCtrl)			TMSRC:Timer clock source, 0: CPU clock, 1:CLK32K							
$0C	Crystal Control	00h	W	Xtalenb	wkmode	0	-	-	-	-	-
	(P_0CH_XtalCtrl)			Xtalenb: Crystal enable, low active wkmode: weak mode selection: 0: strong mode,1:weak mode							
$0D	Interrupt Ctrl	00h	R	NMI/IRQ	0	TMOV	TMXINT	2HZINT	128INT	2KINT	EXINT
	(P_0DH_INTCTRL)		W	NMI/IRQ	0	TMOVEN	TMXEN	2HzEN	128EN	2KEN	EXEN
$0F	Clear Watchdog		W	Writing any data into $f to clean watchdog							
$10	LCD RAM(Com0)	xxh	W	C0S7	C0S6	C0S5	C0S4	C0S3	C0S2	C0S1	C0S0
$11	LCD RAM(Com0)	xxh	W	C0S15	C0S14	C0S13	C0S12	C0S11	C0S10	C0S9	C0S8
$12	LCD RAM(Com0)	xxh	W	C0S23	C0S22	C0S21	C0S20	C0S19	C0S18	C0S17	C0S16
$13	LCD RAM(Com0)	xxh	W	C0S31	C0S30	C0S29	C0S28	C0S27	C0S26	C0S25	C0S24
$14	LCD RAM(Com1)	xxh	W	C1S7	C1S6	C1S5	C1S4	C1S3	C1S2	C1S1	C1S0
$15	LCD RAM(Com1)	xxh	W	C1S15	C1S14	C1S13	C1S12	C1S11	C1S10	C1S9	C1S8
$16	LCD RAM(Com1)	xxh	W	C1S23	C1S22	C1S21	C1S20	C1S19	C1S18	C1S17	C1S16
$17	LCD RAM(Com1)	xxh	W	C1S31	C1S30	C1S29	C1S28	C1S27	C1S26	C1S25	C1S24

Address	Function	Reset value	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$18	LCD RAM(Com2)	xxh	W	C2S7	C2S6	C2S5	C2S4	C2S3	C2S2	C2S1	C2S0
$19	LCD RAM(Com2)	xxh	W	C2S15	C2S14	C2S13	C2S12	C2S11	C2S10	C2S9	C2S8
$1A	LCD RAM(Com2)	xxh	W	C2S23	C2S22	C2S21	C2S20	C2S19	C2S18	C2S17	C2S16
$1B	LCD RAM(Com2)	xxh	W	C2S31	C2S30	C2S29	C2S28	C2S27	C2S26	C2S25	C2S24
$1C	LCD RAM(Com3)	xxh	W	C3S7	C3S6	C3S5	C3S4	C3S3	C3S2	C3S1	C3S0
$1D	LCD RAM(Com3)	xxh	W	C3S15	C3S14	C3S13	C3S12	C3S11	C3S10	C3S9	C3S8
$1E	LCD RAM(Com3)	xxh	W	C3S23	C3S22	C3S21	C3S20	C3S19	C3S18	C3S17	C3S16
$1F	LCD RAM(Com3)	xxh	W	C3S31	C3S30	C3S29	C3S28	C3S27	C3S26	C3S25	C3S24
$20	LCD RAM(Com4)	xxh	W	C4S7	C4S6	C4S5	C4S4	C4S3	C4S2	C4S1	C4S0
$21	LCD RAM(Com4)	xxh	W	C4S15	C4S14	C4S13	C4S12	C4S11	C4S10	C4S9	C4S8
$22	LCD RAM(Com4)	xxh	W	C4S23	C4S22	C4S21	C4S20	C4S19	C4S18	C4S17	C4S16
$23	LCD RAM(Com4)	xxh	W	C4S31	C4S30	C4S29	C4S28	C4S27	C4S26	C4S25	C4S24
$25	Timer Data	xxh	R	Read from current Time value							
		xxh	W	Writing into Reload register							
$27	Latch Timer Data	xxh	W	Writing any data into $27 will load Timer reload Data into Timer							
$40	Clear EXTINT	xxh	W	Writing any data into $40 will clear EXTINT							
$41	Cleak 2KINT	xxh	W	Writing any data into $41 will clear 2KINT							
$42	Clear 128INT	xxh	W	Writing any data into $42 will clear 128INT							
$43	Clear 2HZINT	xxh	W	Writing any data into $43 will clear 2HZINT							
$44	Clear TMXINT	xxh	W	Writing any data into $44 will clear TMXINT							
$45	Clear TMOVINT	xxh	W	Writing any data into $45 will clear TMOVINT							

Note: If the bits of the register is not defined, it will not be implemented in the real chip, its readout value should be random. However, it is defined as 0 in this table for simplification.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

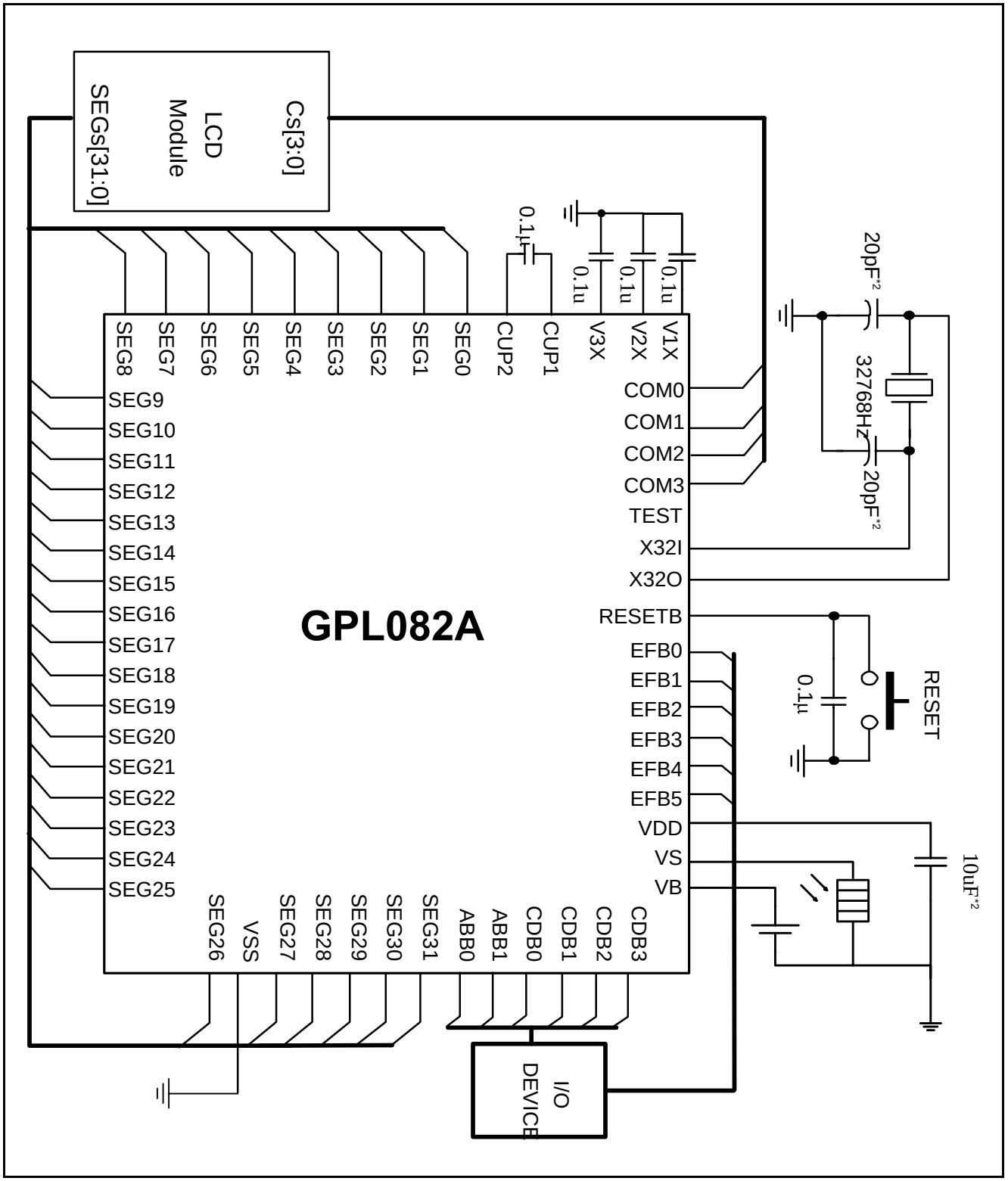
Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	-0.3~5V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	1.2	-	1.7	V	-
Operating Current	I_{OP}	-	-	20	μA	F_{CPU} = 300kHz @ 1.5V, no load
Halt Current	I_{HALT1}	-	-	10	μA	VDD=1.5V, no load
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 1.5V, 32768 Hz OFF
Input High Level	V_{IH}	1.1	-	-	V	VDD = 1.5V
Input Low Level	V_{IL}	-	-	0.5	V	VDD = 1.5V
GPIO Output High Voltage	V_{OH}	-	1.0	-	V	VDD = 1.5V I_{OH} = -1mA
GPIO Output Low Voltage	V_{OL}	-	0.5	-	V	VDD = 1.5V I_{OL} = 2.5mA
Pull low Resistance	R_{PL}	80	160	320	KΩ	VDD = 1.5V
CPU Clock	F_{CPU}	-	150	-	kHz	CPU clock depend on code option
		-	300	-		
		-	600	-		

7. APPLICATION CIRCUIT



Note*1: The 10µF capacitor between VDD and VSS should be placed to IC as close as possible.

Note*2: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GPL082A - NnnV - C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
AUG. 28, 2007	1.0	Release 1.0.	12
NOV. 07, 2006	0.1	Original	12