DATA SHEET

GPL082A1

Low Power 7KB LCD Controller

May 25, 2015

Version 1.0

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LOW POWER 7KB LCD CONTROLLER

1. GENERAL DESCRIPTION

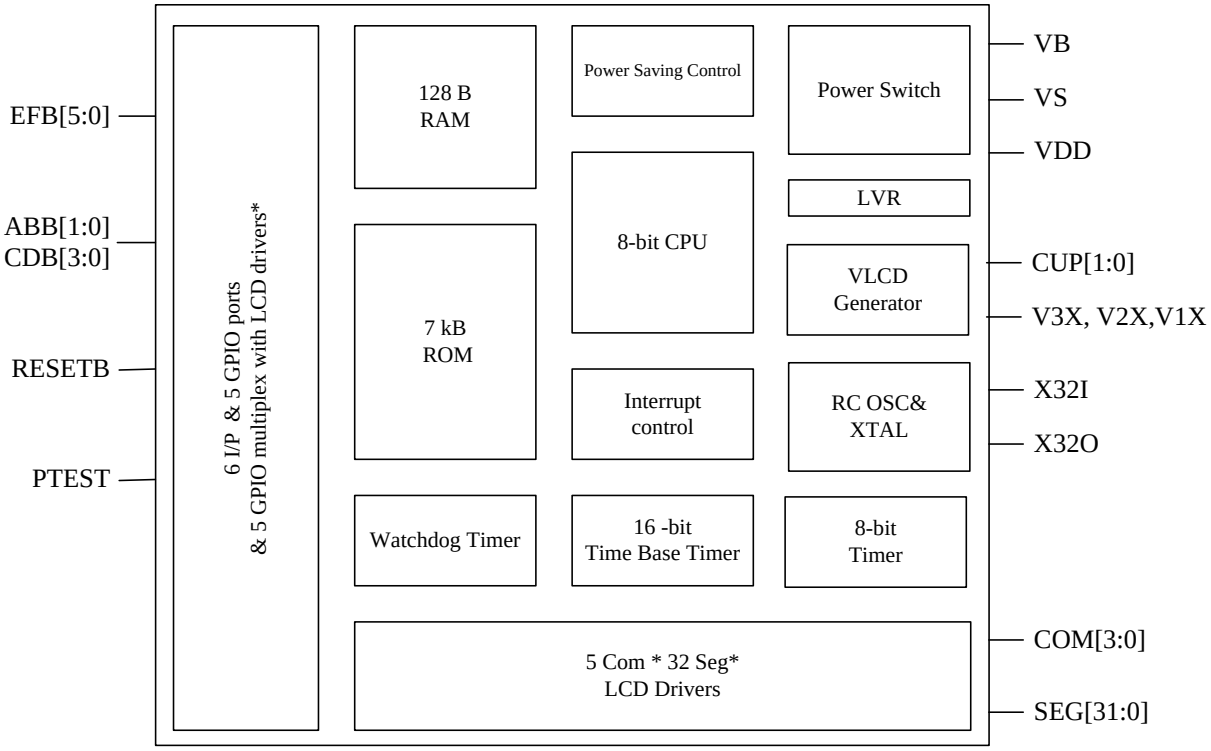
GPL082A1, a CMOS 8-bit microprocessor by Generalplus, is equipped with RAM, ROM, I/Os, an interrupt controller, and an automatic display controller/driver in a small device. Its extraordinary features is the capability of operating in low voltage range from 1.2V ~ 1.7V and also operating under low power that is suitable for solar cell environment. It also has an internal power switch to select two-way power sources and facilitates applying for solar cell and battery co-operation application. This device is applicable for many application fields such as low power calculator, watch and other LCD relevant products requiring either only one solar cell or battery application, or even two-way power source .

2. FEATURES

- Built-in 8-bit high performance processor
- 128-byte SRAM
- 7K-byte ROM
- Built-in 150k/300k/600kHz RC oscillator for system operation (mask option)
- Built-in 32.768KHz oscillator circuit for real clock function
- Watchdog mode (1Hz)
- Low operating voltage: 1.2V – 1.7V
- Low standby current, I_{STBY} < 1μA
- LCD matrix: 28 - 32 segments, 4 (or 5) commons
- 12 general I/O pins (segment 28,29,30,31 can be defined as I/O; ABB1 can be optioned to 5th common)
- LCD 1/2, 1/3 bias, 1/2, 1/3, 1/4, 1/5 (mask option) duty
- One 8-bit timer
- 6 interrupt sources
  (Timer, T16Hz, T2Hz, 128Hz, 2KHz, external interrupt)
- Power down mode
  (wake-up source: key input, T2Hz, T16Hz, timer)
- Built-in power switch for two way power source.
- Built-in VLCD regulator V1X=1.5v

Note1: T16Hz: 32Hz, 16Hz, 8Hz or 4Hz
Note2: T2Hz: 2Hz or 1Hz

3. BLOCK DIAGRAM



Note1: By mask option, SEG[31:28] can be defined as either segment output or I/O. (SEG[31:28] or ABB[7:4])
Note2: By mask option, ABB1 can be defined as either I/O or common output (ABB[1] or COM[4])

4. SIGNAL DESCRIPTIONS

Mnemonic	Type	Description
SEG[27:0] SEG[31:28]	O	LCD driver segment output. SEG[31:28] can be mask option as ABB[7:4].
COM[3:0]	O	LCD driver common output.
ABB[1:0]	I/O	I/O port (ABB[1] can be mask option as COM[4]).
EFB[5:0]	I	Input port (also for key wake up input).
CDB[3:0]	I/O	I/O port.
RESETB	I	System reset input.(low active)
X32I	I	32.768KHz crystal input (provide LCD frequency).
X32O	O	32.768KHz crystal output.
PTEST	I	Test input.
VS	I	Solar cell power input.
VB	I	Battery power input.
VDD	I	Power input.
VSS	I	Ground input.
V1X V2X V3X	I	Inputs for setting LCD bias.
CUP1 CUP2	I	Inputs for setting LCD bias.

5. FUNCTIONAL DESCRIPTIONS

5.1. CPU

The 8-bit microprocessor in GPL082A1 is a high performance processor equipped with Accumulator, Program Counter, X Register Stack pointer and Processor Status Register (this is the same as the 6502 instruction structure).

5.2. Clock Source

The GPL082A1 is equipped with two internal RC Oscillators. One generates high frequency to support the entire system operation, providing frequency options, 150k/300k/600KHz, and can be selected by mask option based on user's demand. The other generates low frequency 32768Hz to control LCD frame rate and time base timer. In order to provide a precise timing source for 32768Hz clock, this device also provides 32768Hz crystal oscillator and user can select 32768Hz clock source in either RC oscillator or crystal oscillator by mask option.

5.3. ROM/RAM Area

The GPL082A1 provides 7K-byte ROM that can be defined as the program area and its address locate from $200 to $3FF and from $600 to $1FFF. Its RAM consists of 128 bytes (including Stack) at locations from $80 through $FF.

5.4. Stop Clock Mode

The GPL082A1 provides a power saving mode for those applications required very low stand-by current. Users can simply enable the wakeup sources and then stop the CPU clock by writing the STOP CLOCK Register ($09). By doing that, CPU will go to standby mode and the RAM and I/Os retain at their previous states until wakeup. There are four wakeup sources in the GPL082A1: Port EFB wake-up, TIMER wake-up, T2Hz, and T16Hz wake-up. After the GPL082A1 wakes up, CPU will go to the next state of Sleep. Wake-up action will not affect RAM and I/Os.

Note1: T16Hz: 32Hz, 16Hz, 8Hz or 4Hz
Note2: T2Hz: 2Hz or 1Hz

5.5. Timer/Counter

The GPL082A1 contains an 8-bit timer. In the timer mode, TMA is a re-loadable up-counter. It will automatically be reloaded with the user's preset value and up-count again.

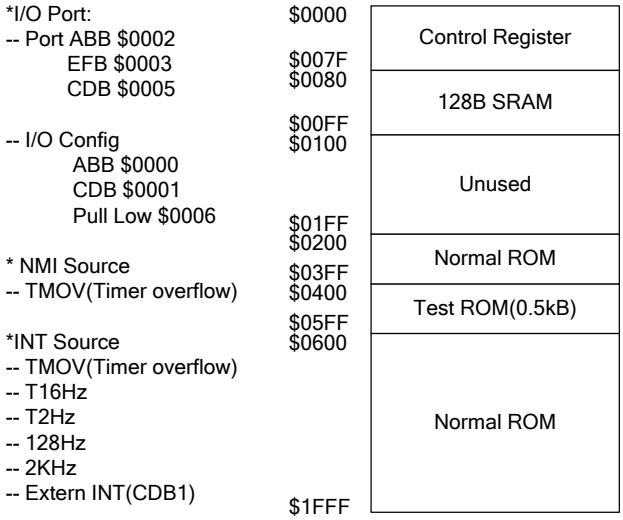
The clock source is selected as the following:

Timer/Counter		Addr.	Clock Source
TMA	8-BIT TIMER	$0025	CPU CLOCK (T) or CLK32K (32768Hz or CPU clock / 8)

5.6. LCD Controller

GPL082A1 contains a LCD controller/driver that provides the capability of driving 5 commons and 32 segments LCD. To light the overhead of CPU, a display buffer is designed for mapping to LCD. A LCD dot/pattern is set ON or OFF by programming the corresponding bit of the display buffer. To make the chip more flexible, the pin SEG31, 30, 29, 28, can be selected as I/O pins by mask option. In addition, the LCD bias can be programmed as 1/2 or 1/3. The duty can be selected as 1/2, 1/3, 1/4 or 1/5.

5.7. Map of Memory and I/Os



6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

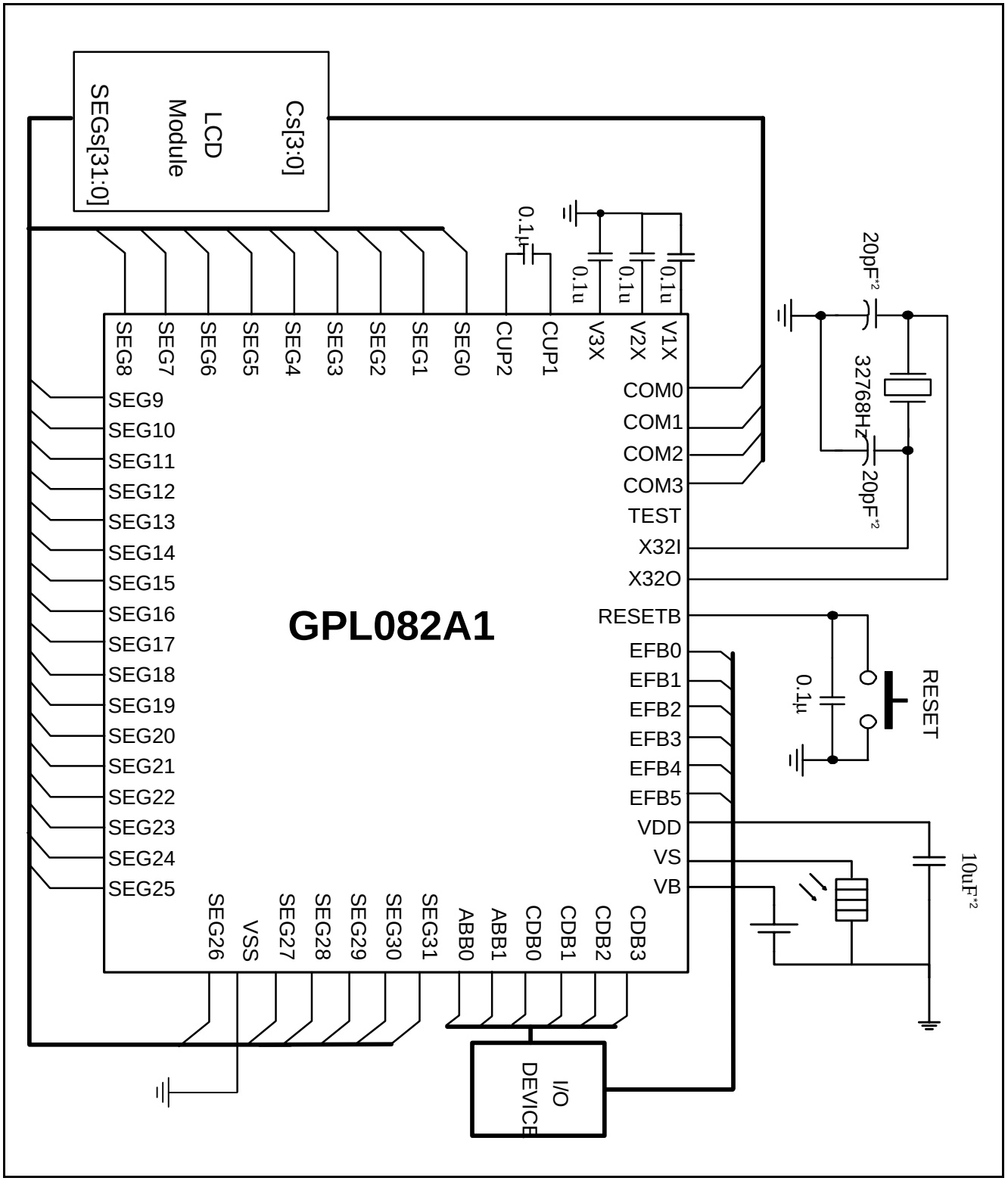
Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	-0.3~5V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics(TA=25˚C)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	1.2	-	1.7	V	-
Operating Current	I_{OP}	-	-	20	μA	F_{CPU} = 300kHz @ 1.5V, no load
Halt Current	I_{HALT1}	-	-	10	μA	VDD=1.5V, no load
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 1.5V, 32768 Hz OFF
Input High Level	V_{IH}	1.1	-	-	V	VDD = 1.5V
Input Low Level	V_{IL}	-	-	0.5	V	VDD = 1.5V
GPIO Output High Voltage	V_{OH}	-	1.0	-	V	VDD = 1.5V I_{OH} = -1mA
GPIO Output Low Voltage	V_{OL}	-	0.5	-	V	VDD = 1.5V I_{OL} = 2.5mA
Pull low Resistance	R_{PL}	80	160	320	KΩ	VDD = 1.5V
CPU Clock	F_{CPU}	-	150	-	kHz	CPU clock depend on code option
		-	300	-		
		-	600	-		

7. APPLICATION CIRCUIT



Note*1: The 10µF capacitor between VDD and VSS should be placed to IC as close as possible.

Note*2: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GPL082A1 - NnnV - C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

9. DISCLAIMER

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10. REVISION HISTORY

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