DATA SHEET

GPL083B1

24KB Low Power LCD Controller

Aug. 26, 2015

Version 1.0

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24KB LOW POWER LCD CONTROLLER

1. GENERAL DESCRIPTION

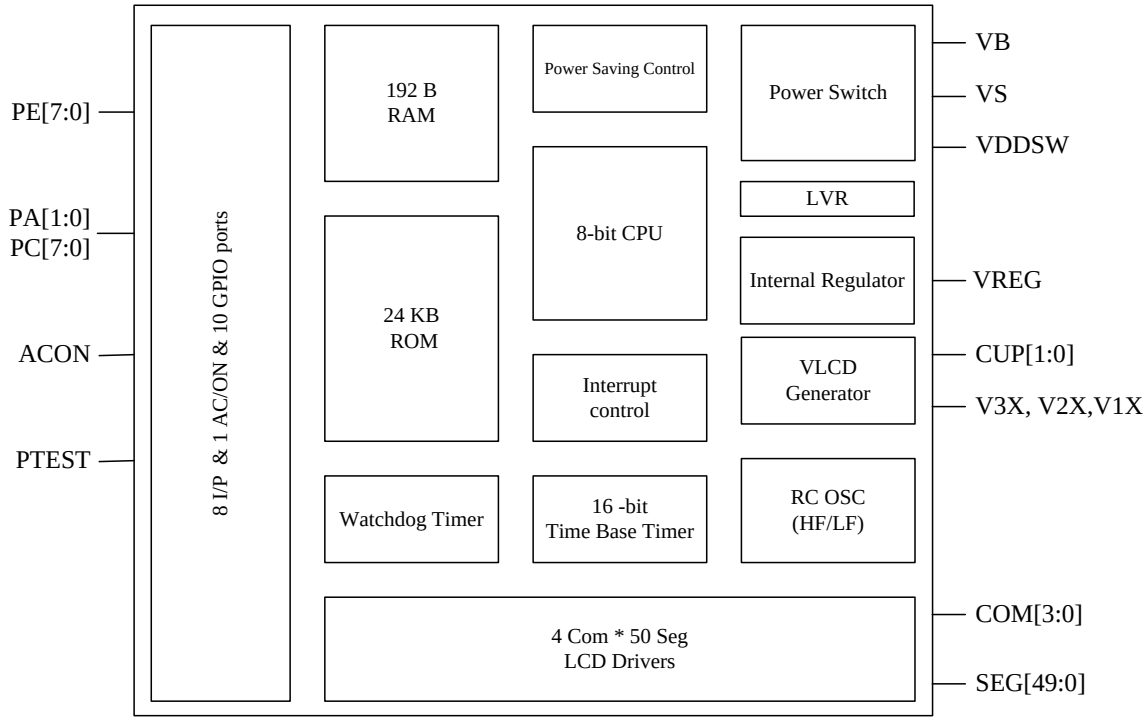
GPL083B1, a special designed CMOS 8-bit microprocessor by Generalplus, offers the best cost/performance ratio in the industry. It combines RAM, ROM, I/Os, an interrupt controller, and an automatic display controller/driver in a small device. Its extraordinary features include the capability of operating in low voltage range from 1.15V ~ 3.6V and also operating under low power that is suitable for solar cell environment. It also provides built-in internal power switch to select two-way power sources automatically and facilitates user applying for solar cell and battery cooperation application. This device is suitable for many application fields such as low power calculator and other LCD related products requiring either only one solar cell or battery application, or even two-way power source.

2. FEATURES

- Built-in 8-bit high performance processor
- 192-byte SRAM
- 24K-byte ROM
- Built-in 225k/1800KHz RC oscillator for system operation
- Built-in 30.72kHz oscillator circuit for timebase
- Low Operating Voltage: 1.15 V – 3.6 V
- Low Standby Current, I_{STBY} < 1uA @3.6V@25℃
- Ten general I/O pins and eight pure input pins
- LCD Matrix: fifty segments, four commons
- LCD 1/2, 1/3 bias, 1/2, 1/3, 1/4 duty
- One 16-bit time base timer
- Watchdog mode (~2 sec)
- Four interrupt sources
  (T16Hz, T2Hz, 128Hz, 2KHz)
- Power Down Mode
  (wakeup source: key input, T2Hz, T16Hz,T128Hz)
- Built-in power switch for two-way power source
- Built-in internal regulator at 1.5V for LCD operation
- Built-in internal regulator for system operation
- Built-in Low voltage reset to prevent system turned down at low voltage condition.

Note1: T16Hz: 32Hz, 16Hz, 8Hz or 4Hz
Note2: T2Hz: 2Hz or 1Hz

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

Mnemonic	Type	Description
SEG[49:0]	O	LCD driver segment output.
COM[3:0]	O	LCD driver common output.
PA[1:0]	I/O	GPIO I/O port.
PC[7:0]	I/O	GPIO I/O port.
PE[7:0]	I	Input port. (also for key wake up input)
ACON	I	Clear or system power on pin (active low) and 4ms de-bounce circuit inside.
PTEST	I	Test mode input pin. (active high)
VS	I	Solar cell power input.
VB	I	Battery power input.
VDDSW	O	Power switch output.
VREG	O	Internal regulator output.
VSS	I	Ground input.
V1X V2X V3X	O	VLCD generator output.
CUP1 CUP2	I	Inputs for setting LCD bias.

5. FUNCTIONAL DESCRIPTIONS

5.1. CPU

The 8-bit microprocessor in GPL083B1 is a high performance processor equipped with Accumulator, Program Counter, X Register, Y Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure).

5.2. Clock Source

The GPL083B1 equips with two internal RC oscillators. One generates high frequency to support the whole system operation. It provides three frequency options: the 225KHz and 1800kHz can be selected by mask options according to various applications. The other one generates low frequency 30.72KHz to control LCD frame rate and time base timer.

5.3. ROM/RAM Area

The GPL083B1 provides 24K-byte ROM that can be defined as the program area where address locates from $9800 to $FFFF. Its RAM consists of 192 bytes (including Stack) at locations from $60 through $11F and $160 to $1FF. The address range from $160 to $1FF is mapping to the same address area from $60 to $FF.

5.4. Stop Clock Mode

The GPL083B1 provides a power saving mode for those applications requiring very low stand-by current. Users can simply enable the wake-up sources and stop the CPU clock by writing the STOP CLOCK Register ($09). Therefore, CPU will enter standby mode, and RAM and I/Os will keep retaining at their previous states until being awakened. There are four wakeup sources in the GPL083B1 - Port PE wake-up, T2Hz, T16Hz or T128Hz wake-up. After the GPL083B1 wakes up, CPU will go to the next state of Sleep. Wake-up action will not affect RAM and I/Os.

Note1: T16Hz: 32Hz, 16Hz, 8Hz or 4Hz

Note2: T2Hz: 2Hz or 1Hz

5.5. I/O Ports

The GPL083B1 has three I/O ports: Port A, Port C, and Port E. These port pins are all equipped with special features for key board scan. In general, when in initial reset state, all ports are used as a general purpose input port. Port A and Port C contain three major parts: data, direction and attribution registers. Port E is only for input and contains two parts: data and attribution registers. Programmer should follow the following table to set each I/O function with corresponding bits in each port.

Port A[1:0], C[7:0]

Attribution	Direction	Data	Function	Description
0	0	0	Input with pull-low	General Purpose I/O function
0	0	1	Pure Input	
0	1	0	Output Low	
0	1	1	Output High	
1	1	0	Pad Floating	Special function

Port E[7:0]

Attribution	Data	Function	Description
0	0	Input with pull-low	General Purpose I/O function
0	1	Pure Input	

5.6. LCD Controller

GPL083B1 contains a LCD controller/driver that provides the capability to drive four commons and fifty segments LCD. To light the CPU overhead, a display buffer is designed for mapping LCD. A LCD dot/pattern is set ON or OFF by programming the corresponding bits of the display buffer. In addition, the LCD bias can be programmed as 1/2 or 1/3. The duty can be selected as 1/2, 1/3, 1/4. In spite of the duty selection, its frame rate is always set at 80Hz.

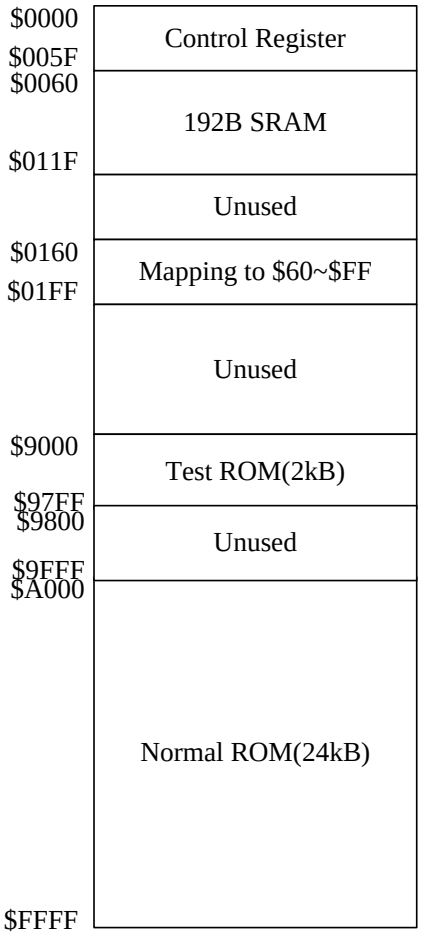
5.7. Auxiliary Calculation Hardware

GPL083B1 contains auxiliary calculation hardware. This hardware allows some nibble operation to accomplish only at one store and load instruction. The original data content should be stored at the register ($50, $51) firstly, and then many decimal operation such as x10/10 or nibble swap, can be acquired by executing read instruction at the corresponding registers ($52~5D). It speeds up many decimal operations that originally need many instructions for one operation.

5.8. Analog Block

In addition to LCD controller and clock source, GPL083B1 also provides many low power and useful analog blocks. The built-in power switch to change the power source automatically between battery and solar cell source and is helpful for two-way source that is a common solution for many low power systems. Either 1.2V or 1.5V internal regulator by code option provides whole system operation at low current environment. Internal low voltage reset analog block prevents the system from uncontrolled at the voltage lower than the operation range.

5.9. Map of Memory



6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	-0.3~5 V
Input Voltage Range	V_{IN}	-0.3V to V_+ + 0.3V
Operating Temperature	T_{OPR}	-20℃ to +70℃
Storage Temperature	T_{STG}	-40℃ to +125℃
Input Current	I_{IN}	1mA
Output Current	I_{OUT}	1mA

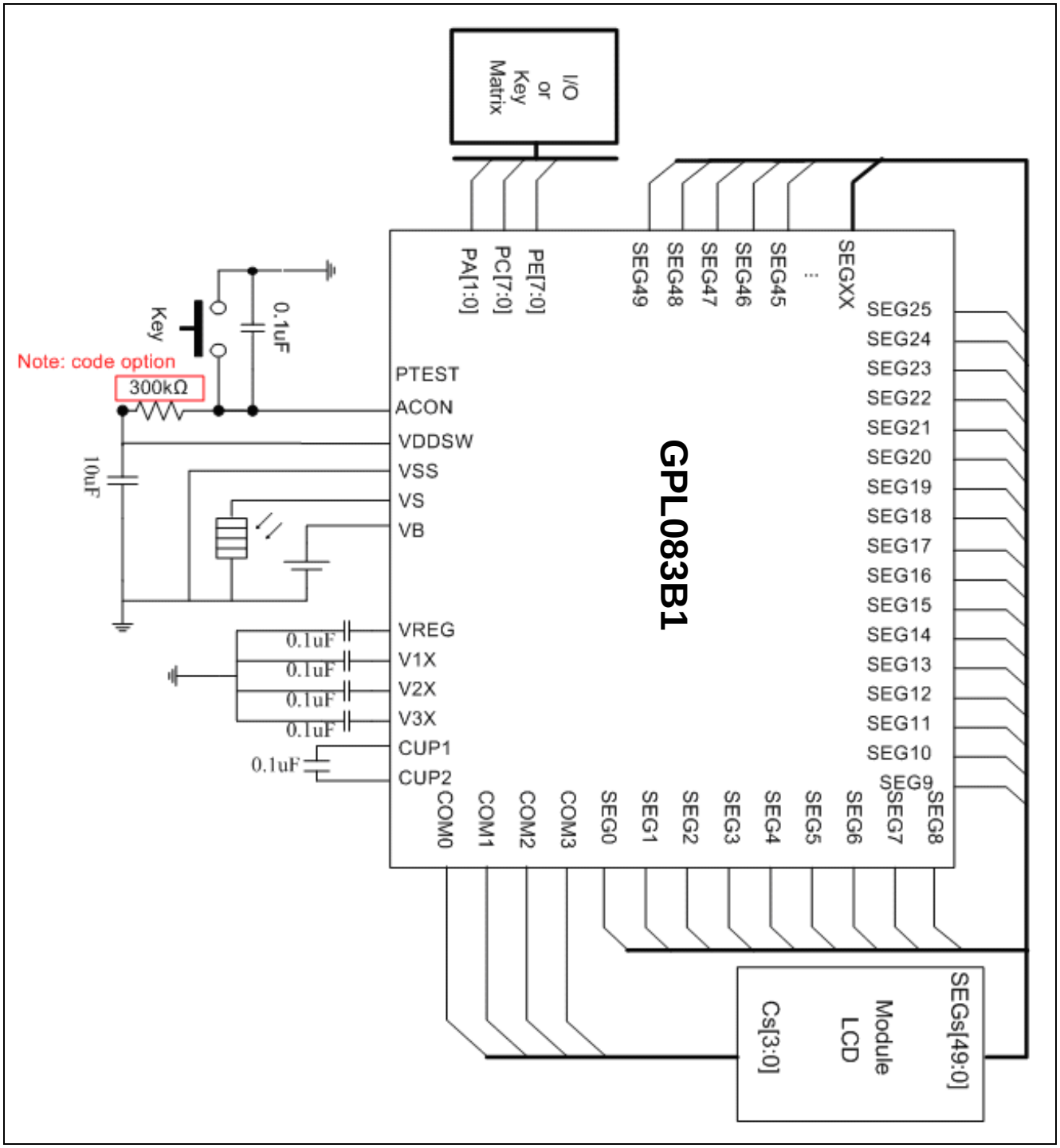
Note: Stresses beyond those given in the Absolute Maximum Rating table may permanent damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

6.2. DC Characteristics

Characteristics	Symbol	Limit			Unit	Terminal	Test Condition
		Min.	Typ.	Max.			
Operating Voltage	VCC	1.15	-	3.6	V	VDD	
Hysteresis Voltage of Power Switch	V_{HS}	0.09	0.1	0.13	V	VB, VS	
Internal Regulator Output for Logic	VREG	-	1.2	-	V	VREG	Clock select as 225kHz
		-	1.5	-	V	VREG	Clock select as 1.8MHz
Input High Level	V_{IH}	VREG*0.7	-	VREG	V	PA, PC, PE	
Input Low Level	V_{IL}	-	-	VREG*0.3	V	PA, PC, PE	
High Level Output Voltage	V_{OH}	VREG*0.7	-	VREG	V	PA, PC	I_{OH}=210uA, VREG=1.2V
Low Level Output Voltage	V_{OL}	-	-	VREG*0.3	V	PA, PC	I_{OL}=500uA, VREG=1.2V
LCD Bias Voltage	V_{L1}	-	1.5	-	V	V1X	@25℃
	V_{L2}	-	3	-	V	V2X	@25℃
	V_{L3}	-	4.5	-	V	V3X	@25℃
Pull low Resistance	R_{PL}	80	160	320	KΩ	PA, PC, PE	VDD=1.2~3.6V
High Frequency	F_H	-	225	-	kHz		Clock select as 225kHz
		-	1800	-	kHz		Clock select as 1800kHz
Low Frequency	F_L	-	30.72	-	kHz		
Operating Current	I_{OP}	-	-	20	μA		High Frequency =225kHz, CPU on, LCD on, no load (VDD=3.6V)
		-	-	180	μA		High Frequency =1800kHz, CPU on, LCD on, no load (VDD=3.6V)
Halt Current	I_{HALT}	-	-	5	μA		Low Frequency active, CPU off, LCD on, no load(VDD=3.6V)
Standby Current	I_{STBY}	-	-	1.0	μA		Clock is stopped, LCD off(VDD=3.6V) @25℃

Note: The input voltage of PA, PC, PE cannot be larger than VREG; otherwise, it will affect the regulator voltage.

7. APPLICATION CIRCUITS



Note : The 300kΩ is possible to be removed, if the internal resistor is enable by code option.

8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GPL083B1 - NnnV - C	Chip form

Note1: Code number (NnnV) is assigned for customer.

Note2: Code number (N = A-Z or 0-9, nn=00-99); version (V = A - Z)

9. DISCLAIMER

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10. REVISION HISTORY

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