DATA SHEET

GPL084A

336-dot Low Power LCD Controller with 24KB ROM

May 11, 2010

Version 1.0

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336-DOT LOW POWER LCD CONTROLLER WITH 24KB ROM

1. GENERAL DESCRIPTION

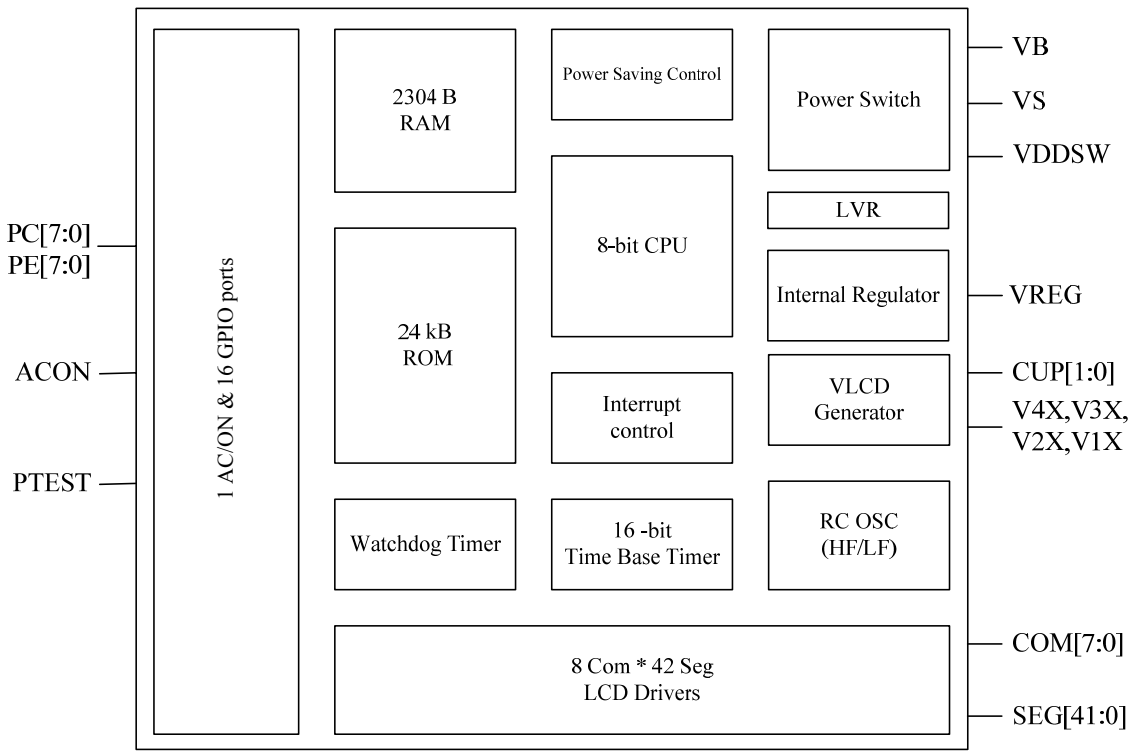
GPL084A, a special designed CMOS 8-bit microprocessor by Generalplus, equips RAM, ROM, I/Os, an interrupt controller, and an automatic display controller/driver in a small device. Its extraordinary features is the capability of operating in low voltage range from 1.1V ~ 3.6V and also operating under low power that is suitable for solar cell environment. It also builds in internal power switch to select two way power sources automatically and facilitates user applying for solar cell and battery co-operation application. This device is suitable for many application fields such as low power calculator and other LCD related products required either only one solar cell or battery application, or even two way power source.

2. FEATURES

- Built-in 8-bit high performance processor
- 2304-byte SRAM
- 24K-byte ROM
- Built-in 225k/1800kHz RC oscillator for system operation
- Built-in 30.72kHz RC oscillator circuit for timebase.
- Low operating voltage: 1.1 V – 3.6 V
- Low standby current, I_{STBY} < 1uA @3.6V@25℃
- 16 general I/O pins.
- LCD configurations: 42*8(336 dots), 44*6(264 dots), 45*5(225 dots), 46*4(184 dots)
- LCD 1/3 ,1/4bias, 1/4, 1/5, 1/6, 1/8 duty
- One 16-bit time base timer
- Watchdog mode (~2 sec)
- 4 interrupt sources
  (TMBB, TMBA, 128Hz, 2KHz)
- Power down mode
  (wake-up source: key input, TMBA, TMBB,T128Hz)
- Built_in power switch for two way power source
- Built_in internal regulator for LCD operation
- Built_in internal regulator for system operation
- Built_in Low voltage reset to avoid system runaway at low voltage

Note1: TMBB: 32Hz, 16Hz, 8Hz or 4Hz
Note2: TMBA: 2Hz or 1Hz

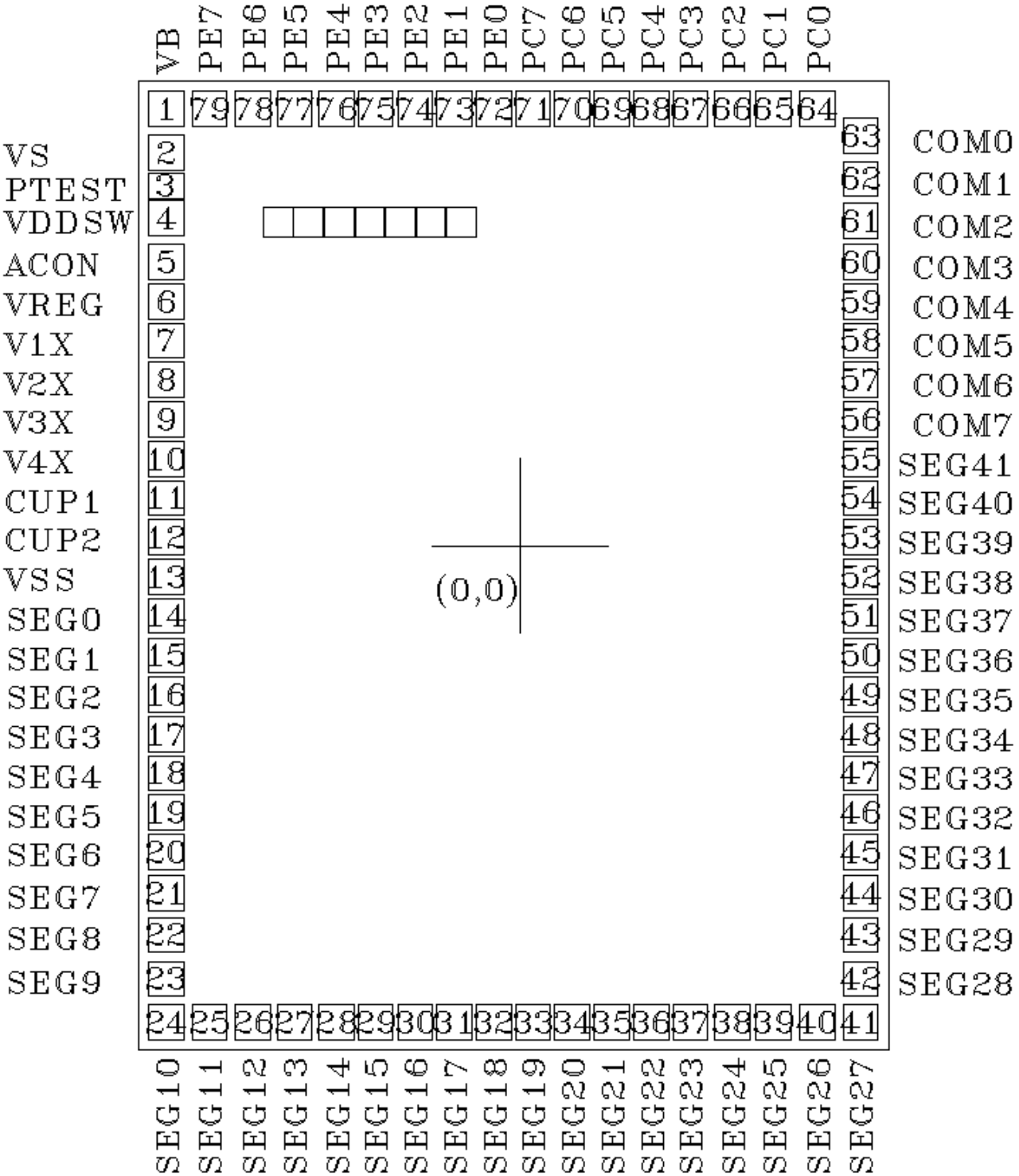
3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

Mnemonic	Type	Description
SEG[41:0]	O	LCD driver segment output.
COM[7:0]	O	LCD driver common output. (COM[7:4] can be option to SEG[42:46] by LCD control register)
PC[7:0]	I/O	GPIO I/O port.
PE[7:0]	I/O	GPIO I/O port.
ACON	I	Clear or system power on pin (active low) and 4ms debounce ckt inside.
PTEST	I	Test mode input pin. (active high)
VS	I	Solar cell power input.
VB	I	Battery power input.
VDDSW	O	Power switch output.
VREG	O	Internal regulator output.
VSS	I	Ground input.
V1X V2X V3X V4X	O	VLCD generator output.
CUP1 CUP2	I	Inputs for setting LCD bias.

4.1. PAD Assignment



5. FUNCTIONAL DESCRIPTIONS

5.1. CPU

The 8-bit microprocessor in GPL084A is a high performance processor equipped with Accumulator, Program Counter, X Register, Y Register, Stack pointer and Processor Status Register (this is the same as the CPU-6502 instruction structure).

5.2. Clock Source

The GPL084A equips with two internal RC Oscillators. One generates high frequency to support the whole system operation. It provides two frequency 225k/1800kHz operating frequency and can be selected by mask option that rely on user different application. The other one generate low frequency 30.72kHz to control LCD frame rate and time base timer.

5.3. ROM/RAM Area

The GPL084A provides 24K-byte ROM that can be defined as the program area and its address located from $A000 to $FFFF. Its RAM consists of 2304 bytes (including Stack) at location from $60 through $95F.

5.4. Stop Clock Mode

The GPL084A provides a power saving mode for those applications required very low stand-by current. Users can simply enable the wake-up sources to stop the CPU clock by writing the STOP CLOCK Register ($09). By doing that, CPU will go to standby mode and the RAM and I/Os remain in their previous states until being woken up. There are four wake-up sources in the GPL084A, Port PortE wake-up, TMBA, TMBB or T128Hz wake-up. After the GPL084A is woken up, CPU will go to the next state of Sleep. Wake-up action will not affect RAM and I/Os.

Note1: TMBB: 32Hz, 16Hz, 8Hz or 4Hz
Note2: TMBA: 2Hz or 1Hz

5.5. I/O Ports

The GPL084A has two ports, PortC, PortE. These port pins all equip with special features for key board scan. In general, when an initial reset start, all ports are used as a general purpose input port. PortC and PortE contain three parts: data, direction and attribution registers. Programmer should follow below table to set each I/O function with corresponding bit in each ports.

PortC[7:0], PortE[7:0]

Attribution	Direction	Data	Function	Description
0	0	0	Input with pull-low	General Purpose I/O function
0	0	1	Pure Input	
0	1	0	Output Low	
0	1	1	Output High	

5.6. LCD Controller

GPL084A contains a LCD controller/driver that provides the capability of driving 8 commons and 42 segments LCD. To light the overhead of CPU, a display buffer is designed for mapping to LCD. A LCD dot/pattern is set ON or OFF by programming the corresponding bit of the display buffer. In addition, the LCD bias can be programmed as 1/3 or 1/4. The duty can be selected as 1/4, 1/5, 1/6 or 1/8. The frame rate is set to 77Hz at 1/5 duty. When the 1/4, /1/6 or 1/8 duty selected, its frame rate is set to 80Hz.

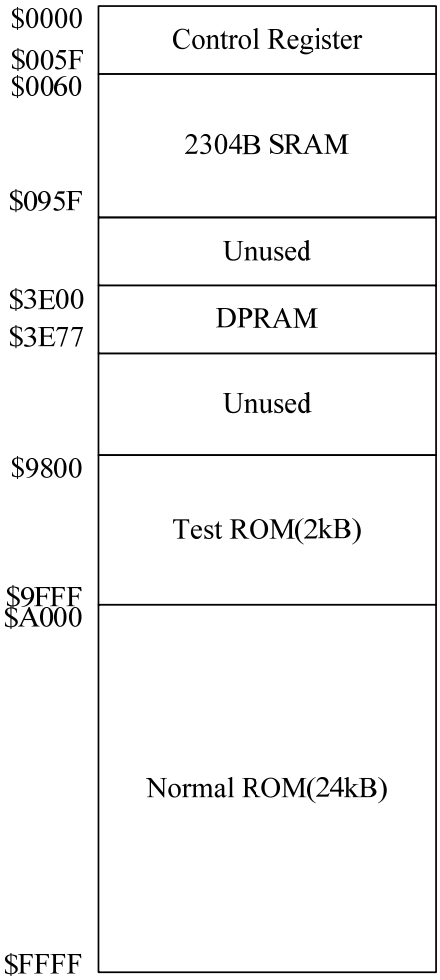
5.7. Auxiliary Calculation Hardware

GPL084A contains auxiliary calculation hardware. This hardware allows some nibble operations to accomplish only at one store and load instruction. The original data content should be stored at the register ($50, $51) firstly and then, many decimal operations, e.g. x10, /10 or nibble swap, can be gotten just by executing reading instruction at the relative register ($52~5D). It speeds up many decimal operations that originally need many instructions for one operation.

5.8. Analog Block

In addition to the LCD controller and clock source, GPL084A also provides many low power and useful analog block. Built-in power switch to change the power source automatically between battery and solar cell source and is helpful for two-way source that is a common solution for many low power systems. A 1.2V or 1.5V internal regulator (by code option) supplies whole system operation at low current environment. Internal low voltage reset analog block prevents the system from runaway at the voltage that is lower than the operation range.

5.9. Map of Memory



5.10. Control Register

Address	Function	Reset value	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$01	P_IO_PortC_Dir	00h	W	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
				Port C Direction control: 0: IN; 1:OUT							
$03	P_IO_PortE_Data	xxh	R	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
		00h	W	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
$04	P_IO_PortE_DataLatch	xxh	R	Read this port to latch the data of Port E							
$05	P_IO_PortC_Data	00h	R	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
			W	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
$06	P_IO_Ctrl	00h	W	-	-	PC[7:4]	PC[3:0]	PE[7:4]	PE[3:2]	PE1	PE0
	Attribute Ctrl			Attribute Control: 1: Unknown, 0: General I/O							
$07	P_LCD_Ctrl	00h	W	Duty1	Duty0	Bias					LCD En
				Duty[1:0] =0=>1/8 duty,1=>1/6 duty,2=>1/5 duty, 3=>1/4 duty; Bias=0=> 1/4 bias,1=>1/3 bias							
$08	P_WAKEUP_Ctrl	00h	R	-	-	-	-	TMBB	T128Hz	TMBA	KEYCH
		00h	W	-	-	-	-	TMBB	T128Hz	TMBA	KEYCH
				TMBB depends on $000A.[1:0]							
$09	P_SYSTEM_Ctrl	xxh	W	Writing any data into $09 to enter sleep mode							

Address	Function	Reset value	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$0A	P_TIMER_TimeBase_Sel	xxh	R	R 0.5Hz	R 1Hz	R 2Hz	R 4Hz	R 8Hz	R 16Hz	R 32Hz	R 64Hz
		00h	W	TMBA: 0: 2Hz 1: 1Hz	-	-	-	-	-	TMBBSEL: 00: 4Hz, 01: 8Hz 10:16Hz, 11:32Hz	
$0B	P_IO_PortE_Dir	00h	W	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
				Port E Direction control: 0: IN; 1:OUT							
$0C	P_CLK_32768_En	00h	W	EN	-	-	-	-	-	-	-
				EN: 32KHz Frequency oscillator enable, low active							
$0D	P_INT_Ctrl	00h	R	-	-	-	TMBBINT	TMBAINT	128HzINT	2KHzINT	-
		00h	W	-	-	-	TMBBEN	TMBAEN	128HzEN	2KHzEN	-
$0E	P_ACON_Reset_Flag	00h	R							FlagON	FlagC
		00h	W							FlagON	FlagC
				FlagON : Reset due to ACON key in at Stop mode(Stop all clock source) FlagC: Reset due to ACON key in at Normal mode(include only CPU sleep)							
$0F	P_WDT_Flag_Clear		W	Writing any data into $0F to clean watchdog							
$37	Code option in test mode (P_37H_CodeOption)	18h	R/W	Wdogopt	HFCLK1	HFCLK0	VBEN	VSEN	RSTPHEN		
				Wdogopt:0=>Watchdog disable, 1=>Watchdog enable; HFCLK[1:0]:0=>225KHz, 1=>500KHz, 2=>1800KHz; VBEN:0=>Battery source disable, 1=>Battery source enable; VSEN:0=>Solar source disable, 1=>Solar source enable RSTPHEN:0=>Reset pin pull high disable, 1=>Reset pin pull high enable							
$41	P_INT_2KHz_Clear	Xxh	W	Writing any data into $41 will clear 2KINT							
$42	P_INT_128Hz_Clear	Xxh	W	Writing any data into $42 will clear 128INT							
$43	P_INT_TimeBaseA_Clear	Xxh	W	Writing any data into $43 will clear 2HZINT							
$44	P_INT_TimeBaseB_Clear	Xxh	W	Writing any data into $44 will clear TMXINT							
$50	P_AUX_DataX	00h	R	Data X							
		00h	W	Data X							
$51	P_AUX_DataY	00h	R	Data Y							
		00h	W	Data Y							
$52	P_AUX_DataX_0H	00h	R	0	0	0	0	X7	X6	X5	X4
$53	P_AUX_DataX_0L	00h	R	0	0	0	0	X3	X2	X1	X0
$54	P_AUX_DataY_0H	00h	R	0	0	0	0	Y7	Y6	Y5	Y4
$55	P_AUX_DataY_0L	00h	R	0	0	0	0	Y3	Y2	Y1	Y0
$56	P_AUX_DataX_H0	00h	R	X7	X6	X5	X4	0	0	0	0
$57	P_AUX_DataX_L0	00h	R	X3	X2	X1	X0	0	0	0	0
$58	P_AUX_DataY_H0	00h	R	Y7	Y6	Y5	Y4	0	0	0	0
$59	P_AUX_DataY_L0	00h	R	Y3	Y2	Y1	Y0	0	0	0	0
$5A	P_AUX_DataX_LH	00h	R	X3	X2	X1	X0	X7	X6	X5	X4
$5B	P_AUX_DataY_LH	00h	R	Y3	Y2	Y1	Y0	Y7	Y6	Y5	Y4
$5C	P_AUX_DataXY_XLYH	00h	R	X3	X2	X1	X0	Y7	Y6	Y5	Y4
$5D	P_AUX_DataXY_YLXH	00h	R	Y3	Y2	Y1	Y0	X7	X6	X5	X4

LCDRAM mapping

	SEG0-SEG7	SEG8-SEG15	SEG16-SEG23	SEG24-SEG31	SEG32-SEG39	SEG40-SEG45
	b0-b7	b0-b7	b0-b7	b0-b7	b0-b7	b0-b5
Com0	$3E00	$3E01	$3E02	$3E03	$3E04	$3E05
Com1	$3E10	$3E11	$3E12	$3E13	$3E14	$3E15
Com2	$3E20	$3E21	$3E22	$3E23	$3E24	$3E25
Com3	$3E30	$3E31	$3E32	$3E33	$3E34	$3E35
Com4	$3E40	$3E41	$3E42	$3E43	$3E44	$3E45
Com5	$3E50	$3E51	$3E52	$3E53	$3E54	$3E55
Com6	$3E60	$3E61	$3E62	$3E63	$3E64	$3E65
Com7	$3E70	$3E71	$3E72	$3E73	$3E74	$3E75

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	-0.3~5 V
Input Voltage Range	V_{IN}	-0.3V to V_+ + 0.3V
Operating Temperature	T_{OPR}	0℃ to +60℃
Storage Temperature	T_{STG}	-40℃ to +125℃
Input Current	I_{IN}	1mA
Output Current	I_{OUT}	1mA
ESD	V_{HMB} (Human Body mode)	2KV
	V_{MM} (Machine mode)	250V
Latchup	V_{PCL}	100mA
	V_{CCL} ESD Induced latchup (MM trigger)	40V

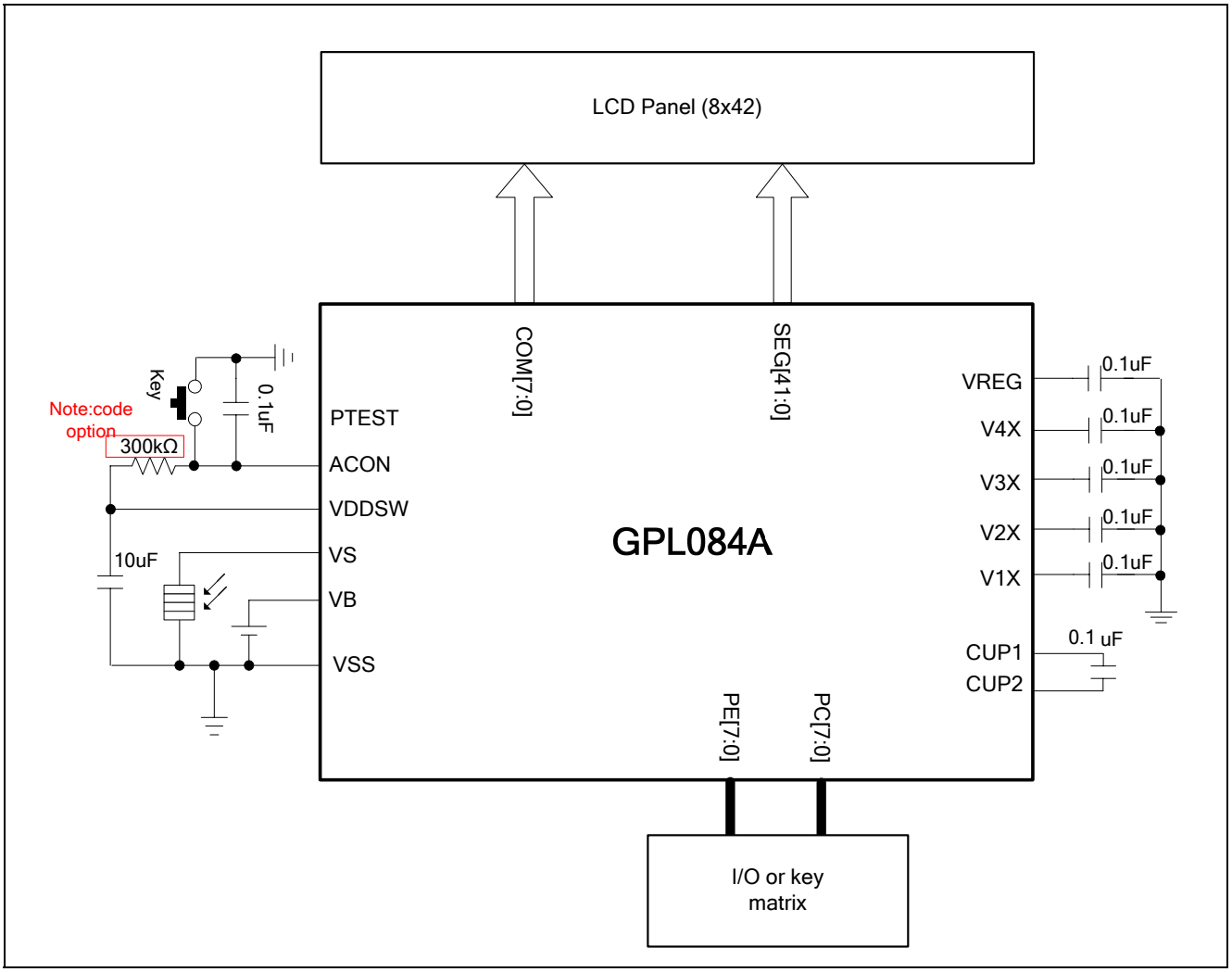
Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics

Characteristics		Symbol	Limit			Unit	Terminal	Test Condition
			Min.	Typ.	Max.			
Operating Voltage		VCC	1.1	-	3.6	V	VDD	
RAM Hold Voltage		V_{HOLD}	1.0	-	-	V	VDD	
Hysteresis voltage of power Switch		V_{HS}	0.09	0.1	0.13	V	VB,VS	
Internal regulator output for logic		VREG	1.0	1.2	1.3	V	VREG	Clock select as 225kHz
			1.3	1.5	1.7	V	VREG	Clock select as 1.8MHz
Input High Level		V_{IH}	VREG*0.7	-	VREG	V	PC,PE	
Input Low Level		V_{IL}	-	-	VREG*0.3	V	PC,PE	
High level output voltage		V_{OH}	VREG*0.7	-	VREG	V	PC,PE	I_{OH}=210uA, VREG=1.2V
Low level output voltage		V_{OL}	-	-	VREG*0.3	V	PC,PE	I_{OL}=500uA, VREG=1.2V
LCD Bias Voltage	1/3 bias	VL1	-5%	1.5	+5%	V	V1X	At 25 deg and -2.7mv/℃
		VL2	-5%	3	+5%	V	V2X	At 25 deg and -5.4mv/℃
		VL3	-5%	4.5	+5%	V	V3X/V4X	At 25 deg and -8.1mv/℃
	1/4 bias	VL1	-5%	1.125	+5%	V	V1X	At 25 deg and -2.7mv/℃
		VL2	-5%	2.25	+5%	V	V2X	At 25 deg and -5.4mv/℃
		VL3	-5%	3.375	+5%	V	V3X	At 25 deg and -8.1mv/℃
		VL4	-5%	4.5	+5%	V	V4X	At 25 deg and -10.8mv/℃
Pull low Resistance		R_{PL}	50	140	300	KΩ	PC,PE	VDD=1.1~3.6V
High Frequency		F_H	-20%	225	+20%	kHz		Clock select as 225kHz
				1800				Clock select as 1800kHz
Low Frequency		F_L	-20%	30.72	+20%	kHz		
LCD Frame Frequency		F_{LCD}	-20%	80	+20%	Hz		1/4,1/6 & 1/8 duty
				77				1/5 duty
Operating Current		I_{OP}	-	13	20	μA		High Frequency =225kHz, CPU on, LCD on, no load (VDD=3.6V)
			-	100	-			High Frequency =1800kHz, CPU on, LCD on, no load (VDD=3.6V)

Characteristics	Symbol	Limit			Unit	Terminal	Test Condition
		Min.	Typ.	Max.			
Halt Current	I_{HALT}	-	3.2	4	μA		Low Frequency active, CPU off, LCD on, no load(VDD=3.6V) @50℃
Standby Current	I_{STBY}	-	-	1.0	μA		Clock is stopped, LCD off(VDD=3.6V) @25℃
		-	-	0.9	μA		Clock is stopped, LCD off(VDD=2.0V) @25℃
		-	-	1.5	μA		Clock is stopped, LCD off(VDD=3.6V) @50℃
Input Leakage Current	I_{INLKG}	-	-	1	μA		VDD=3.6v
LCD Output Rise Time	T_{RLCD}	-	-	20	us		Cload=3nF, Vdd=1.15v
LCD Output Fall Time	T_{FLCD}	-	-	15	us		Cload=3nF, Vdd=1.15v
VDD Rise Time	T_{RVDD}	-	-	1	s		Vdd=1.15v

7. APPLICATION CIRCUITS



8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GPL084A -NnnV - C	Chip form

Note1: Code number (NnnV) is assigned for customer.

Note2: Code number (N = A-Z or 0-9, nn=00-99); version (V = A - Z)

9. DISCLAIMER

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10. REVISION HISTORY

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