DATA SHEET

GPL085A

Low Power 660-dot LCD Controller with 64KB ROM

Aug. 25, 2016

Version 1.4

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LOW POWER 660-DOT LCD CONTROLLER WITH 64KB ROM

1. GENERAL DESCRIPTION

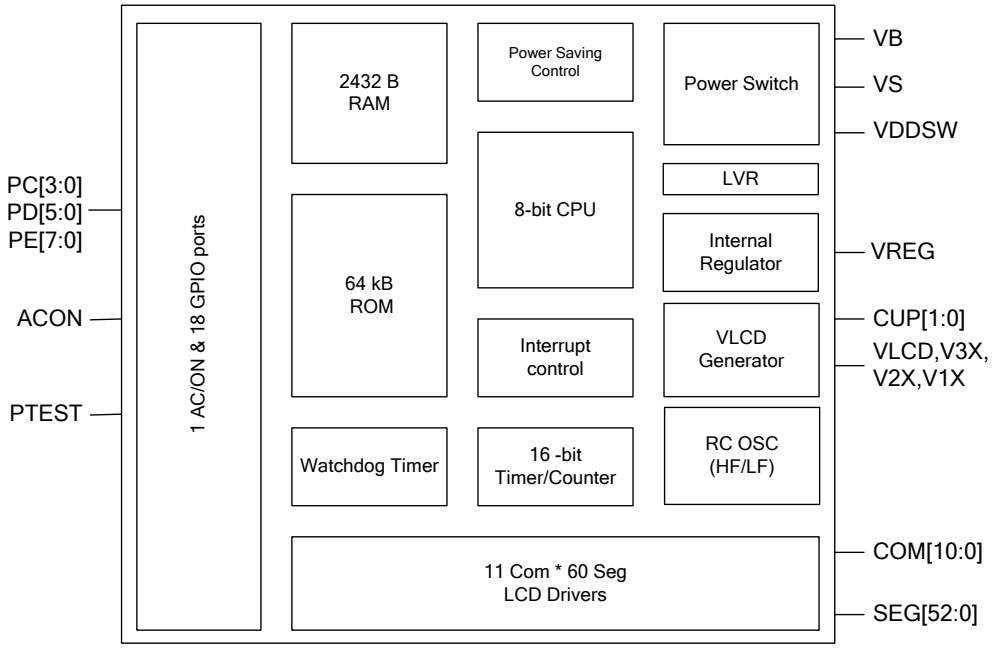
GPL085A, an 8-bit CMOS microprocessor by Generalplus, offers one of the best cost/performance ratio LCD controllers in the industry, equipping RAM/ROM memory, configurable I/Os, an interrupt controller, and an automatic display controller/driver in a single and compact package. One of its extraordinary features is the capability of operating under a low voltage range of 1.2V ~ 3.6V, which is especially suitable for solar cell environment. It also outfits an internal power switch to alternately change in between two types of power sources- solar cell and battery. This device is applicable for applications such as low power calculator and products requiring either one solar cell or battery power, or a two-way power from both of them.

2. FEATURES

- Built-in 8-bit processor
- 2432-byte SRAM
- 64K-byte ROM(including 2KB test code ROM size)
- 88-byte DPRAM
- Built-in 225k/500k/1000k/1800kHz RC oscillator for system operation
  - Adjustable CPU clock speed : 1, 1/2, 1/4, 1/8, 1/16 for R_{OSC} 1000k/1800kHz CPU clock speed can only be used at operating voltage 1.8V~3.6V
- Built-in 30.72kHz RC oscillator
- Low operating voltage: 1.2V – 3.6V
- Low standby current, I_{STBY} < 1uA @3.6V, 25℃
- 18 general I/O pins.
  PD[5:0](PD[5:3] are shared with SEG[57:59]; PD[1:0] are shared with 2 buzzers)
  PC[3:0](shared with SEG[53:56])
  PE[7:0]
- LCD configurations: 11 coms x 60 segs (MAX) , 3x60, 4x60, 5x60, 6x60, 8x60, 9x60, 10x60, 4x64
- LCD 1/3 ,1/4 bias, 1/3, 1/4, 1/5, 1/6,1/8, 1/9, 1/10, 1/11 duty
- One 16-bit reloadable timer/counter
- Watchdog mode (~ 2 seconds)
- Six interrupt sources:
  TMBB, TMBA, 128Hz, 2KHz, Timer, EXT(PD2)
- Power down mode
  Wakeup sources: key input, TMBB, TMBA,128Hz, Timer
- Built-in power switch for two-way power sources
  - 15uA @ 3.6V, F_{CPU} = 225KHz under operating mode
  - 3uA @ 3.6V, F_{CPU} = 225KHz under halt mode
  - I stby < 1uA @ 3.6V
- Built-in internal regulator for LCD operation, 5-level contrast control
- Built-in internal regulator for system operation
- Built-in low voltage reset to prevent unusual system operation under a low voltage condition.

Note1: TMBB: 4KHz, 1KHz, 128Hz, 64Hz, 32Hz, 16Hz, 8Hz or 4Hz
Note2: TMBA: 2Hz or 1Hz

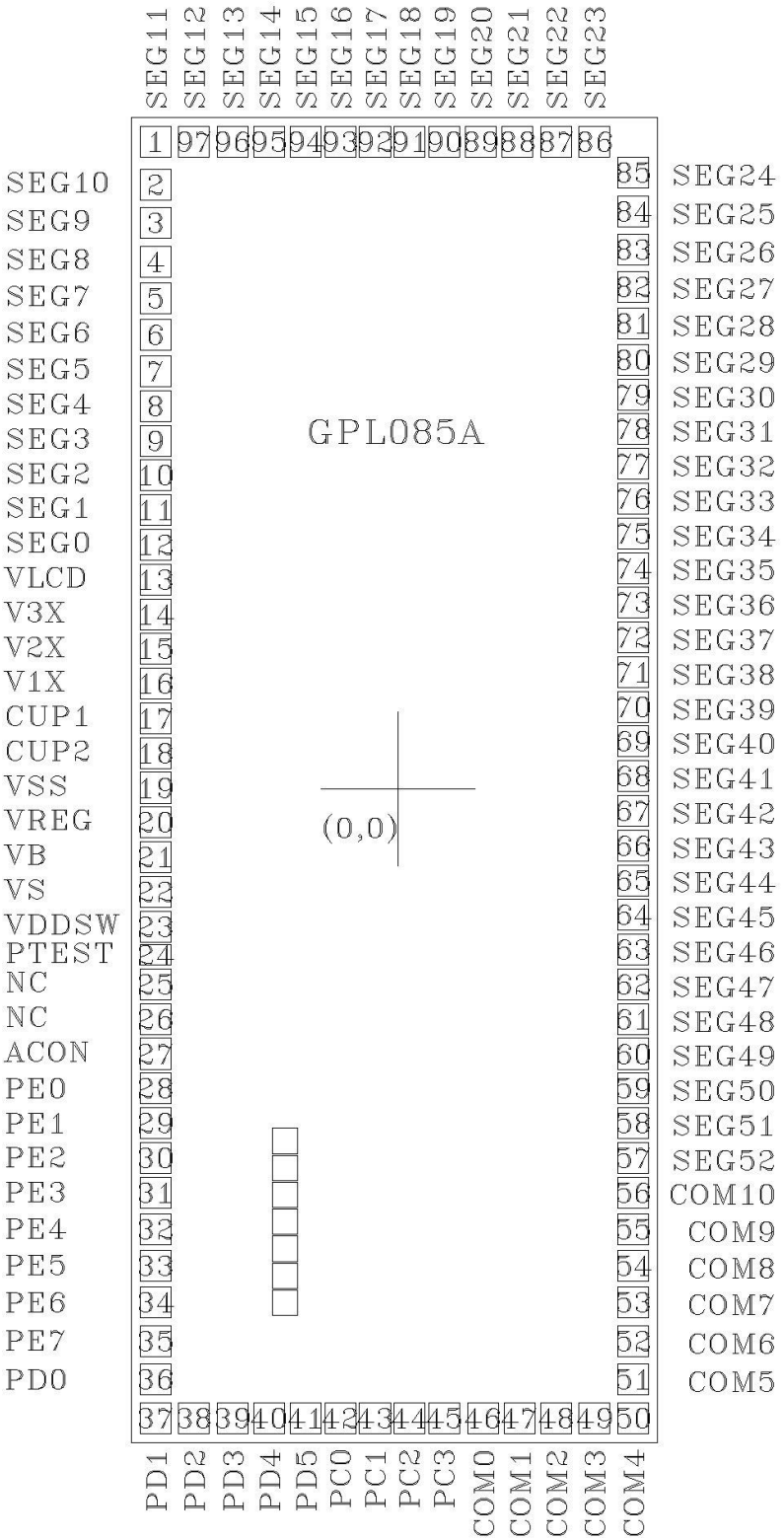
3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

Mnemonic	Type	Description
VS	I	Solar cell power input.
VB	I	Battery power input.
VDDSW	O	Power switch output.
VREG	O	Internal regulator output.
VSS	I	Ground input.
COM[2:0]	O	LCD driver common output.
COM[10:3]	O	LCD driver common output. (COM[10:4] can be opted to SEG[57:63] and COM3 to SEG56)
SEG[52:0]	O	LCD driver segment output.
PD[5:0]	I/O	GPIO I/O port. (PD[5:3] are shared with SEG[57:59]; PD[1:0] are shared with 2 buzzers)
PC[3:0]	I/O	GPIO I/O port. (shared with SEG[53:56])
PE[7:0]	I/O	GPIO I/O port.
ACON	I	Clear or system power on pin (active low) and 4ms debouncing circuit inside.
PTEST	I	Test mode input pin. (active high)
V1X V2X V3X VLCD	O	VLCD generator output.
CUP1 CUP2	I	Inputs for LCD bias settings

4.1. PAD Assignment



Note1: This IC substrate should be connected to VSS or floated.

Note2: To ensure IC functions properly, please bond all of VDD and VSS pins.

Note3: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

5. FUNCTION DESCRIPTION

5.1. CPU

The 8-bit CPU adopted in GPL085A is a high performance processor featuring an Accumulator, a Program Counter, an X Register, a Y Register, a Stack pointer and a Processor Status Register (this is the same as CPU 6502 instruction structure).

5.2. Clock Source

The GPL085A equips with two groups of clock sources:

(1) Four high speed frequency (RCHF) options support the entire system operation: 225KHz, 500KHz, 1000KHz, 1800KHz, selectable from Register $18H based on requirements. GPL085A features programmable CPU clock options for power sources, including 1, 1/2, 1/4, 1/8, or, 1/16 of RCHF.

(2) A low speed frequency, derived from IOSC30K, controls LCD frame rate and time base timer.

5.3. ROM/RAM Area

The GPL085A features 64K-byte ROM that can be defined as a program area, located from $4000 to $FFFF. Its RAM memory consists of 2432 bytes (including Stack) at locations from $60 through $9DF.

5.4. Stop Clock Mode

A power saving mode is designed in GPL085A for applications requiring low energy consumption. Users can simply enable wake-up sources and stop the CPU clock via writing data into STOP CLOCK Register ($09). CPU will then enter standby mode and both RAM memory and I/Os keep remaining at their previous states until wakeup. There are five wake-up sources available in GPL085A: Port PortE wake-up, TMBB, TMBA, T128Hz, and Timer wake-up. After GPL085A wakes up from power saving mode, CPU will proceed to execute the next instruction right after the moment of entering sleep mode. Wake-up action will not influence both RAM and I/Os.

Note1: TMBB: 4KHz, 1KHz, 128Hz, 64Hz, 32Hz, 16Hz, 8Hz or 4Hz

Note2: TMBA: 2Hz or 1Hz

5.5. I/O Ports

The GPL085A has three input/output ports: PortC, PortD and PortE. These port pins all equip with special features for key board scan function. In general, when an initial reset starts, all ports are used as general purpose input ports. All PortC, PortD, and PortE contain three major parts: data, direction, and attribution registers. Please follow the table below to define each I/O function with corresponding bit in each port.

PortC[3:0], PortD[5:0], PortE[7:0]

Attribution	Direction	Data	Function	Description
0	0	0	Input with pull-low	General Purpose I/O function
0	0	1	Pure Input	
0	1	0	Output Low	
0	1	1	Output High	
1	1	0	Pad Floating	Special function

5.6. LCD Controller

GPL085A contains a LCD controller/driver that provides the capability to drive 11 commons and 60 segments LCD. To reduce the CPU loading, a display buffer is designed for mapping it to LCD. A LCD dot/pattern is set ON or OFF by programming the corresponding bit of the display buffer. In addition, the LCD bias can be programmed as 1/3 or 1/4. The available duty options are 1/3, 1/4, 1/5, 1/6, 1/8, 1/9, 1/10, or 1/11. The frame rate is set to 85Hz at 1/9 duty, 77Hz at 1/10 duty; and 87Hz at 1/11 duty. When selecting 1/3, 1/4, 1/6, or 1/8 duty, its frame rate is set to 80Hz. The frame rate is measured when low speed frequency equals to 30.72KHz.

5.7. LCD Voltage Generation

The GPL085A offers a voltage regulator and a charge-pumping circuit. Users can get the desired VLCD by changing the output reference voltage (writing to register) of the voltage regulator. Enabling the voltage regulator and charge-pumping circuit gets a stable VLCD that will not be affected by VDD. The VLCD is adjustable from 3V to 4.5V with 5 levels at 1/3 bias, or 4.0V to 6.0V with 5 levels at 1/4 bias. It is suggested that VLCD must be higher than VDD or abnormal operation will take place.

5.8. Buzzer Driver

PD[1:0] can be used as buzzer output. When $16.b1 = b0 = '1', PD.1 and PD.0 are set for buzzer output. Or else when b1 = b0 ='0', PD.1 and PD.0 are set to normal I/O. When counter overflows, it will toggle PD.1 and PD.0 to drive buzzer.

5.9. Auxiliary Calculation Hardware

GPL085A contains auxiliary calculation hardware. This hardware allows some nibble operations to accomplish only at one store and

one load instruction. The original data content should first be stored at the register ($50, $51) and then many decimal operations, e.g., x10,/10 or nibble swap, can be acquired just by executing read instruction at the relevant registers ($52~5F). It speeds up many decimal operations that originally need several instructions for one operation.

5.10. Analog Block

In addition to the LCD controller and clock source, GPL085A also equips many low power and useful analog blocks. The built-in power switch changes the power source automatically between battery and solar cell source and is helpful for two-way source that is a common solution for many low power systems. Either 1.2V or 1.5V internal regulator by register provides whole system operation at low current environment. The internal low voltage reset analog block prevents the system from abnormal operation at the voltage lower than the operating range.

5.11. Mask Options

5.11.1. Watchdog timer

1). Enabled
2). Disabled

5.11.2. Operation voltage selection

1). 1.2V~1.8V
2). 1.8V~3.6V

5.11.3. SEG53/PC3 pin share selection

1). Pin used as PC3
2). Pin used as SEG53

5.11.4. SEG54/PC2 pin share selection

1). Pin used as PC2
2). Pin used as SEG54

5.11.5. SEG55/PC1 pin share selection

1). Pin used as PC1
2). Pin used as SEG55

5.11.6. SEG56/PC0 pin share selection

1). Pin used as PC0
2). Pin used as SEG56

5.11.7. SEG57/PD5 pin share selection

1). Pin used as PD5
2). Pin used as SEG57

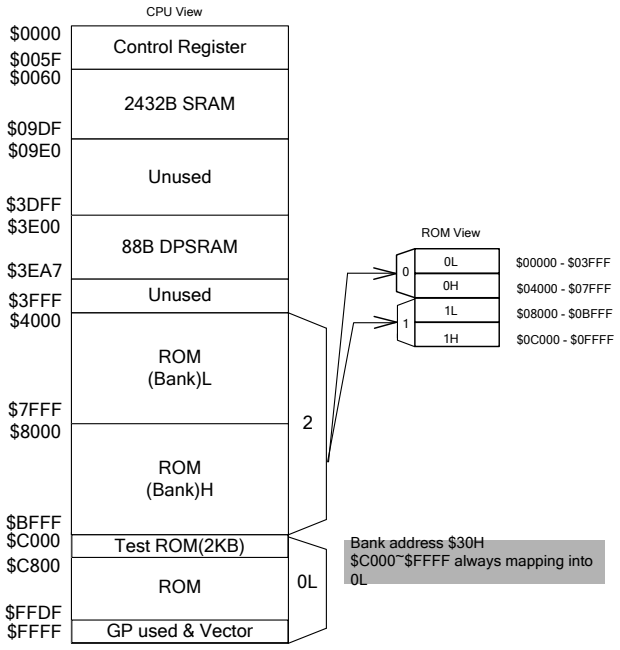
5.11.8. SEG58/PD4 pin share selection

1). Pin used as PD4
2). Pin used as SEG58

5.11.9. SEG59/PD3 pin share selection

1). Pin used as PD3
2). Pin used as SEG59

5.12. Map of Memory



6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	-0.3~5 V
Input Voltage Range	V_{IN}	-0.3V to V_+ + 0.3V
Operating Temperature	T_{OPR}	0℃ to +70℃
Storage Temperature	T_{STG}	-40℃ to +125℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics(T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Terminal	Test Condition
		Min.	Typ.	Max.			
Operating Voltage	VCC	1.2	-	1.8	V	VDDSW	Operation voltage select 1.2~1.8V
		1.8	-	3.6			Operation voltage select 1.8~3.6V
Hysteresis voltage of power Switch	V_{HS}	0.09	0.1	0.13	V	VB,VS	
Internal regulator output for logic	VREG	1.1	1.2	1.4	V	VREG	Operation voltage select 1.2~1.8V
		1.3	1.5	1.7			Operation voltage select 1.8~3.6V
Input High Level	V_{IH}	Vddsw*0.7	-	Vddsw	V	PC,PD,PE	
Input Low Level	V_{IL}	-	-	Vddsw*0.3	V	PC,PD,PE	
Output High Current (I/O)	I_{OH}	2.0	-	-	mA	PC,PD,PE	Vddsw = 3.0V, V_{OH} = 0.7*Vddsw
		0.4	-	-			Vddsw = 1.5V, V_{OH} = 0.7*Vddsw
Output Sink Current (I/O)	I_{OL}	4.0	-	-	mA		Vddsw = 3.0V, V_{OL} = 0.3*Vddsw
		1.0	-	-			Vddsw = 1.5V, V_{OL} = 0.3*Vddsw
Output High Current (Buzzer)	I_{OH}	8	-	-	mA	PD[1:0]	Vddsw = 3.0V, V_{OH} = 0.7*Vddsw
		2	-	-			Vddsw = 1.5V, V_{OH} = 0.7*Vddsw
Output Sink Current (Buzzer)	I_{OL}	10	-	-	mA		Vddsw = 3.0V, V_{OL} = 0.3*Vddsw
		3	-	-			Vddsw = 1.5V, V_{OL} = 0.3*Vddsw
LCD Bias Voltage	Vlcd	-5%	3.0~4.5	+5%	V	Vlcd	1/3 bias, At 25 deg and -8.1mv/℃
			4.0~6.0				1/4 bias,At 25 deg and -10.8mv/℃
Pull low Resistance	R_{PL}	50	140	210	K	PC,PD,PE	VDD=1.2~3.6V
High Frequency	F_H	-20%	225	+20%	kHz		Clock selected as 225kHz
		-	500	-			Clock selected as 500kHz
			1000				Clock selected as 1000kHz
			1800				Clock selected as 1800kHz
Low Frequency	F_L	-20%	30.72	+20%	kHz		Low speed clock
Operating Current	I_{OP}	-	15	20	μA		High Frequency =225kHz, CPU on, LCD on, without loading (VDD=3.6V)
		-	35	-	μA		High Frequency =500kHz, CPU on, LCD on, without loading (VDD=3.6V)
		-	65	-	μA		High Frequency =1000kHz, CPU on, LCD on, without loading (VDD=3.6V)
		-	100	-	μA		High Frequency =1800kHz, CPU on, LCD on, without loading (VDD=3.6V)

Characteristics	Symbol	Limit			Unit	Terminal	Test Condition
		Min.	Typ.	Max.			
Halt Current	I_{HALT}	-	3	4	μA		Low Frequency active, CPU off, LCD on, no load(VDD=3.6V)
Standby Current	I_{STBY}	-	1.0	1.5	μA		Clock is stopped, LCD off(VDD=3.6V) @ Vreg = 1.5v
		-	0.55	1.0	μA		Clock is stopped, LCD off(VDD=3.6V) @ Vreg = 1.2v

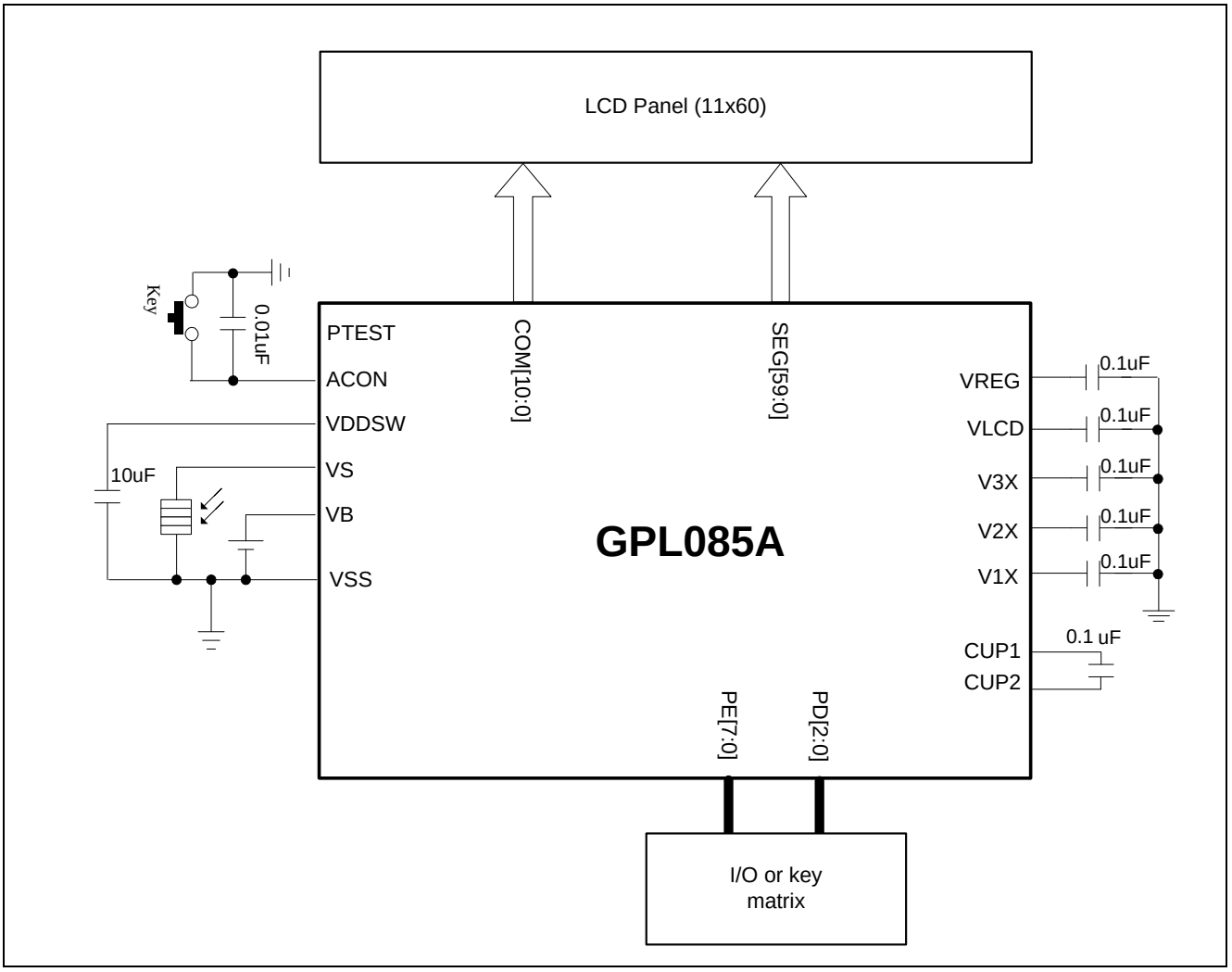
Note1: Vlcd should be higher than VDD to prevent forward biasing the p-n junction of I/O output PMOS.

Note2: Only the main CPU frequency selected in confirmation sheet is guaranteed in the range of +/-20% variation, and the other frequencies may be beyond the range of +/-20% variation.

For example, if 1800KHZ is selected as CPU frequency in confirmation sheet, 1800KHZ is varied in the range of +/-20%. The other frequencies such as 225KHZ, 500KHZ, or 1000KHZ may beyond the range of +/-20% variation.

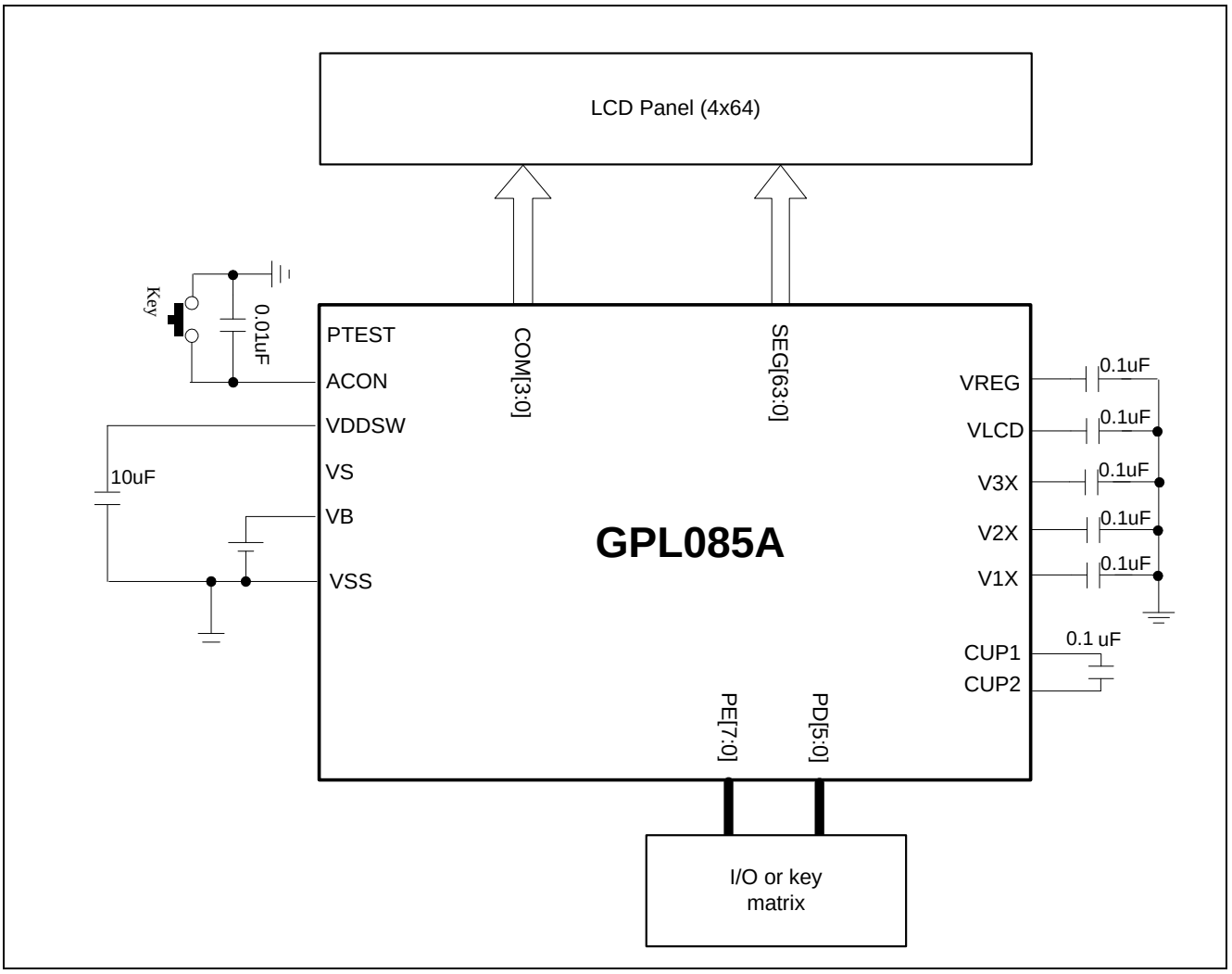
7. APPLICATION CIRCUITS

7.1. 660 Dots LCD Driver, 60 Segments × 11 Commons, 1/4bias, dual power supply - (1)



Note1: These capacitor values are for design reference only. Different capacitor values may be required for different crystal/resonator used.

7.2. 256 Dots LCD Driver, 64 Segments × 4 Commons, 1/3bias, Battery power supply - (2)



8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GPL085A - NnnV - C	Chip form

Note1: Code number (NnnV) is assigned for customer.

Note2: Code number (N = A-Z or 0-9, nn=00-99); version (V = A - Z)

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10. REVISION HISTORY

Date	Revision #	Description	Page
Aug. 25, 2016	1.4	Modify Standby Current Characteristics in section 6.2 DC Characteristics.	9
Mar. 15, 2016	1.3	modified section 6.2	9-10
Dec. 28, 2011	1.2	Modify 4.1 Pad Assignment.	6
Oct. 11, 2011	1.1	Xtal32K description removed.	
Jun. 16, 2011	1.0	1. Modify GENERAL DESCRIPTION	3
		2. Modify FEATURES	3
		3. Modify SIGNAL DESCRIPTION	5,6
		4. Modify Low Voltage Generation	7
		5. Modify Operation Voltage Selection	8
		6. Modify Map Memory	8
		7. Modify ELECTRICAL SPECIFICATIONS	9
		8. Modify APPLICATION CIRCUITS	11
Oct. 08, 2010	0.2	1. Modified features;	3
		2. Add PAD assignment at section 4.1;	5
		3. Modified section 5.4, 5.5, 5.7 & 5.10;	6~7
		4. Add mask option description at section 5.11;	7
		5. Modified control register description at section 5.12;	9~10
		6. Modified DC characteristics at section 6.2;	11
		7. Modified application circuit at section 7.	13
SEP. 16, 2009	0.1	Original	16