DATA SHEET

GPL086A

Low Power 3072 dots LCD Controller with 160KB ROM

Aug. 26, 2016

Version 1.1

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LOW POWER 3072-DOT LCD CONTROLLER WITH 160KB ROM

1. GENERAL DESCRIPTION

GPL086A, an 8-bit CMOS microprocessor by Generalplus, offers one of the best cost/performance ratio LCD controllers in the industry, equipping RAM/ROM memory, configurable I/Os, an interrupt controller, and an automatic display controller/driver in a single and compact package. One of its extraordinary features is the capability of operating under a low voltage range of 1.1V ~ 3.6V, which is especially suitable for applications requiring effective power consumption such as low-power calculator and relevant LCD products.

2. FEATURE

■ 8-bit processor

■ 6048-byte SRAM

■ 160K-byte ROM (includes 2KB test code ROM size)

■ 384-byte DPRAM

■ Built-in 225KHz/500KHz/1000KHz/1800KHz/4000KHz RC OSC for system operation

- Adjustable CPU clock speed options: 1, 1/2, 1/4, 1/8, 1/16 of ROSC
- 1000KHz/1800KHz/4000KHz CPU speeds only can be used at operating voltage range of 1.8V ~ 3.6V.

■ Built-in 30.72kHz RC oscillator

■ Low operating voltage: 1.1 V – 3.6 V

■ Low standby current, I_{STBY} < 1uA @3.6V,25℃

■ 36 general I/O pins.

PA[3:0] (PA[3:2]share with SEG[94:95])

PB[7:0] (shared with COM[16:23])

PC[7:0] (shared with COM[24:31])

PD[7:0] (PD6 can be used as EXT2INT, PD2 can be used as EXTINT, PD[1:0] shared with 2 Buzzer)

PE[7:0]

■ LCD configurations: 32 coms x 96 segs (MAX), 24X96, 16X96, 11X64, 10X64, 9X64, 8X64, 6X64, 5X64, 4X64, 3X64, 2X64

■ LCD 1/2, 1/3, 1/4, 1/5 bias; 1/2, 1/3, 1/4, 1/5, 1/6, 1/8, 1/9, 1/10, 1/11, 1/16, 1/24, 1/32 duty

■ One 16-bit reloadable timer/counter(Timer0), Two 8-bit reloadable timers or counters（Timer1,Timer2）

■ Serial Peripheral Interface(SPI)

- SPI CSN/SCK/SDI/SDO pins share with SEG[93:90]

■ Watchdog mode (~2 seconds)

■ 12 interrupt sources

IRQ controller

- 2KHz for RTC
- 128Hz
- TMBB（4Hz/8Hz/16Hz/32Hz/64Hz/128Hz/1KHz/4KHz）
- TMBA（1Hz/2Hz）
- EXTINT(PD2)
- EXT2INT(PD6)
- Timer0 overflow
- Timer1 overflow
- Timer2 overflow
- Low battery voltage detection
- DMA
- SPI

■ Power down mode

(wake-up sources: key input, TMBB, TMBA, 128Hz, Timer0, Timer1, Timer2)

■ Low power consumption:

- 30uA @ 1.5V, Fcpu = 225KHz for operating mode
- 8uA @ 1.5V, Fcpu = 225KHz for halt mode
- Istby < 1uA @ 1.5V

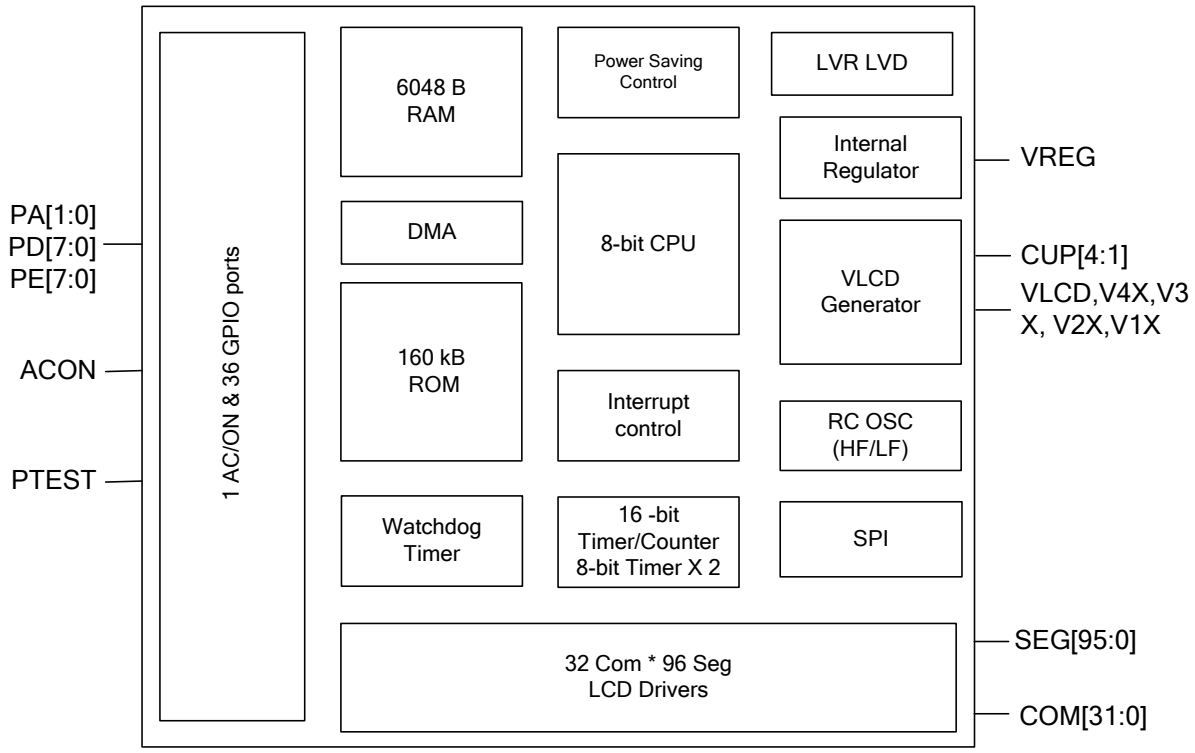
■ Internal regulator for LCD operation, 16-level contrast control

■ Internal regulator for system operation

■ 1.2V/2.0V/2.2V/2.5V low voltage detector

■ Low voltage reset to prevent system crash at low voltage condition.

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTION

Mnemonic	Type	Description
VDD	I	Power supply voltage input.
VREG	O	Internal regulator output.
VSS	I	Ground input.
COM[15:0]	O	LCD driver common output.
COM[23:16]	I/O	LCD driver common output. (COM[23:16] shared with PB[0:7])
COM[31:24]	I/O	LCD driver common output. (COM[31:24] shared with PC[0:7]; COM[31:26] can be altered to SEG[93:88]);
SEG[89:0]	O	LCD driver segment output.
SEG[93:90]	I/O	LCD driver segment output. (SEG[93:90] shared with SPI CSN/CLK/SDI/SDO)
SEG[95:94]	I/O	LCD driver segment output. (SEG[95:94] shared with PA[3:2])
PA[1:0]	I/O	GPIO I/O port.
PE[7:0]	I/O	GPIO I/O port.
PD[7:0]	I/O	GPIO I/O port. (PD[1:0] shared with 2 Buzzers)
ACON	I	Clear or system power on pin (active low) and 4ms debounce circuit inside.
PTEST	I	Test mode input pin. (active high)
V1X V2X V3X V4X VLCD	O	VLCD generator output.
CUP1 CUP2 CUP3 CUP4	I	Inputs for LCD bias setup.

Total 160 PADs

5. FUNCTIONAL DESCRIPTIONS

5.1. CPU

The 8-bit CPU adopted in GPL086A is a high performance processor featuring an Accumulator, a Program Counter, an X Register, a Y Register, a Stack pointer and a Processor Status Register (this is the same as CPU 6502 instruction structure).

5.2. Clock Source

The GPL086A equips with two groups of clock sources:

(1) High speed frequency (RCHF) options support the entire system operation: 225KHz, 500KHz, 1000KHz, 1800KHz, 4000KHz, selectable from Register $18H based on requirements. GPL086A features programmable CPU clock options for power sources, including 1, 1/2, 1/4, 1/8, or, 1/16 of RCHF.

(2) A low speed frequency, derived from IOSC30K, controls LCD frame rate and time base timer.

5.3. ROM/RAM Area

GPL086A has 160K-byte ROM that can be defined for program area, located from $4000 to $FFFF. Its RAM consists of 6048 bytes (including Stack) at locations from $60 through $17FF.

5.4. Stop Clock Mode

A power saving mode is designed in GPL086A for applications requiring low energy consumption. Users can simply enable wake-up sources and stop the CPU clock via writing data into STOP CLOCK Register ($09). CPU will then enter standby mode and both RAM memory and I/Os keep remaining at their previous states until wakeup. There are seven wake-up sources available in GPL086A: Port PortE wake-up, TMBA, TMBB, T128Hz, and Timer0, Timer1 or Timer2 wake-up. After GPL086A wakes up from power saving mode, CPU will proceed to execute the next instruction right after the moment of entering sleep mode. Wake-up action will not influence both RAM and I/Os.

Note1: TMBB: 4KHz, 1KHz, 128Hz, 64Hz, 32Hz, 16Hz, 8Hz or 4Hz

Note2: TMBA: 2Hz or 1Hz

5.5. I/O Ports

The GPL086A has five input/output ports: PortA, PortB, PortC, PortD and PortE. These port pins all equip with special features for key board scan function. In general, when an initial reset starts, all ports are used as general purpose input ports. All ports contain three major parts: data, direction, and attribution registers. Please follow the table below to define each I/O function with corresponding bit in each port.

PortA[3:0], PortB[7:0], PortC[7:0], PortD[7:0] , PortE[7:0]

Attribution	Direction	Data	Function	Description
0	0	0	Input with pull-low	General Purpose I/O function
0	0	1	Pure Input	
0	1	0	Output Low	
0	1	1	Output High	
1	1	0	Pad Floating	Special function

5.6. LCD Controller

GPL086A contains a LCD controller/driver that provides the capability to drive 32 commons and 96 segments LCD. To reduce CPU loading, a display buffer is designed for mapping it to LCD. A LCD dot/pattern is set ON or OFF by programming the corresponding bit of the display buffer. In addition, the LCD bias can be programmed as 1/2, 1/3, 1/4 or 1/5. The available duty options are 1/2, 1/3, 1/4, 1/5, 1/6, 1/8, 1/9, 1/10, 1/11, 1/16, 1/24, or 1/32. The frame rate is set to 85Hz at 1/9 duty, 77Hz at 1/5 duty or 1/10 duty; and 87Hz at 1/11 duty. The frame rate is measured when low speed frequency equals to 30.72KHz.

5.7. LCD Voltage Generation

The GPL086A offers a voltage regulator and a charge-pumping circuit. Users can get the desired VLCD by changing the output reference voltage (writing to register) of the voltage regulator. Enabling the voltage regulator and charge-pumping circuit gets a stable VLCD that will not be affected by VDD. The VLCD is adjustable from 3.0V to 4.5V with 16 levels at 1/3 bias, 4.0V to 6.0V with 16 levels at 1/4 bias, 5.0V to 6.5V with 10 levels at 1/5 bias, or 3.0V at 1/2 bias.

5.8. Buzzer Driver

PD[1:0] can be used as buzzer output. When $16.b1 = b0 = '1', PD.1 and PD.0 are set for buzzer output. Or else when b1 = b0 = '0', PD.1 and PD.0 are set to normal I/O. When Timer0 overflows, it will toggle PD.1 and PD.0 to drive buzzer.

5.9. Auxiliary Calculation Hardware

GPL086A contains auxiliary calculation hardware. This hardware allows some nibble operations to accomplish only at one store and one load instruction. The original data content should first be stored at the register ($50, $51) and then many decimal operations, e.g., x10,/10 or nibble swap, can be acquired just by executing read instruction at the relevant registers ($52~5F). It speeds up many decimal operations that originally need several instructions for one operation.

5.10. DMA function

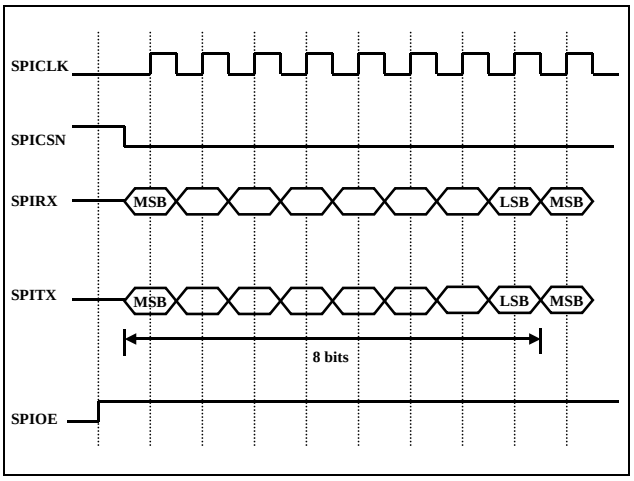
GPL086A contains DMA for direct access from ROM/RAM to RAM/DPRAM. User can select access mode by control register including ROM to DPRAM, ROM to RAM, RAM to DPRAM and DPRAM to RAM. Status flag will go high when DMA action is done.User can choose to generate DMA endflag interrupt or not.

5.11. Analog Block

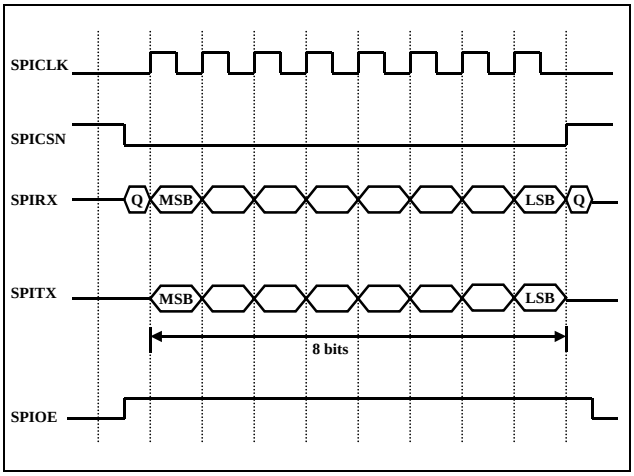
In addition to the LCD controller and clock source, GPL086A also equips many low power and useful analog blocks. Either 1.2V or 1.5V internal regulator optional via mask option provides whole system operation at low current environment. It also features a 1.2V, 2.0V, 2.2V, or 2.5V voltage detector to detect the voltage on VDD pin and user can read the state of VDD from Port $1B. If VDD is higher than LVD level (1.2V, 2.0V, 2.2V or 2.5V), $1B.bit0 will be '0', else it will be '1'. Internal low voltage reset analog block prevents the system from abnormal operation at the voltage lower than the operating range.

5.12. SPI Controller

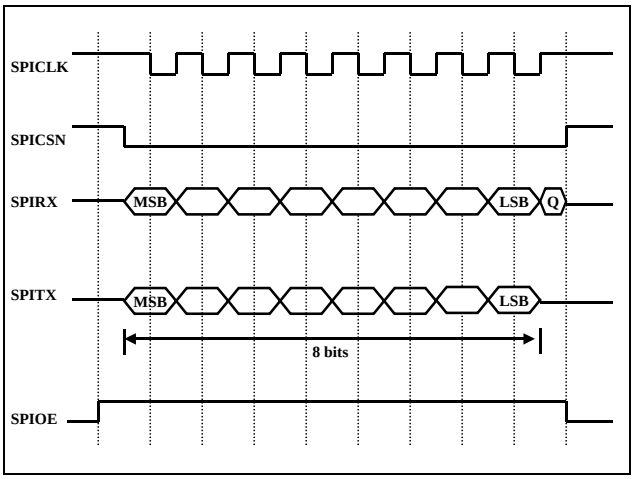
Serial Peripheral Interface (SPI) is a synchronous data bus that offers separate lines for data and clock to keep two sides of talk in synchronous. An SPI controller built inside GPL086A, as standard, enables synchronous serial communication with master and slave peripherals. In our design, there are four control signals operating on SPI including SPICSN (SEG93), SPICLK (SCK, SEG92), SPIRX (SDI, SEG91), and SPITX (SDO, SEG90). The segment numbers indicated in the parenthesis represent the segment pins shared with SPI signal pins. While SPI module is enabled by a corresponding control bit, these four pins cannot be functioning segment out and any setting on corresponding GPIO control register will take no effect. Four types of timing are depicted as follows:



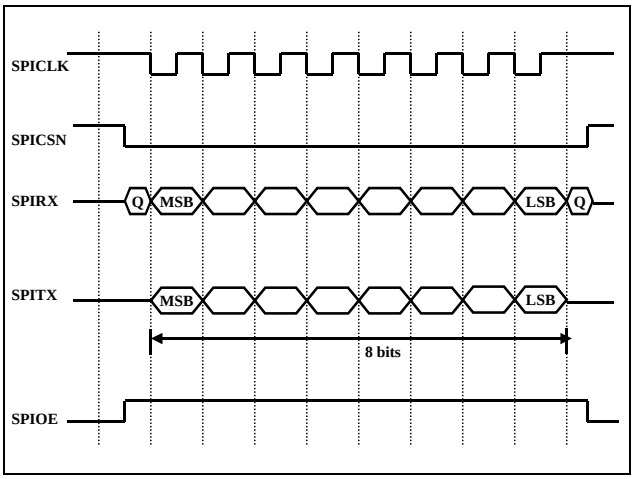
Master Mode, SPO = 0, SPH=0



Master Mode, SPO = 0, SPH=1



Master Mode, SPO = 1, SPH=0



Master Mode, SPO = 1, SPH=1

5.13. Mask Options

5.13.1. Watchdog timer

1). Enable

2). Disable

5.13.2. Internal 1M-Ohm reset pull high resistor

1). Enable

2). Disable

5.13.3. Low voltage detecting function selection

1). Disable

2). Enable

5.13.4. LCD pump clock speed selection

1). 2KHz

2). 4KHz

3). 8KHz

5.13.5. DMA function selection

1). Disable

2). Enable

5.13.6. SPI function selection

1). Disable

2). Enable

5.13.7. COM/PC pin shared selection

1). Pin used as PC[7:0]

2). Pin used as COM[24:32]

5.13.8. COM/PB pin shared selection

1). Pin used as PB[7:0]

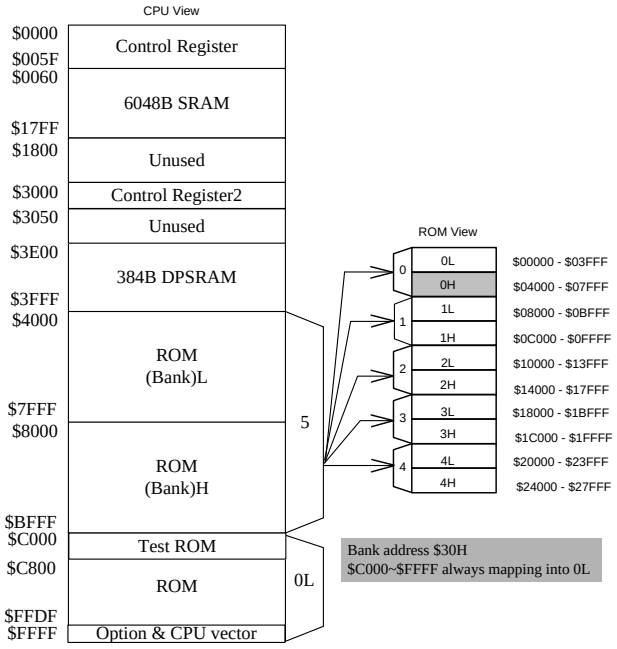
2). Pin used as COM[16:23]

5.13.9. SEG/PA pin shared selection

1). Pin used as PA[3:2]

2). Pin used as SEG[94:95]

5.14. Map of Memory



6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	-0.3~5 V
Input Voltage Range	V_{IN}	-0.3V to V_+ + 0.3V
Operating Temperature	T_{OPR}	0℃ to +60℃
Storage Temperature	T_{STG}	-40℃ to +125℃

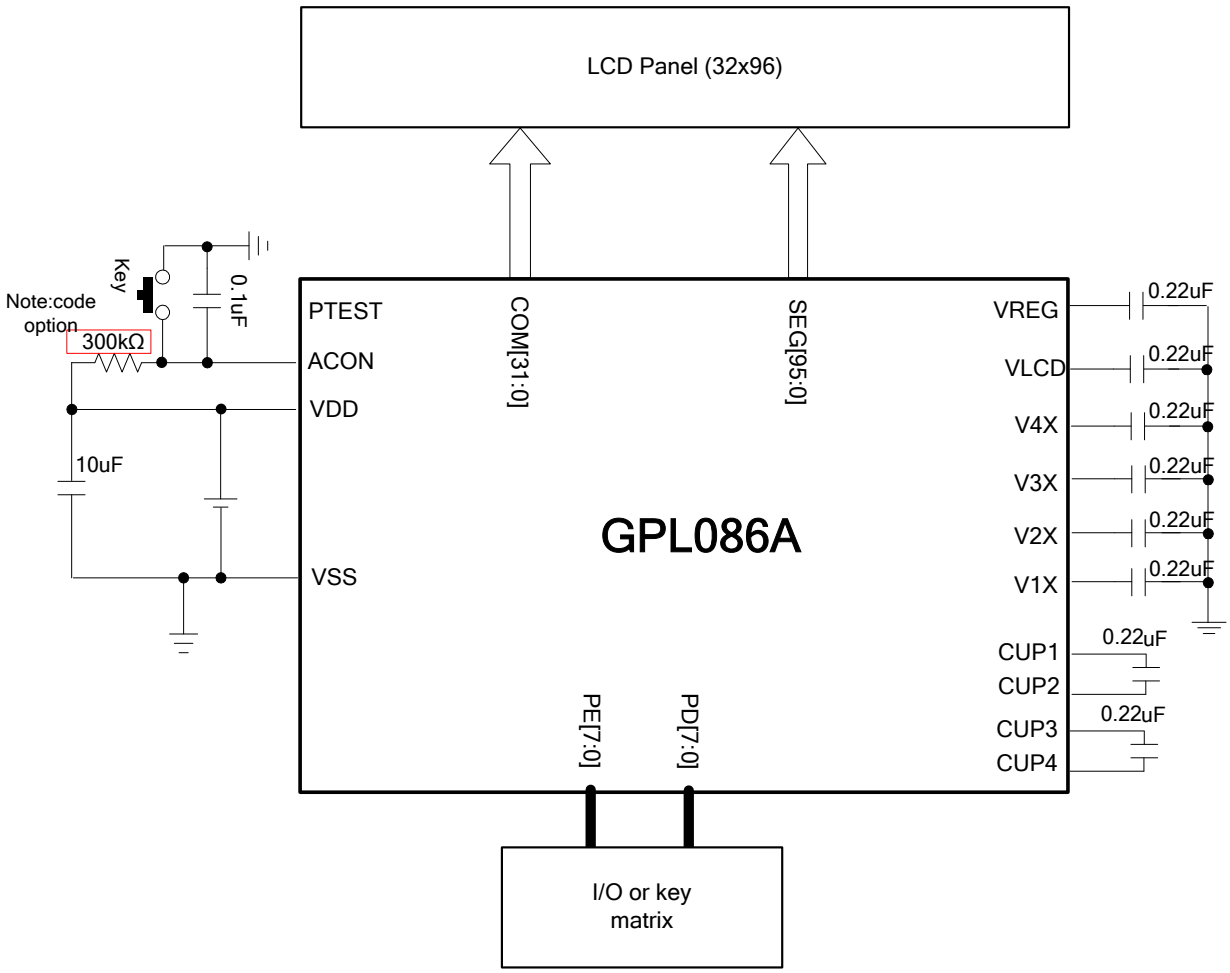
Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Terminal	Test Condition
		Min.	Typ.	Max.			
Operating Voltage	VCC	1.1	-	1.8	V	VDD	Operation voltage select 1.1~1.8V
		1.8	-	3.6			Operation voltage select 1.8~3.6V
Internal regulator output for logic	VREG	1.0	1.2	1.3	V	VREG	Operation voltage select 1.1~1.8V
		1.3	1.5	1.7	V	VREG	Operation voltage select 1.8~3.6V
Input High Level	V_{IH}	Vdd*0.7	-	Vdd	V	PA,PB,PC, PD,PE	
Input Low Level	V_{IL}	-	-	Vdd*0.3	V		
Output High Current (I/O)	I_{OH}	2.0	-	-	mA	PA,PB, PC,PD,PE	Vdd = 3.0V, V_{OH} = 0.7*Vdd
		0.4	-	-			Vdd = 1.5V, V_{OH} = 0.7*Vdd
Output Sink Current (I/O)	I_{OL}	4.0	-	-	mA		Vdd = 3.0V, V_{OL} = 0.3*Vdd
		1.0	-	-			Vdd = 1.5V, V_{OL} = 0.3*Vdd
Output High Current (Buzzer)	I_{OH}	8.0	-	-	mA	PD[1:0]	Vdd = 3.0V, V_{OH} = 0.7*Vdd
		2.0	-	-			Vdd = 1.5V, V_{OH} = 0.7*Vdd
Output Sink Current (Buzzer)	I_{OL}	10.0	-	-	mA		Vdd = 3.0V, V_{OL} = 0.3*Vdd
		3.0	-	-			Vdd = 1.5V, V_{OL} = 0.3*Vdd
LCD Bias Voltage	VLCD	-5%	3.0	+5%	V	VLCD	1/2 bias At 25 deg and -5.4mv/℃
			3.0~4.5				1/3 bias At 25 deg and -8.1mv/℃
			4.0~6.0				1/4 bias At 25 deg and -10.8mv/℃
			5.0~6.25				1/5 bias At 25 deg and -13.5mv/℃
Pull low Resistance	R_{PL}	-	150	-	Kohm	PA,PB,PC, PD,PE	VDD=1.5V
		-	60	-			VDD=3.0V
High Frequency	F_H	-20%	225	+20%	kHz		Clock select as 225kHz
		-	500	-			Clock select as 500kHz
			1000				Clock select as 1000kHz
			1800				Clock select as 1800kHz
			4000				Clock select as 4000kHz
Low Frequency	F_L	-20%	30.72	+20%	kHz		Low speed clock select as IOSC30K
		-	32768	-		X32I,X32O	Low speed clock select as XTAL32K
Operating Current	I_{OP}	-	30	-	uA		High Frequency =225kHz, CPU on, LCD on, no load (VDD=3.6V)
		-	600	-	uA		High Frequency =4000kHz, CPU on, LCD on, no load (VDD=3.6V)
Halt Current	I_{HALT}	-	8	-	uA		Low Frequency active, CPU off, LCD on, no load(VDD=3.6V)

Characteristics	Symbol	Limit			Unit	Terminal	Test Condition
		Min.	Typ.	Max.			
Standby Current	I_{STBY}	-	1.0	1.5	uA		Clock is stopped, LCD off(VDD=3.6V)

7. APPLICATION CIRCUITS



Note1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GPL086A -NnnV - C	Chip form

Note1: Code number (NnnV) is assigned for customer.

Note2: Code number (N = A-Z or 0-9, nn=00-99); version (V = A - Z)

9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
Aug. 26, 2016	1.1	1. Add T_A = 25℃ in section 6.2 headline.	9
		2. Remove Celsius 50 degrees condition for Halt mode current in section 6.2 DC characteristics.	9
		3. Modify Standby Current Characteristics in section 6.2 DC Characteristics	9
		4. Remove Celsius 50 degrees condition for Standby current in section 6.2 DC characteristics.	9
Mar. 05, 2013	1.0	Feature modified;	3
		PAD assignment removed;	5
		DC characteristics modified;	9
OCT. 12, 2010	0.1	Original	14