DATA SHEET

GPL08A6

LOW VOLTAGE 4KB LCD CONTROLLER

Aug 04, 2016

Version 1.2

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LOW VOLTAGE 4KB LCD CONTROLLER

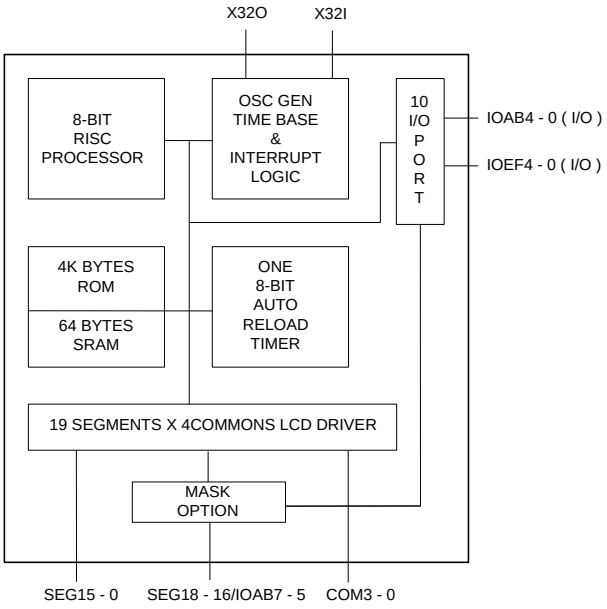
1. GENERAL DESCRIPTION

The GPL08A6, a CMOS 8-bit single chip microprocessor, is designed for low power applications. With only one battery (1.5V), it is capable of processing remarkable LCD graphics. By adopting advanced processing technology, it contains RAM, ROM, I/Os, an interrupt controller, and a LCD display controller/driver, all in one compact package. In GPL08A6, a software controllable standby switch is built-in to save the power.

2. FEATURES

- Built-in 8-bit RISC processor
- 64-byte SRAM
- 4K-byte ROM
- CPU frequency: 0.3 and 0.6MHz @ 1.5V (code option)
  (determined by VDD)
- Built-in RC oscillator
- Built-in 32.768KHz oscillator circuit for real clock function
- Watchdog mode (1Hz or 0.5Hz)
- One 8-bit timer
- Low operating voltage: 1.2V - 1.7V
- Rather low standby current
  In standby mode: I_{STBY} < 1μA
- LCD matrix: 19 - 16 segments, 4 commons
- 10 general I/O pins (segment 16, 17, 18 can be defined as I/O)
- LCD 1/2, 1/3 bias, 1/2, 1/3, 1/4 duty
- Provides 5 INT sources
- Power down mode
  (Wakeup sources: key input, 2Hz, 16Hz, timer)

3. BLOCK DIAGRAM



Note: SEG18 - 16 can be mask option for IOAB7 - 5. The mask option can be defined as one I/O for one segment.

4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
SEG18 - 15 SEG14 - 4 SEG3 - 0	27 - 24 22 - 12 10 - 7	O	LCD driver segment output. SEG18 - 6 can be mask option for IOAB7 - 5.
COM3 - 2 COM1 - 0	42 - 43 1 - 2	O	LCD driver common output.
IOAB4 - 0	32 - 28	I/O	I/O port.
IOEF4 - 0	33 - 37	I/O	I/O port (also for key wake input).
RESET	40	I	System reset input.
X32I	38	I	32.768KHz crystal input (provide LCD frequency).
X32O	39	O	32.768KHz crystal output.
TEST	41	I	Test input.
VDD	11	I	Power input.
VSS	23	I	Ground input.
V3 V45	3 4	I	Inputs for setting LCD bias.
CUP1 CUP2	5 6	I	Inputs for setting LCD bias.

5. FUNCTIONAL DESCRIPTIONS

5.1. ROM Area

The GPL08A6 provides 4K-byte ROM with a LCD driver which is capable to control 4 commons and 19 segments. (Basically, the available ROM for users is 3.75K bytes and the other 0.25K byte of ROM is for test program.)

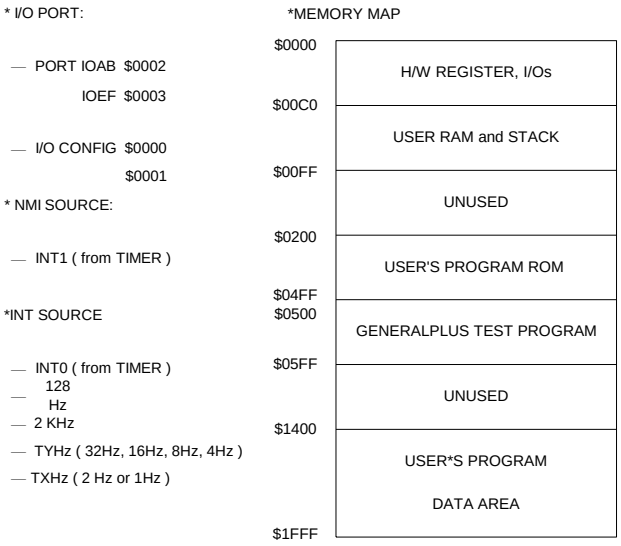
5.2. Stop Clock Mode

The GPL08A6 provides a power saving mode for those applications required very low standby current. Users can simply enable the wakeup sources to stop the CPU clock by writing the STOP CLOCK Register ($09). Thus, CPU will go to standby mode and the RAM and I/Os remain in their previous states until it wakes up. There are three wake-up sources in the GPL08A6: Port IOEF, TIMER, and 2 Hz or 16Hz. After the GPL08A6 wakes up, the internal CPU will go to the next state of sleep. The wakeup action will not affect RAM and I/Os.

5.3. LCD Controller

The GPL08A6 contains a LCD driver, which is capable of controlling 4 commons and 19 segments. In normal operation, the segments send data to LCD port from RAM buffer, and segment 16, 17, 18 can be used as I/O port. The LCD driver of the GPL08A6 is designed to fit most LCD specifications. It can either be programmed as 1/2 or 1/3 bias. The duty is also programmable as 1/2, 1/3 or 1/4 duty.

5.4. Map of Memory and I/Os



5.5. Timer/Counter

The GPL08A6 contains an 8-bit timer. In the timer mode, TMA is a re-loadable up-counter. The timer will automatically be reloaded to the user's preset value and up count again.

The clock source of the timer can be selected as the following:

Timer/Counter		Addr.	Clock Source
TMA	8-BIT TIMER	$0025	CPU CLOCK (T) or CLK32K (32768Hz or CPU clock / 8)

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

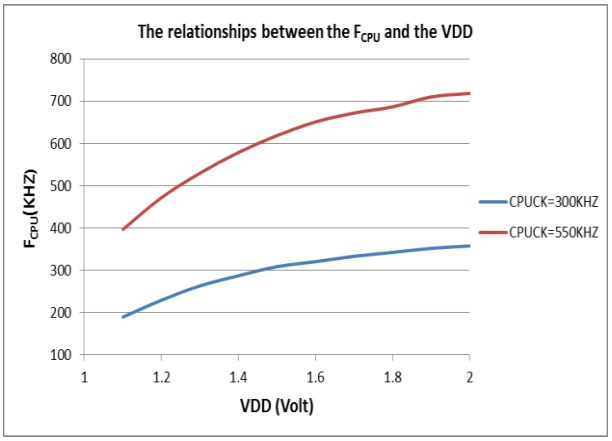
Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 1.7V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

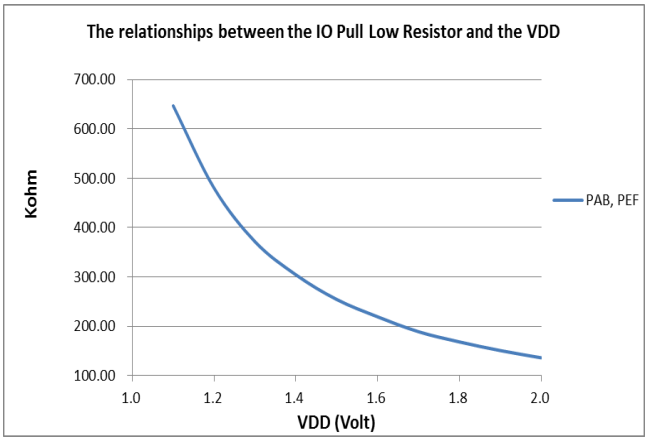
6.2. DC Characteristics (VDD=1.5V, T_A=25℃, unless otherwise specified)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	1.2	-	1.7	V	-
Halt Current 1	I_{HALT1}	-	3.0	-	μA	F_{CPU} = 0.3MHz @ 1.5V No load use 32768Hz crystal
Halt Current 2	I_{HALT2}	-	16	-	μA	F_{CPU} = 0.3MHz @ 1.5V No load no use 32768Hz crystal
Operating Current	I_{OP}	-	45	-	μA	F_{CPU} = 0.3MHz @ 1.5V, no load
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 1.5V, 32768 Hz OFF
Input High Level	V_{IH}	1.1	-	-	V	VDD = 1.5V
Input Low Level	V_{IL}	-	-	0.5	V	VDD = 1.5V
Output High Current (I/O)	I_{OH}	-	-1.0	-	mA	VDD = 1.5V V_{OH} = 1.0V
Output Sink Current (I/O)	I_{OL}	-	2.5	-	mA	VDD = 1.5V V_{OL} = 0.5V
CPU Clock	F_{CPU}	-15%	0.3 0.6	+15%	MHz	0.3, 0.6 MHz by code option VDD = 1.5V

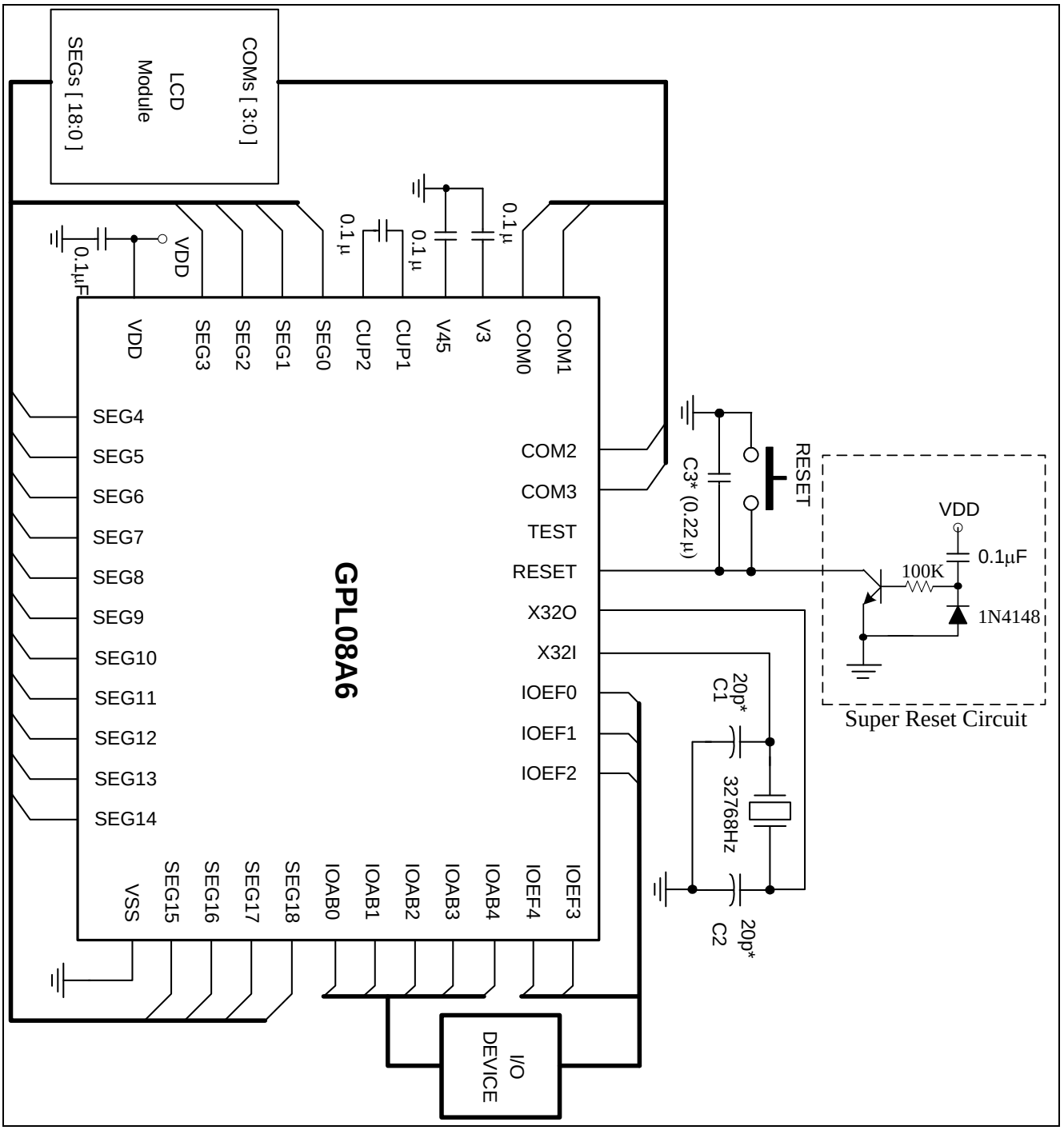
6.2.1. Frequency vs. VDD



6.2.2. IO Pull Low Resistance vs. VDD



7. APPLICATION CIRCUIT



Note: The 0.1µF capacitor between VDD and VSS should be placed to IC as close as possible.

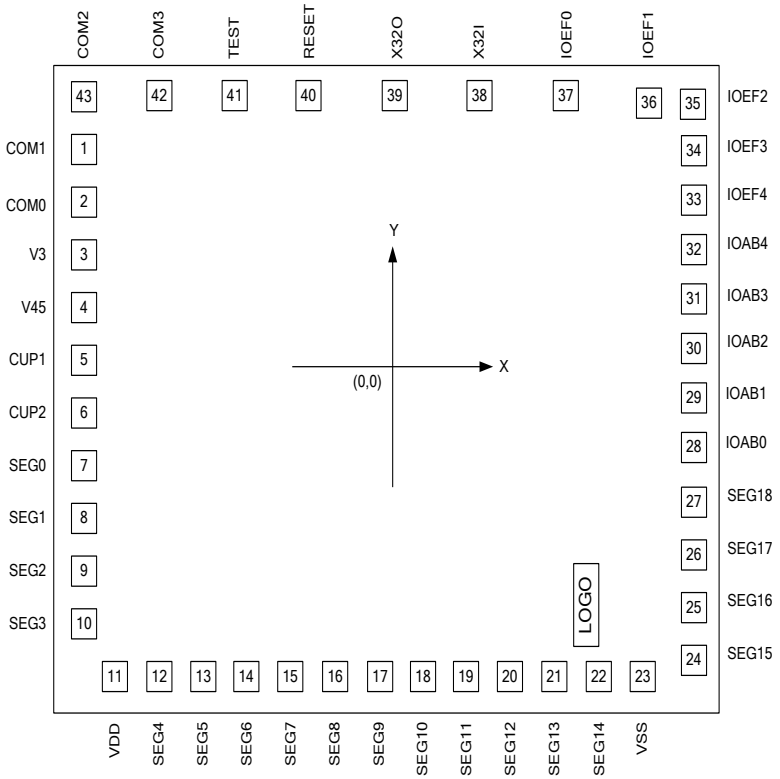
Note*: C1/C2 values in above application circuit are for design guidance only. Different capacitor values may be required for different crystal used. Usually, the values of C1/C2 are in the range 12~20pF.

Note*: C3 value in above application circuit is a typical value for design guidance only.

Note: Super reset circuit is able to prevent the voltage level from brown out which may further lead CPU run into unstable state.

8. PACKAGE/PAD LOCATIONS

8.1. PAD Assignment



This IC substrate should be connected to VSS

Note: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

8.2. Ordering Information

Product Number	Package Type
GPL08A6 - NnnV - C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
Aug 04, 2016	1.2	Add super reset application circuit in section 7	7
Feb 17, 2016	1.1	1. Modify 2. FEATURES 2. Modify 6.2 DC Characteristics 3. Modify 7 APPLICATION CIRCUIT	3 6 7
Aug 07, 2015	1.0	Generating GPL08A6 Data Sheet	10