DATA SHEET

GPL11B

8K-BYTE OTP MICRO-CONTROLLER WITH LCD DRIVER

MAR. 21, 2012

Version 1.4

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8K BYTES OTP MICRO-CONTROLLER WITH LCD DRIVER

1. GENERAL DESCRIPTION

Generalplus GPL11B is a CMOS 8-bit single chip Micro-controller containing LCD drivers, one-time programmable (OTP) ROM, SRAM, I/O, timer/counter, PLL/ROSC, audio/remote control out, and resistor to frequency converter (RFC) function, all in one chip. The GPL11B is designed to drive LCD directly and perform efficient controller function as well as arithmetic function. With on-chip crystal oscillator, the real-time clock can be easily achieved. For power savings, several power-down modes are controllable by software. The GPL11B is widely used for low power electronic products, e.g. remote controller and general-purpose LCD controller. For more information about how to program GPL11B OTP chip, please refer to ***Generalplus OTP/MTP Writer User's Manual.***

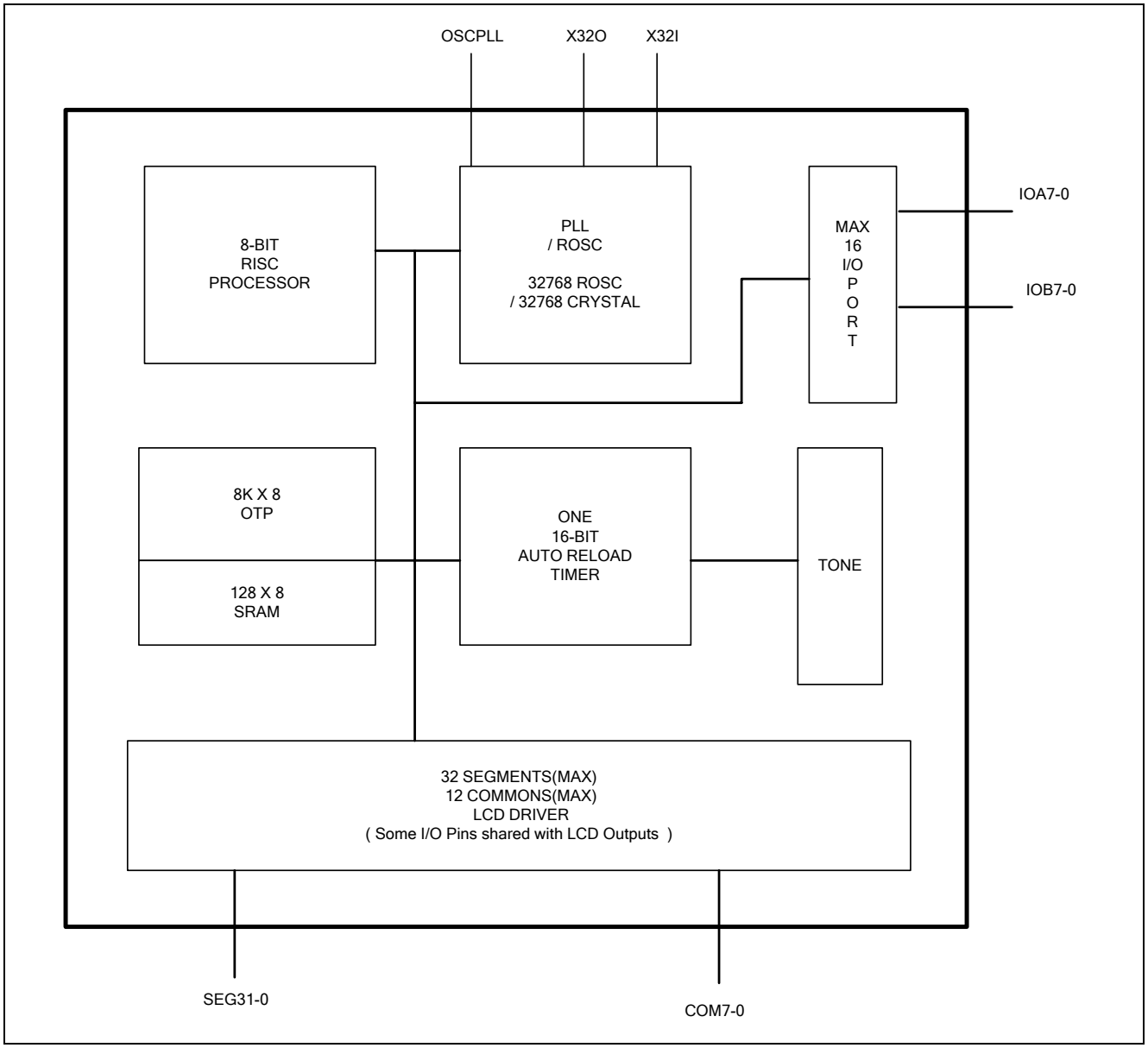
2. FEATURES

- Built-in Generalplus 8-bit CPU
  - 128-byte SRAM
  - 8K-byte OTP
  - Working Voltage 2.4V ~ 5.5V (low voltage reset is disabled), 2.6V ~ 5.5V (low voltage reset is enabled)
  - Maximum CPU speed 4MHz @ 2.4V
  - CPU clock can be switched between High-Speed clock (PLL / R-oscillator) divided by 2 / 4 / 8 / 16 or Low-speed clock (32768Hz Crystal-oscillator / 32768 R-oscillator)
  - Watchdog timer and illegal address reset circuit are always enabled and will reset CPU if these events occur
  - Eight wakeup sources (37.9K/N, 32768/N, TMO, EXT1, EXT2, T2Hz, KEYC, NMI)
  - Eight interrupt sources
- Dual clock sources:
  - Dual clock sources are controlled by two clock option pins
  - High-Speed clock sources: PLL/R-oscillator
  - Low-speed clock sources: 32768 Crystal / 32768 R-oscillator
  - PLL clock = 4.85MHz
  - IR carrier frequency = 37.9KHz
  - Maximum system clock in PLL clock mode = 2.42MHz
- Programmable LCD driver
  - 48 byte Dual-port SRAM for LCD buffers
  - LCD has 1/2 bias, 1/3 bias, 1/4 bias selections
  - Maximum LCD 12x30 (360 dots), 11x30 (330 dots), 10x30 (300 dots), 9x32 (288 dots), 8x32 (256 dots), 5x32 (160 dots), 4x32 (128 dots), 3x32 (96 dots)
- A 16-bit re-loadable timer/counter
- Low voltage reset level is at 2.4V and can be disable by LVROFF pin
- Four Operating modes: Operating / WAIT / HALT /STANDBY
  - Interrupt will wake CPU up
  - Wakeup from CPU reset or next instruction is programmable
- Built-in RFC (Resistor to Frequency Converter) function
- I/O Port definition:
  - 8 IOA, 4 shared pins with LCD Commons / Segments
  - 8 IOB with key wakeup function, 5 shared pins with LCD Commons / Segments / V3 / CUP3 / CUP4
- Five Reset flags: watchdog, error address, power-on, external reset, and low voltage
- Low Power consumption:
  - Operating current < 1mA @ 3.0V, CPU runs at 1.2MHz, 4.85MHz, PLL on
  - Operating current < 500μA @ 3.0V, CPU run 1MHz, 2MHz, ROSC on
  - Operating current < 20μA @ 3.0V, CPU run 32KHz, 32768 crystal on, PLL off
  - Halt current < 2μA @ 3.0V, 1/8 duty, no load, 32768 crystal & LCD on, PLL & CPU off
- Serial OTP programming interface

  Needs only 7 pins for OTP programming: VDD, VSS, VPP, TEST, PIEP, SCK (SEG14), SDA (SEG13)

Note*: EV-board can not emulate IOB's output function.

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

4.1. PIN Description

Mnemonic	PIN No.		Type	Description
	QFP80	LQFP80		
SEG27 - 21 SEG20 - 6 SEG5 - 0	13 - 19 25 - 39 44 - 49	11 - 17 23 - 37 42 - 47	O	LCD driver segment output SEG13 shared pin with OTP programming interface SDA SEG14 shared pin with OTP programming interface SCK
COM4_SEG31	9	7	O	Shared pin for LCD common4 or segment31
COM5_SEG30	10	8	O	Shared pin for LCD common5 or segment30
COM6_SEG29	11	9	O	Shared pin for LCD common6 or segment29
COM7_SEG28	12	10	O	Shared pin for LCD common7 or segment28
COM3 - 0	50 - 53	48 - 51	O	LCD driver common output
V1 V2	54 55	52 53	I	Inputs for setting LCD bias
CUP1 CUP2	56 57	54 55	I	Inputs for setting LCD bias
IOA7	72	70	I/O	IOA port bit7, can be used to output IR carrier
IOA6	73	71	I/O	IOA port bit6, can be used to output tone
IOA5	74	72	I/O	IOA port bit5, shared pin with LCD common8 In RFC application, used as a pass-through (output) pin and connected to sensor
IOA4	75	73	I/O	IOA port bit4, shared pin with LCD common11 In RFC application, used as a pass-through (output) pin and connected to sensor
IOA3	76	74	I/O	IOA port bit3, shared pin with LCD segment29 In RFC application, used as a pass-through (output) pin and connected to sensor
IOA2	77	75	I/O	IOA port bit2, shared pin with LCD segment28
IOA1	78	76	I/O	IOA port bit1, Timer external input 2, External Interrupt input 2 In RFC application, used as input-floating pin and connected to sensor & capacitor
IOA0	79	77	I/O	IOA port bit0, Timer external input 1, External Interrupt input 1
CUP3_IOB7	58	56	I/O	Shared pin for (1) IOB port bit7 with key-change detection (2) Input for setting LCD bias (CUP3)
CUP4_IOB6	59	57	I/O	Shared pin for (1) IOB port bit6 with key-change detection (2) Input for setting LCD bias (CUP4)
V3_IOB5	65	63	I/O	Shared pin for (1) IOB port bit5 with key-change detection (2) Input for setting LCD bias (V3)
IOB4	8	6	I/O	Shared pin for (1) IOB port bit4 with key-change detection (2) LCD segment 31 (3) LCD common 10
IOB3	7	5	I/O	Shared pin for (1) IOB port bit3 with key-change detection (2) LCD segment 30 (3) LCD common 9
IOB2	6	4	I/O	IOB port bit2 with key-change detection
IOB1	5	3	I/O	IOB port bit1 with key-change detection
IOB0	4	2	I/O	IOB port bit0 with key-change detection
LVROFF	3	1	I	LVR (Low-voltage reset) disable pin
NC	20	18	P	No connection
VPP	21	19	P	OTP programming power. Should left floating or connect to VSS in normal operating mode

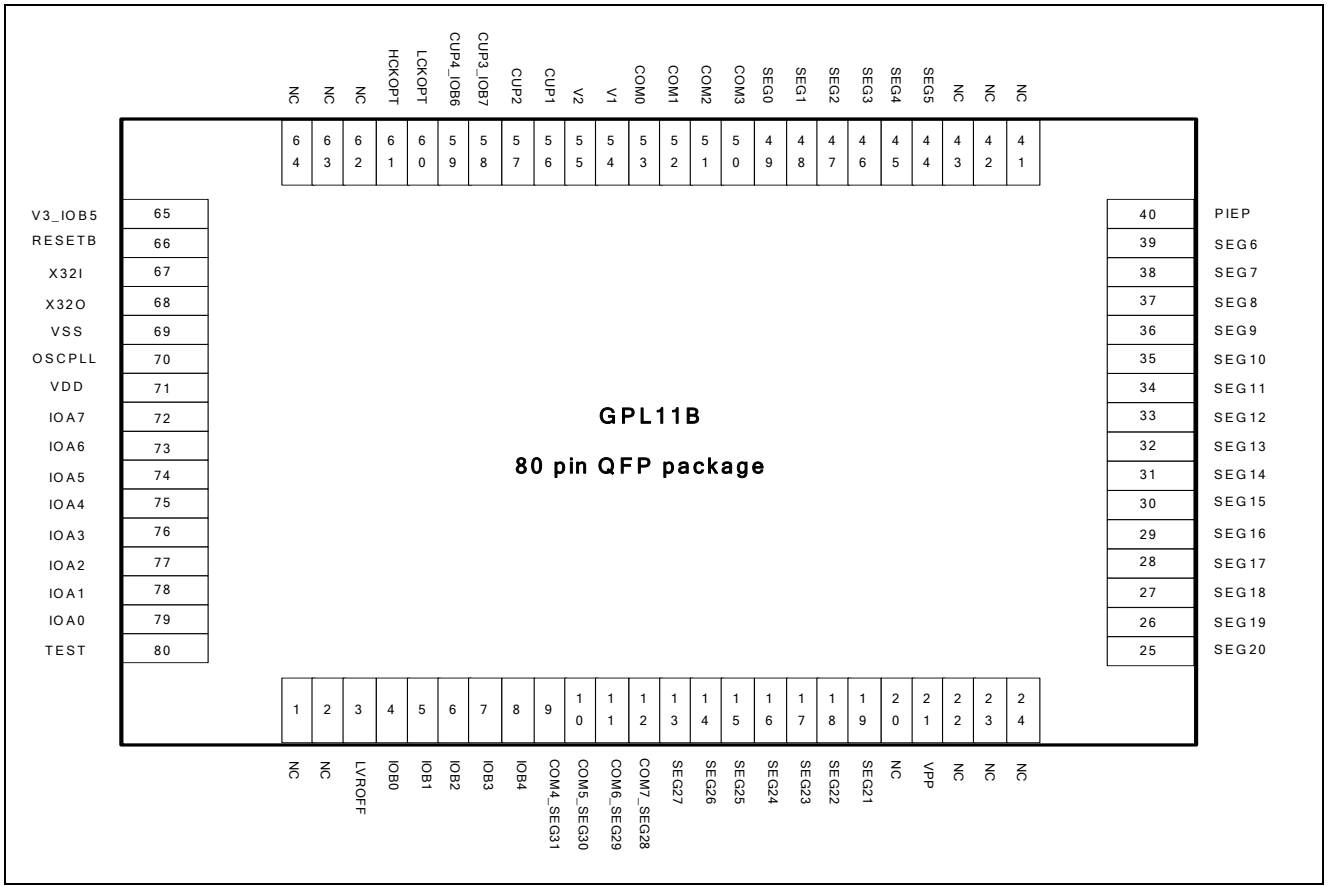
Mnemonic	PIN No.		Type	Description
	QFP80	LQFP80		
PIEP	40	38	I	OTP programming interface enable
X32I	67	65	I	32.768KHz Crystal/R-OSC Input (option)
X32O	68	66	O	32.768KHz crystal output
LCKOPT	60	58	I	Option pin for Low-speed clock selection 0: 32768 crystal; 1: 32768 R-oscillator
HCKOPT	61	59	I	Option pin for high-speed clock selection 0: R-oscillator; 1: 4.85MHz PLL
RESETB	66	64	I	External reset input pin (Low active)
VSS	69	67	P	Ground input
OSCPLL	70	68	I	PLL Input/R-OSC Input (option)
VDD	71	69	P	Power input
TEST	80	78	I	Test input

Legend: I = Input, O = Output, P = Power

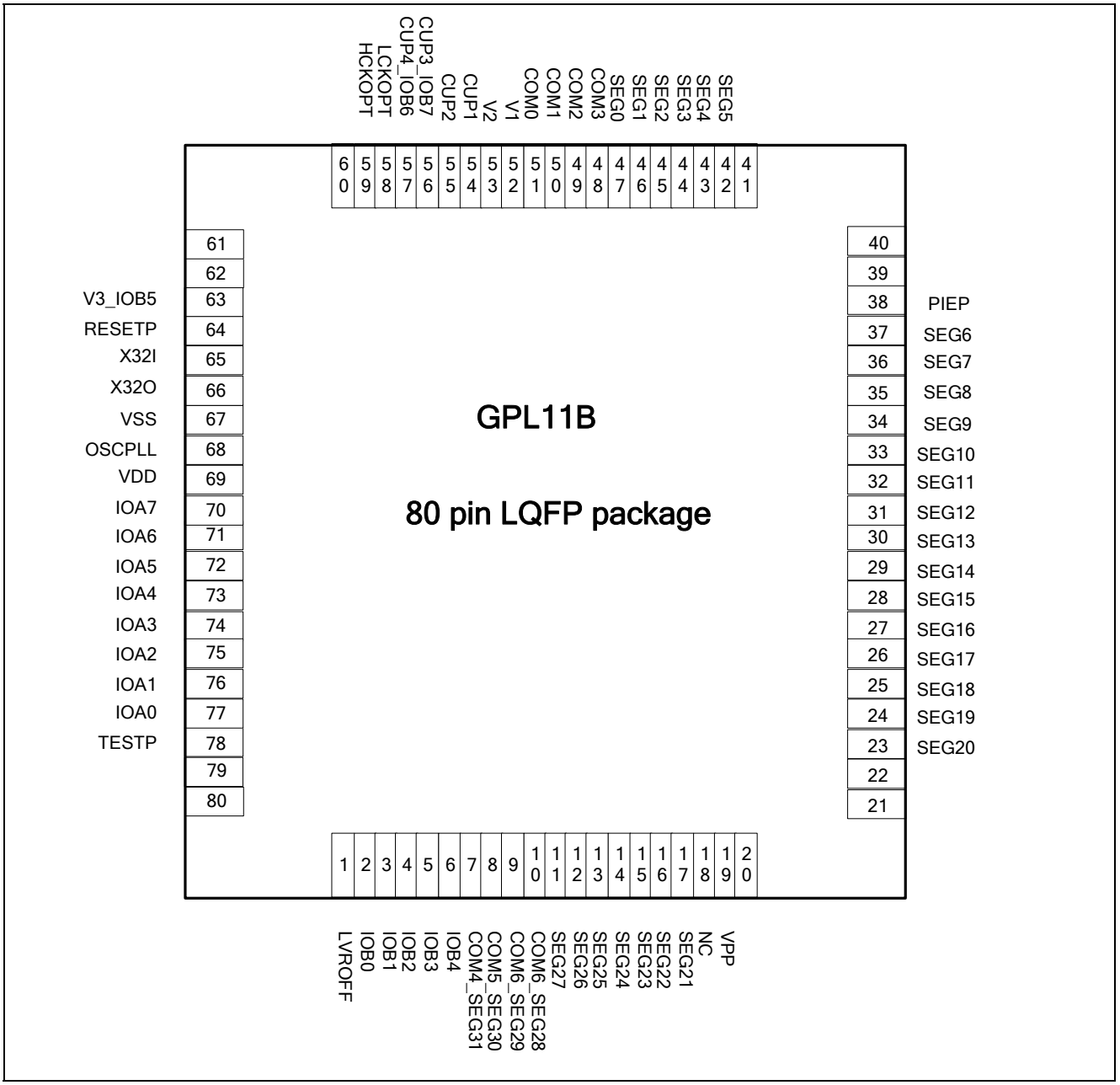
Total 69 pins

4.2. PIN Assignment

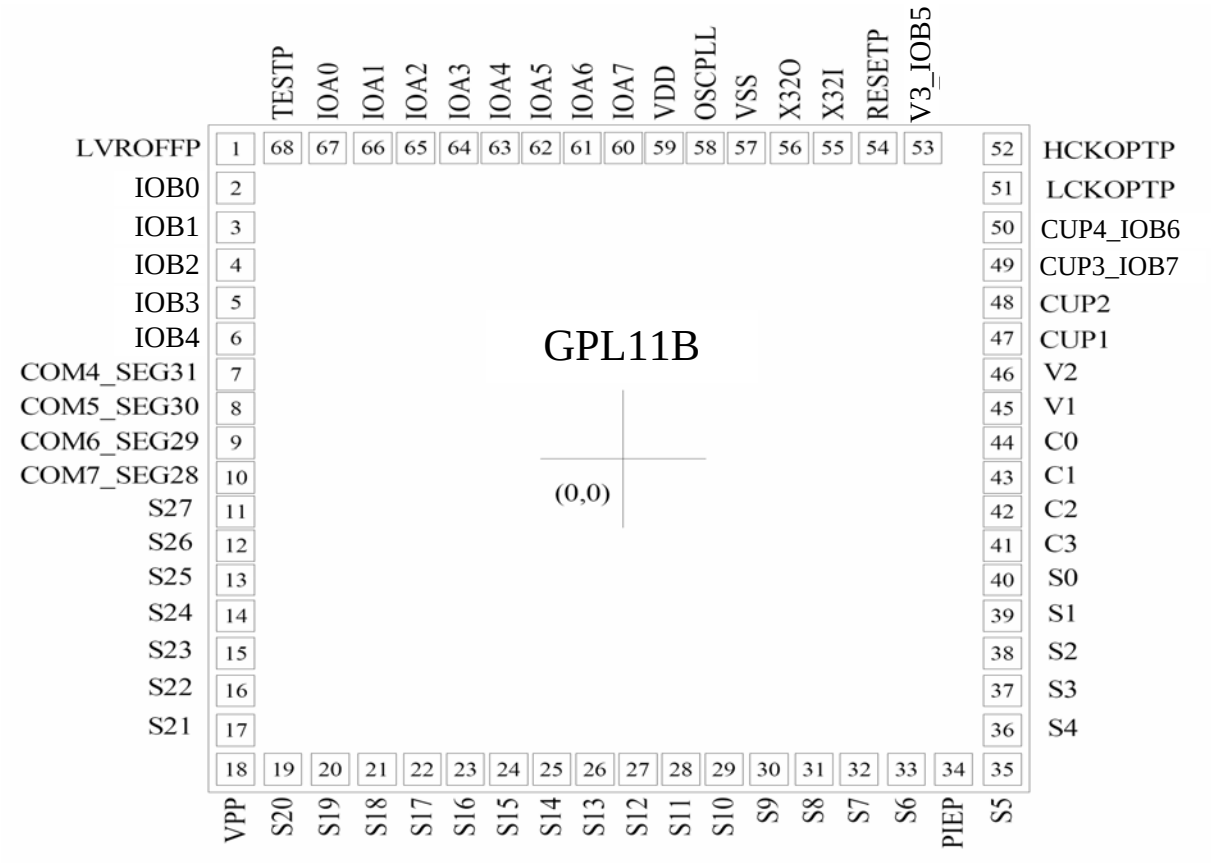
4.2.1. 80 pin QFP



4.2.2. 80 pin LQFP



4.3. PAD Assignment



This IC substrate should be connected to VSS or floated

Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

5. FUNCTION DESCRIPTIONS

5.1. Map of Memory and I/Os

$00 ~ $1F	Control Port
$50 ~ $7F	48 Byte LCD RAM
$80 ~ $FF $1E0 ~ $1FF	128 Byte SRAM
$200 ~ $3FF	Reserved
$400 ~ $DFFF	Reserved
$E000 ~ $FFFF	OTP

Note:

1. 512 bytes testing program ROM: $400 ~ $5FF
2. $0080 ~ $00FF maps to the 128 bytes SRAM, and $01E0 ~ $01FF also maps to $E0 ~ $FF (maximum stack is 32 byte)
3. Illegal address range: $0020 ~ $004F, $0100 ~ $01DF, $0200 ~ $03FF $0400 ~ $DFFF

5.2. Clock Sources Control

There are two groups of clock sources controlled by two clock option pins: (1) High-speed clock source: PLL / ROSC (2) Low-speed clock source: 32768Hz R-oscillator / Crystal oscillator.

5.2.1. Clock sources combination

	HCKOPT	LCKOPT	
ROSC/C32K	0	0	
ROSC/R32K	0	1	
PLL/C32K	1	X	Note1

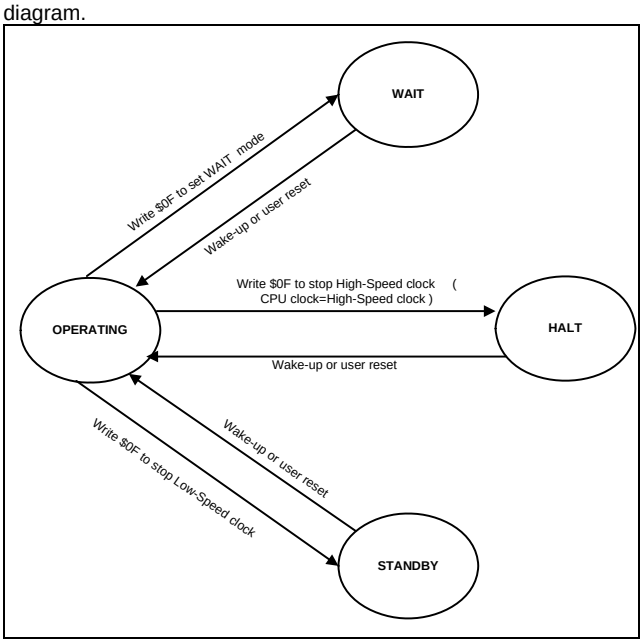
Note1: No PLL/R32K combination, it is mapped to PLL/C32K mode.

5.2.2. Switching of CPU clock

CPU clock is programmable as (1) high-speed clock / 2 / 4 / 8 / 16 or (2) 32768Hz.

5.3. Operation Modes

There are four operation modes involved in GPL11B - standby, halt, wait and operating. The following figure is the GPL11B state diagram.



The following table summarizes the differences between these modes.

	Operating	Wait	Halt	Standby
CPU clock	ON	OFF	OFF	OFF
PLL/Oscillator	ON	ON	OFF	OFF
32768 crystal /32768 oscillator	ON	ON	ON	OFF

5.3.1. Operating mode

In operating mode, all functions (CPU, PLL/R-oscillator, 32768 crystal/32768 oscillator, timer/counter, LCD driver…) are activated. In general, this mode consumes the highest power.

5.3.2. Wait mode

In wait mode, CPU clock halts and waits for an event (key-change, timer overflow…) to wake up. In addition to CPU stop, all other resources are still working. This mode consumes less power than all other activated peripherals except CPU.

5.3.3. Halt mode

In halt mode, CPU clock halts and PLL/ROSC clock sources stops, waits for an event (key change, timer overflow…) to wake up. The 32768Hz relevant functions, such as timer/counter and LCD driver, may remain active in halt mode.

5.3.4. Standby mode

The standby mode is a mode that the device is placed in its lowest current consumption state. In standby mode, all functions are turned off. In addition, RAM and I/Os will remain in their previous states.

5.4. LCD Controller/Driver

The GPL11B contains a 360-dot LCD controller/driver that can be configured to specified patterns via programming the LCD Control register. Once the configuration is completed, desired patterns can be displayed by filling data into LCD RAM. The LCD driver supports 1/3 ~ 1/12 duty and 1/2 ~ 1/4 bias, and its LCD frame rate can be adjusted by programming the Port_LCDCK_CTL($11) register in small step between 40 Hz ~ 100 Hz. The LCD controller/driver can still be operating during sleep mode by keeping the 32768Hz oscillator alive.

5.5. Watchdog Timer (WDT)

FPL11B also features an on-chip watchdog timer (WDT) that is designed to recover the system from abnormal operation. If WDT is not cleared within one second, the WDT generates a signal to reset CPU and the WDT is recommended to be cleared every 0.5 seconds via software programming to avoid accidental reset. Note that the WDT only works when 32768Hz clock is activated.

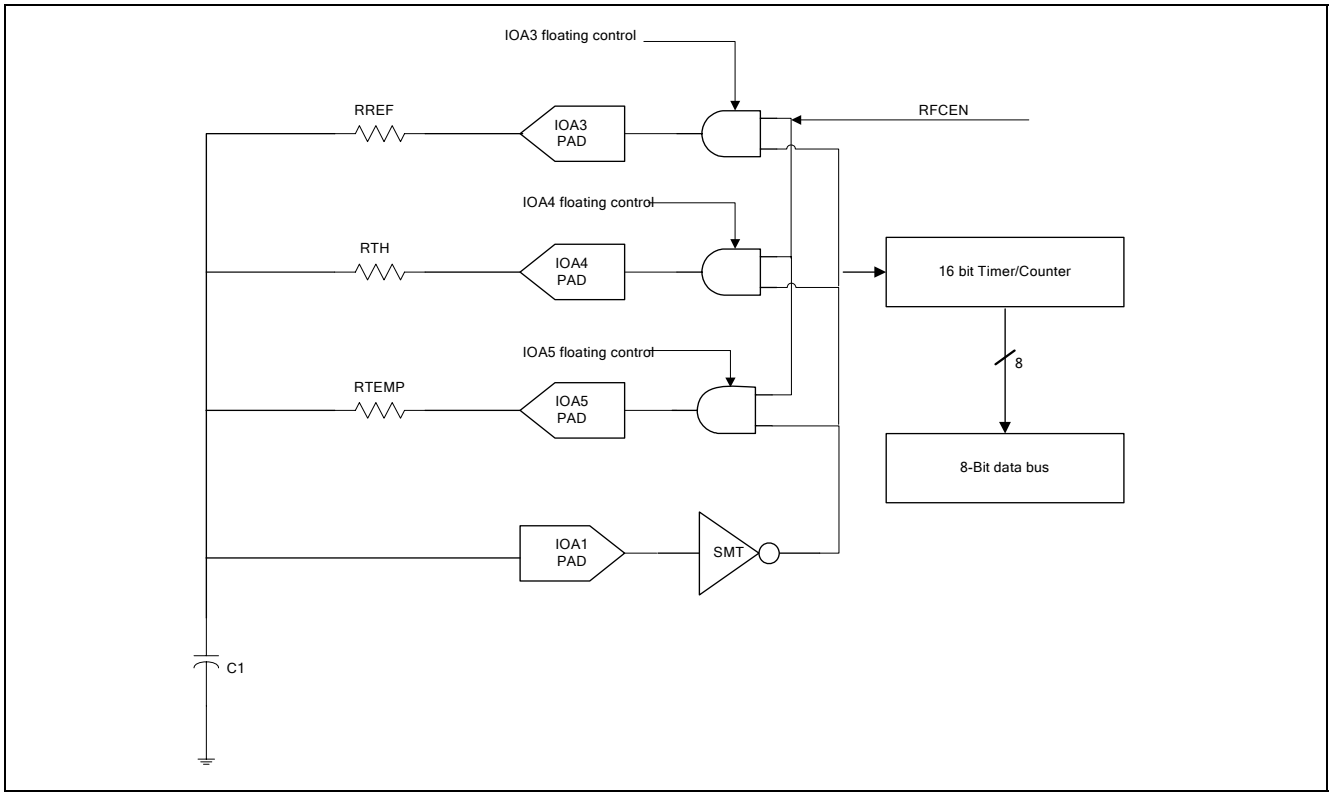
5.6. Wakeup/Interrupt Control

There are eight wakeup sources: 37.9K/N, 32768/N, TMO, EXT1, EXT2, T2Hz, KEYC, and NMI.

Interrupt sources can be used as (1) wake-up source only. (2) both wakeup source and interrupt CPU.

5.7. RFC Function

The RFC (Resistor to Frequency Converter) circuit contains a RC oscillation circuit and a 16-bit timer/counter to calculate the resistance of temperature or humidity sensor relative to reference resistor. The circuit is shown below.



5.8. IR Output Control

In IR-application, we must first use PLL/32768 Hz crystal combination of clock sources to get PLL Freq = 4.85MHz. Next, the 4.85MHz PLL Freq is transmitted to the duty controller to generate 37.9KHz and 1/8 duty resolution IR-output pulse. The 37.9KHz IR-output pulse is delivered t to Port IOA7 and can be controlled by software or Timer-overflow.

5.9. Option Pin

PIN	Description	Comment
HCKOPT	0: ROSC; 1: PLL	
LCKOPT	0: 32768 Hz crystal 1: 32768 Hz oscillator	
LVROFF	0: LVR enable 1: LVR disable	

5.10. Default Status of PINs

IOA (IOA0 ~ IOA7) => Input with pull-low
IOB (IOB0 ~ IOB7) => Input with pull-low
LCD => OFF (Common = Low & Segment = Low)
CUP3_IOB6 = IOB6
CUP4_IOB7 = IOB7
V3_IOB5 = IOB5
COM4_SEG31 = SEG31
COM5_SEG30 = SEG30
COM6_SEG29 = SEG29
COM7_SEG28 = SEG28
IOB3 (SEG30/COM9) = IOB3
IOB4 (SEG31/COM10) = IOB4
IOA4 (COM11) = IOA4
IOA5 (COM8) = IOA5
OSCPLL = ROSC (HCKOPT pin=Low)
X32I/R32I = X32K (LCKOPT pin=Low)

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to + 60℃
Storage Temperature	T_{STO}	-50℃ to + 150℃

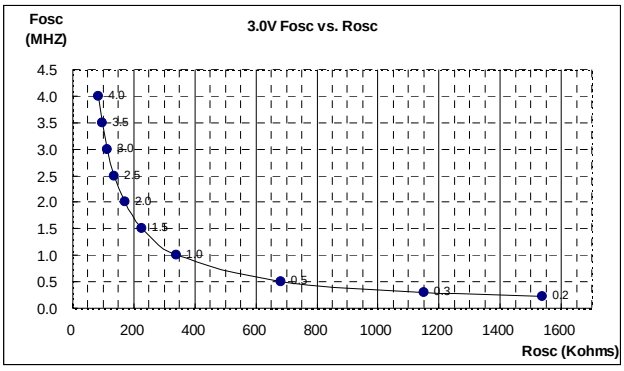
Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

6.2. DC Characteristics

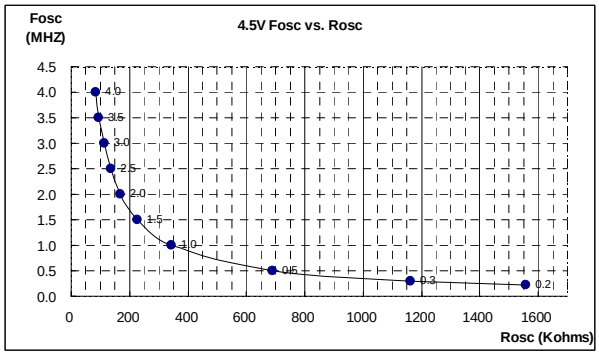
Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	5.5	V	-
Operating Current	I_{OP}	-	-	1.0	mA	VDD = 3.0V, CPU = 1.2MHz, PLL ON
		-	-	500	μA	VDD = 3.0V, CPU = 1.0MHz, 2MHz ROSC ON
		-	-	20	μA	VDD = 3.0V, CPU = 32768, 32768 ON, PLL OFF
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 3.0V, PLL & 32768 OFF
Audio Output Current	I_{AUD}	8.0	-	-	mA	VDD = 3.0V
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High Current	I_{OH1}	2.0	-	-	mA	VDD = 3.0V, VOH = 2.4V, IOA[2:0]
	I_{OH2}	5.0	-	-	mA	VDD = 3.0V, VOH = 2.4V, IOA[7:3]
Output Low Current	I_{OL1}	4.0	-	-	mA	VDD = 3.0V, VOL = 0.8V, IOA[2:0]
	I_{OL2}	8.0	-	-	mA	VDD = 3.0V, VOL = 0.8V, IOA[7:3]
Pull-up Resistor	R_{PU1}	-	120K	-	-	VDD = 3.0V
Pull-down Resistor	R_{PD1}	-	120K	-	-	VDD = 3.0V

6.3. The Relationships between the F_{OSC} and the R_{OSC}

6.3.1. VDD = 3V

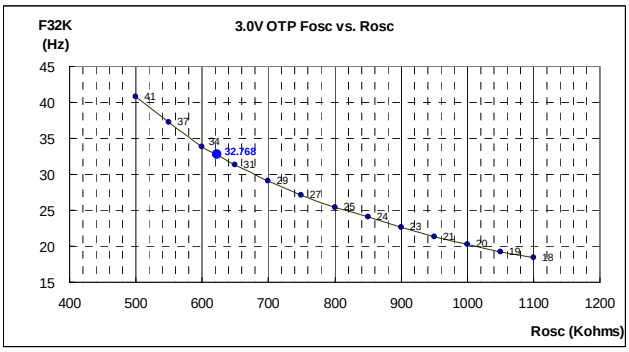


6.3.2. VDD = 4.5V

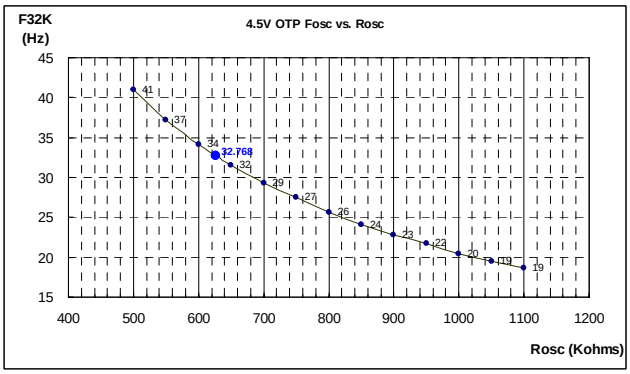


6.4. The Relationships between the Fosc32K and the R_{OSC32K}

6.4.1. VDD = 3V

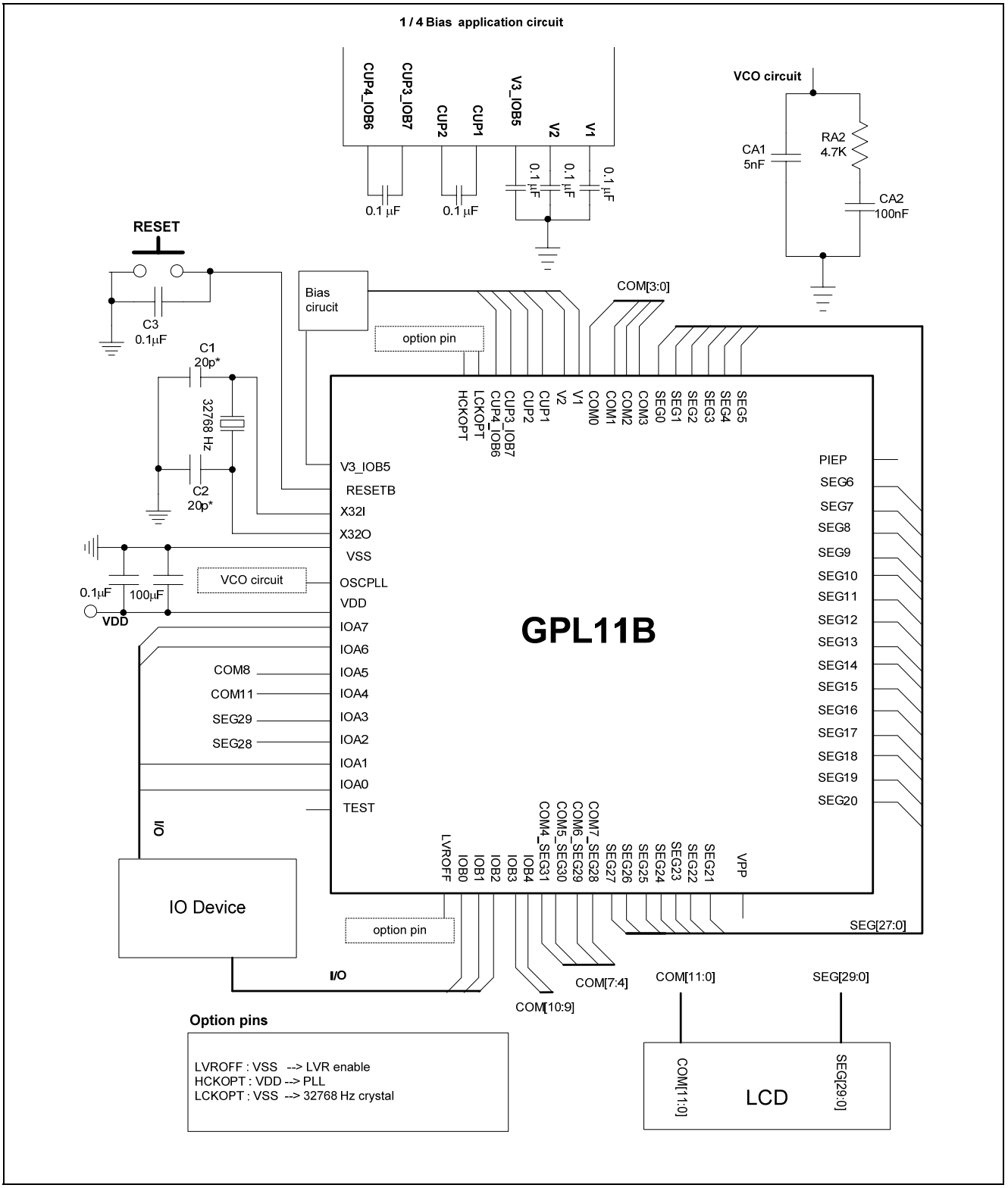


6.4.2. VDD = 4.5V



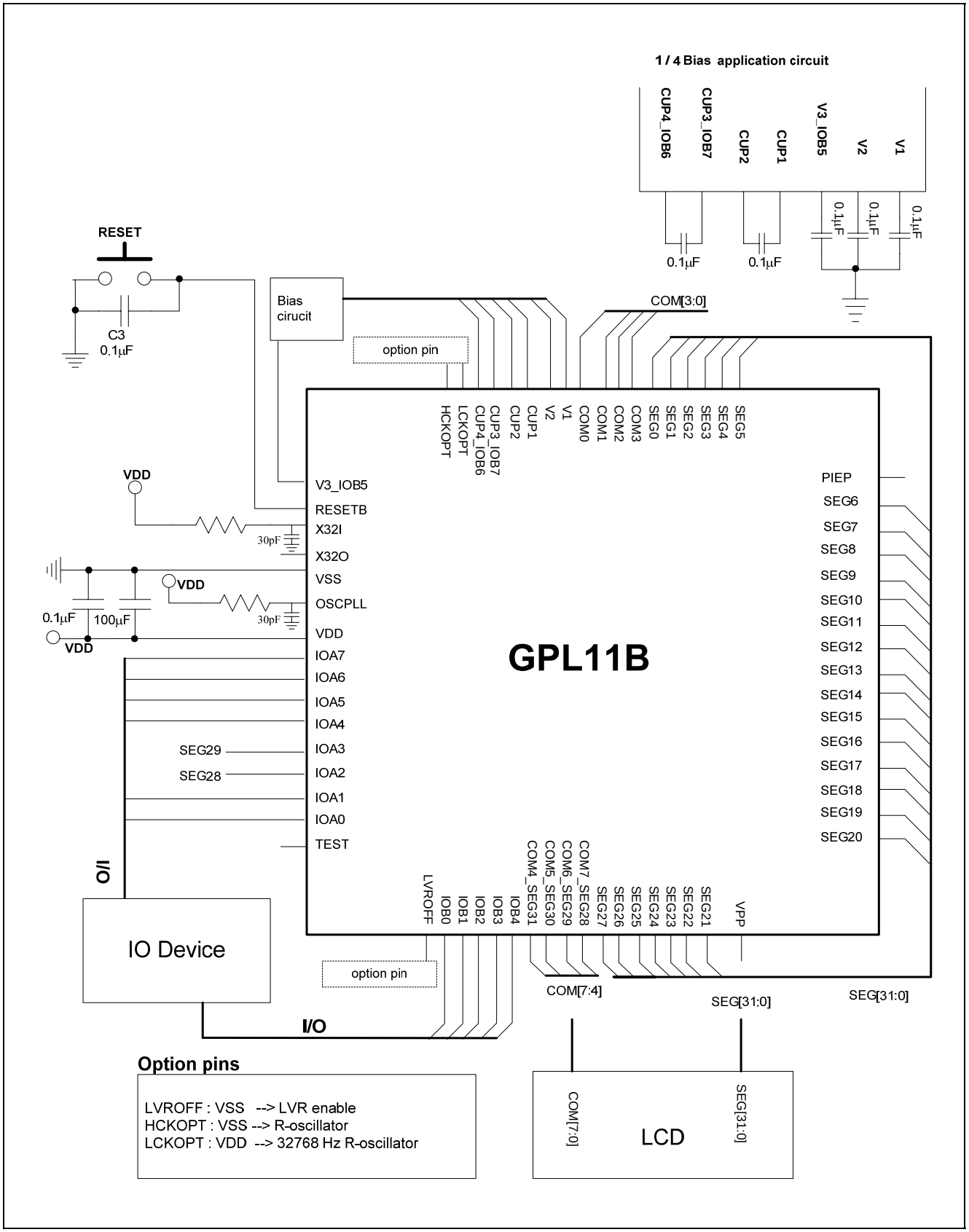
7. APPLICATION CIRCUITS

7.1. 360 Dots (12 x 30) LCD Driver, 1/4 Bias, PLL / 32768Hz Crystal

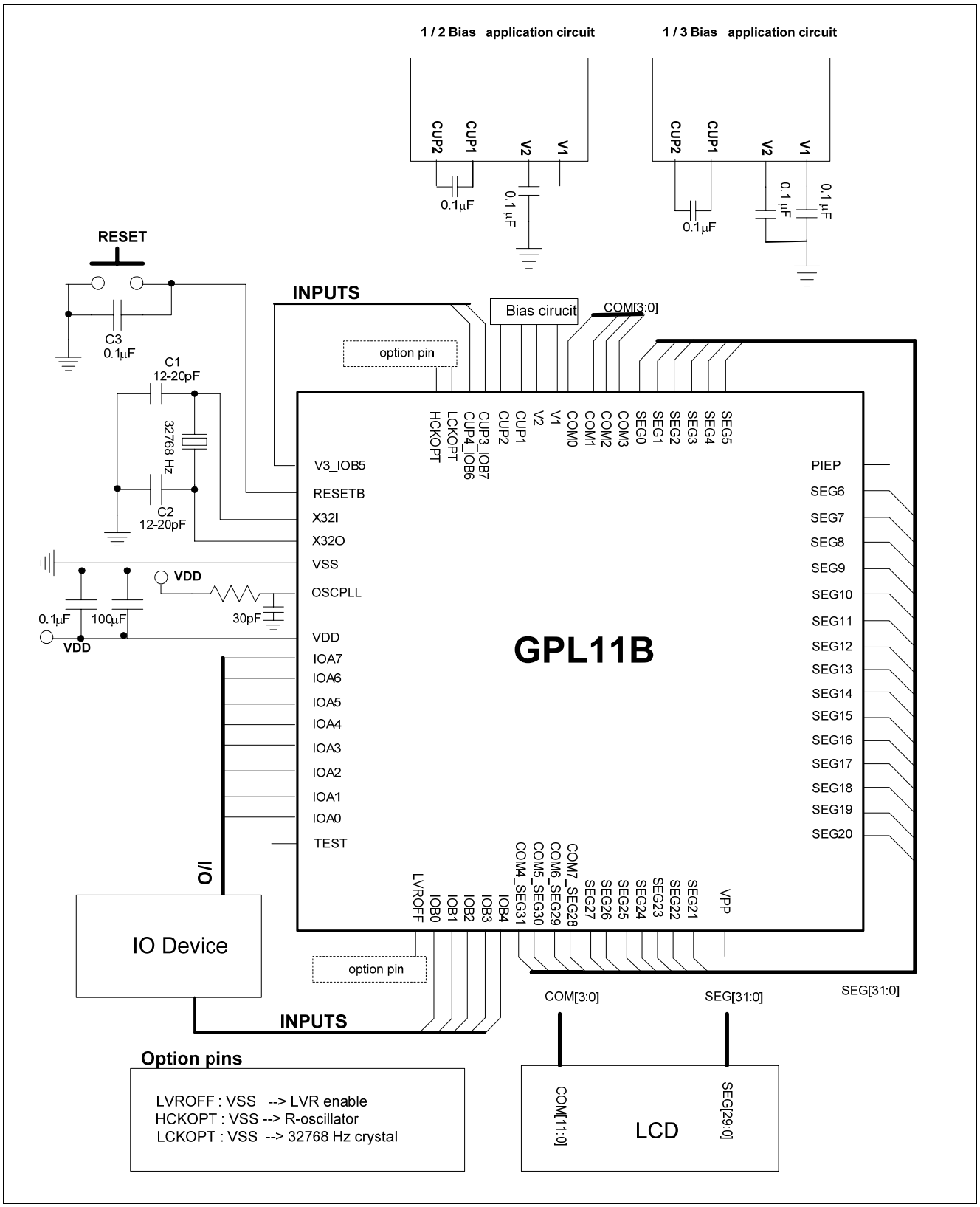


Note*: C1/C2 values in above application circuit are for design guidance only. Different capacitor values may be required for different crystal used. Usually, the values of C1/C2 are in the range 12~20pF.

7.2. 256 Dots (8 x 32) LCD Driver, 1/4 Bias, R-Oscillator / 32768Hz R-Oscillator



7.3. 128 Dots (4 x 32) LCD Driver, 1/2 or 1/3 Bias, R-Oscillator / 32768Hz Crystal



Note*: C1/C2 values in above application circuit are for design guidance only. Different capacitor values may be required for different crystal used. Usually, the values of C1/C2 are in the range 12~20pF.

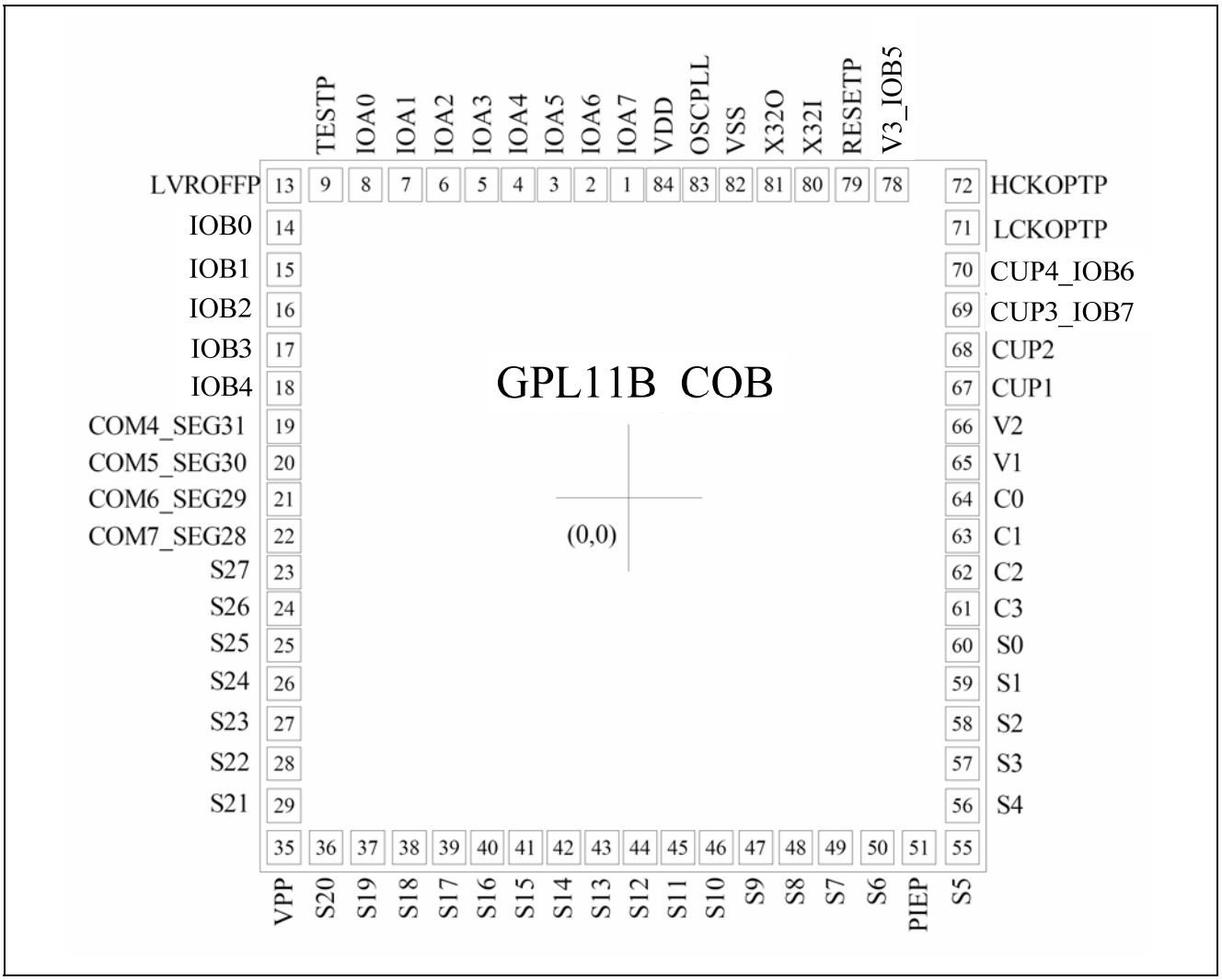
8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GPL11B - C	Chip Form
GPL11B – HQ05x	Package form - 80 pin QFP Green Package
GPL11B - QL04x	Halogen Free 80 pin LQFP Package

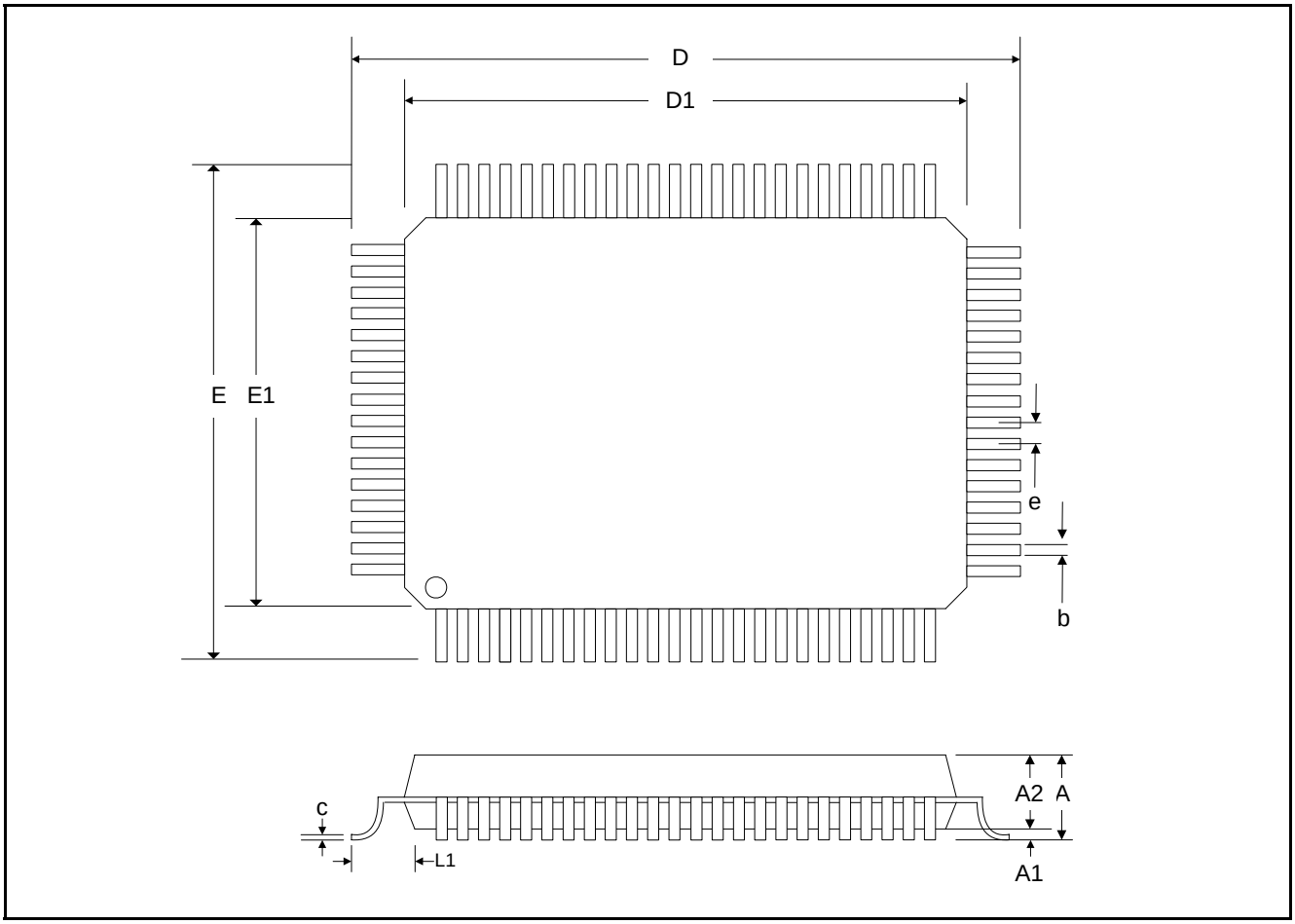
Note: x = 0 - 9, serial number.

8.2. COB Bounding Diagram (84 pin)



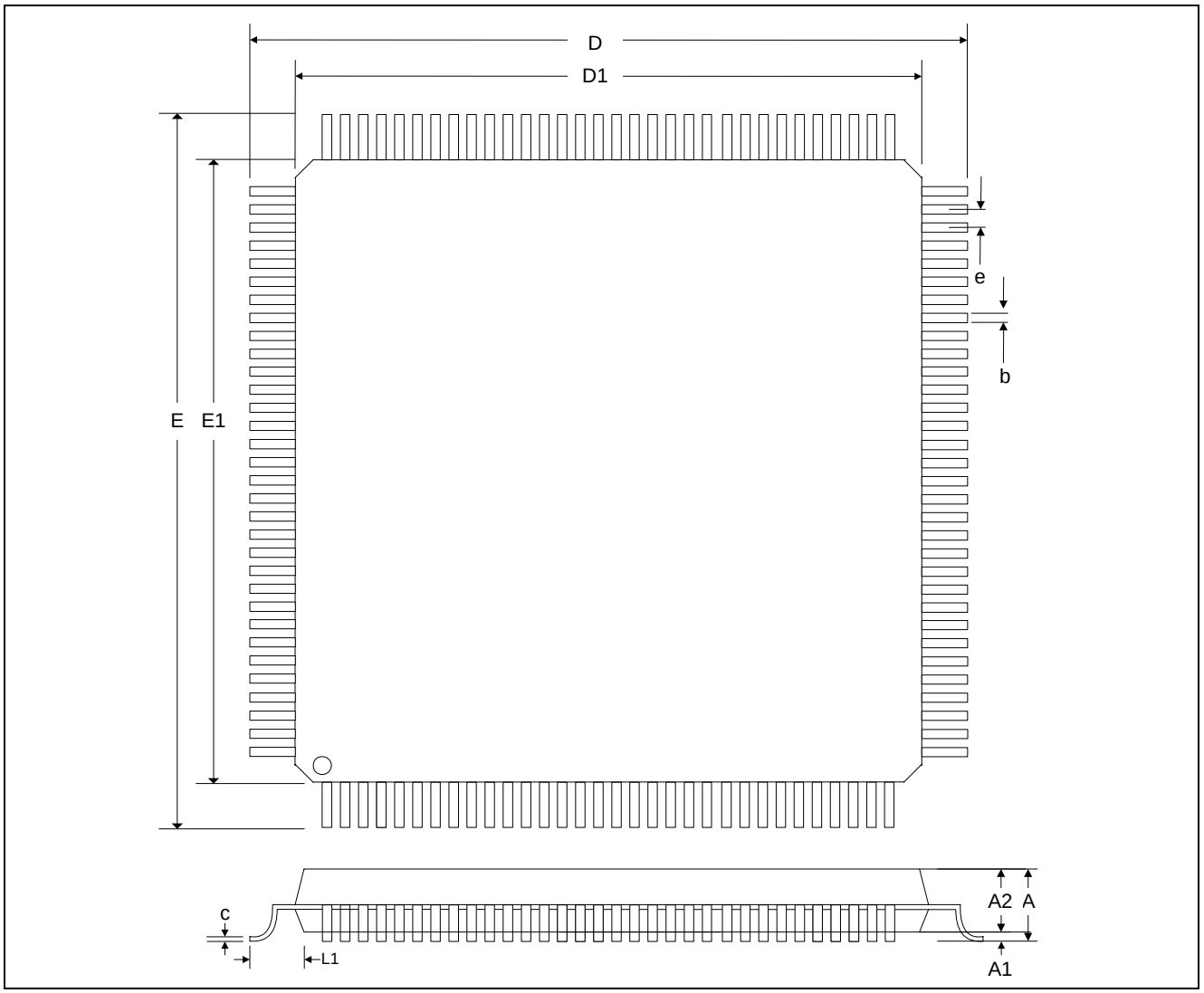
8.3. Package Information

8.3.1. QFP 80L outline dimensions



Symbol	Min.	Nom.	Max.	Unit
A	-	-	3.40	Millimeter
A1	0.25	-	-	Millimeter
A2	2.50	2.72	2.90	Millimeter
D	23.20 REF			Millimeter
D1	20.00 REF			Millimeter
E	17.20 REF			Millimeter
E1	14.00 REF			Millimeter
e	0.80 REF			Millimeter
b	0.30	0.35	0.45	Millimeter
c	0.11	0.15	0.23	Millimeter
L1	1.60 REF			Millimeter

8.3.2. LQFP 80L outline dimensions



Symbol	Min.	Nom.	Max.	Unit
A	-	-	1.60	Millimeter
A1	0.05	-	0.15	Millimeter
A2	1.35	1.40	1.45	Millimeter
D	14.00 BSC.			Millimeter
D1	12.00 BSC.			Millimeter
E	14.00 BSC.			Millimeter
E1	12.00 BSC.			Millimeter
e	0.50 REF			Millimeter
B	0.17	0.20	0.27	Millimeter
c	0.09	-	0.20	Millimeter
L1	1.00 REF			Millimeter

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10. REVISION HISTORY

Date	Revision #	Description	Page
Mar. 21, 2012	1.4	Modify ordering information from GPL11B-QQ05X to GPL11B-HQ05X in section 8.1	17
Sep. 15, 2011	1.3	1. Modify IC substrate connect describe to 'This IC substrate should be connected to VSS or floated'. 2. Modify the relationship between R_{OSC} & F_{OSC}.	8 12,13
Jul. 09, 2008	1.2	1. Modify IOB[7:5], IOB[2:0] type to 'I/O'. 2. "IOA3" in RFC function diagram change to "IOA1".	5 9
May. 28, 2007	1.1	Modify the diagrams in section 8.1 and 8.3.	15, 16
Mar. 29, 2007	1.0	1. Modify the Working Voltage form 3.6V to 5.5V. 2. Add the OTP programming interface descriptions in section 2 and 3.	3, 11 3, 5
Feb. 06, 2007	0.2	1. Pin VDDT deleted. 2. INBx changed to IOBx. 3. Modify the "Option Pin" in section 5.9. 4. Modify the application circuit in section 7.2. 5. Modify the "Ordering Information" in section 8.2. 6. EPROM changed to OTP.	 10 13 15
Sep. 23, 2005	0.1	Original	17