DATA SHEET

GPL12A

8K Bytes Micro-controller with LCD Driver

Jul. 27, 2011

Version 1.4

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8K BYTES MICRO-CONTROLLER WITH LCD DRIVER

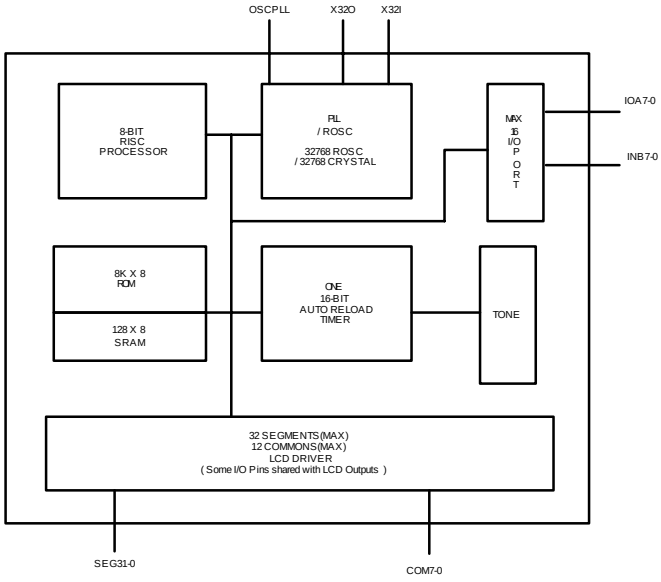
1. GENERAL DESCRIPTION

Generalplus GPL12A is the mask-version of GPL11B(OTP) which features a CMOS 8-bit single chip Micro-controller containing LCD drivers, 8K bytes ROM, SRAM, I/O, timer/counter, PLL/ROSC, audio/remote control out, and resistor to frequency converter (RFC) function, all in one chip. The GPL12A is designed to drive LCD directly and to perform sophisticated functions as well as complex arithmetic. With the on-chip crystal oscillator, the real-time clock can be easily approached. For power savings, several power-down modes are controllable by software. The GPL12A is widely used for low power electronic products, e.g. remote controller and general-purpose LCD controller.

2. FEATURES

- Built-in Generalplus 8-bit CPU
  - 128 bytes SRAM
  - 8K bytes ROM
  - Working Voltage: 1.9V - 5.5V
  - Maximum CPU speed: 4.0MHz @ 2.7V ~ 5.5V
    2.5MHz @ 1.9V ~ 3.6V
  - CPU Clock can be switched between High-Speed clock (PLL / R-oscillator) divided by 2 / 4 / 8 / 16 or Low-speed clock (32768Hz Crystal-oscillator / 32768Hz R-oscillator)
  - Watchdog timer and illegal address reset circuit are always enabled and will reset CPU if these events occur.
  - Eight wake-up sources (37.9K/N, 32768/N, TMO, EXT1, EXT2, T2Hz, KEYC, NMI)
  - Eight interrupt sources
- Dual clock sources:
  - Dual clock sources controlled by two clock mask options
  - High-speed clock sources: PLL/R-oscillator
  - Low-speed clock sources: 32768 Crystal / 32768 R-oscillator
  - PLL clock = 4.85MHz
  - IR carrier frequency = 37.9KHz
  - Maximum system clock in PLL clock mode = 2.42MHz
- Programmable LCD driver
  - 48-byte Dual-port SRAM for LCD buffers
  - LCD has 1/2 bias, 1/3 bias, 1/4 bias selections
  - Maximum LCD 12x30 (360 dots), 11x30 (330 dots), 10x30 (300 dots), 9x32 (288 dots), 8x32 (256 dots), 5x32 (160 dots), 4x32 (128 dots), 3x32 (96 dots)
- A 16-bit re-loadable timer/counter
- Low voltage reset level is at 2.2V/1.9V and can be disable by Mask-option
- Four Operating modes: Operating / WAIT / HALT /STANDBY
  - Interrupt will wake CPU up
  - Wakeup from CPU reset or next instruction is programmable.
- Built-in RFC (Resistor to Frequency Converter) function
- I/O Port definition
  - 8 IOA, 4 shared pins with LCD Commons / Segments
  - 8 Inputs (INB) with key wakeup function 5 shared pins with LCD Commons / Segments / V3 / CUP3 / CUP4
- Five Reset Flags: watchdog, error address, power-on, external reset, and low voltage reset.
- Low Power consumption:
  - Operating current < 1.0mA @ 3.0V, CPU runs at 1.2MHz, 4.85MHz. PLL on
  - Operating current < 500μA @ 3.0V, CPU runs at 1MHz, 2MHz ROSC on
  - Operating current < 20μA @ 3.0V, CPU runs at 32KHz, 32768 crystal on, PLL off
  - Halt current < 2.0μA @ 3.0V, 1/8 duty, no load, 32768 crystal & LCD on, PLL & CPU off

3. BLOCK DIAGRAM



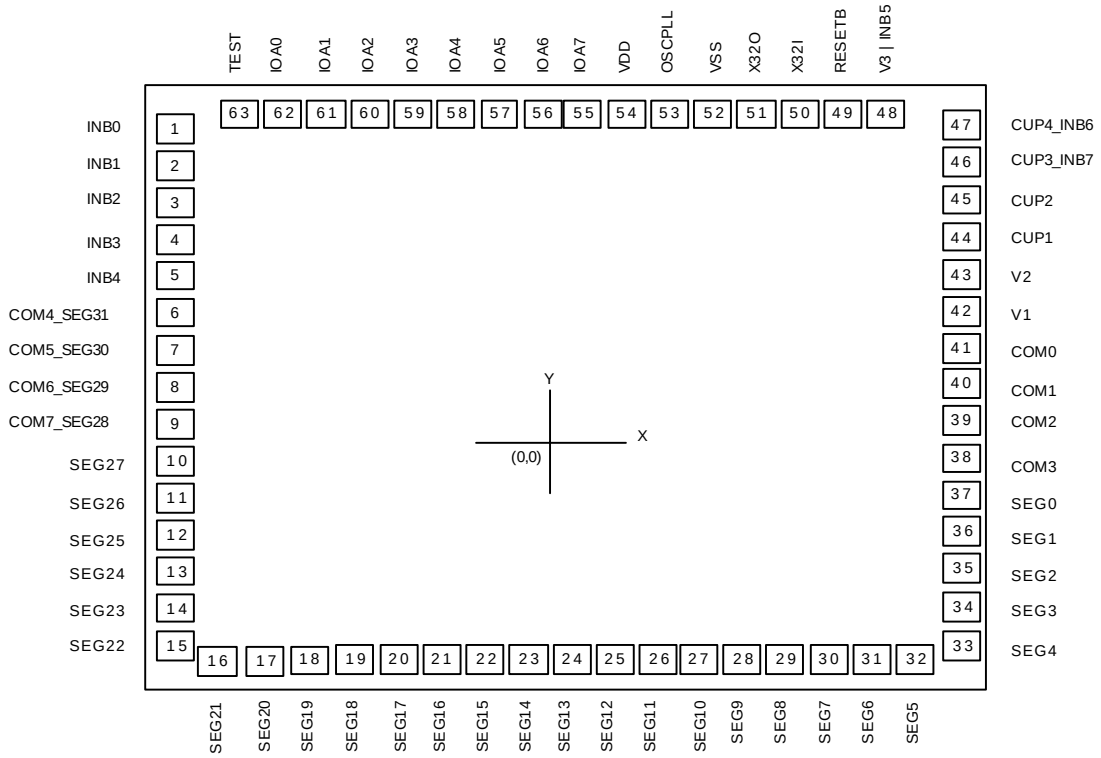
4. SIGNAL DESCRIPTIONS

4.1. PIN Description

Mnemonic	PIN No.		Type	Description
	80 QFP	80 LQFP		
SEG27 – 21 SEG20 – 6 SEG5 – 0	13 - 19 25 - 39 44 - 49	11 - 17 23 - 37 42 - 47	O	LCD driver segment output.
COM4_SEG31	9	7	O	Shared pin for LCD common4 or segment31
COM5_SEG30	10	8	O	Shared pin for LCD common5 or segment30
COM6_SEG29	11	9	O	Shared pin for LCD common6 or segment29
COM7_SEG28	12	10	O	Shared pin for LCD common7 or segment28
COM3 - 0	50 - 53	48 - 51	O	LCD driver common output
V1 V2	54 55	52 53	I	Inputs for setting LCD bias
CUP1 CUP2	56 57	54 55	I	Inputs for setting LCD bias
IOA7	72	70	I/O	IOA port bit7, can be used to output IR carrier
IOA6	73	71	I/O	IOA port bit6, can be used to output tone
IOA5	74	72	I/O	IOA port bit5, shared pin with LCD common8 In RFC application, used as a pass-through (output) pin and connected to sensor.
IOA4	75	73	I/O	IOA port bit4, shared pin with LCD common11 In RFC application, used as a pass-through (output) pin and connected to sensor
IOA3	76	74	I/O	IOA port bit3, shared pin with LCD segment29 In RFC application, used as a pass-through (output) pin and connected to sensor.
IOA2	77	75	I/O	IOA port bit2, shared pin with LCD segment28.
IOA1	78	76	I/O	IOA port bit1, Timer external input 2, External Interrupt input 2. In RFC application, used as input-floating pin and connected to sensor & capacitor.
IOA0	79	77	I/O	IOA port bit0, Timer external input 1, External Interrupt input 1
CUP3_INB7	58	56	I	Shared pin for (1) INB input port bit7 with key-change detection (2) Input for setting LCD bias (CUP3).
CUP4_INB6	59	57	I	Shared pin for (1) INB input port bit6 with key-change detection (2) Input for setting LCD bias (CUP4).
V3_INB5	65	63	I	Shared pin for (1) INB input port bit5 with key-change detection (2) Input for setting LCD bias (V3).
INB4	8	6	I/O	Shared pin for (1) INB input port bit4 with key-change detection (2) LCD segment 31 (3) LCD common 10.
INB3	7	5	I/O	Shared pin for (1) INB input port bit3 with key-change detection (2) LCD segment 30 (3) LCD common 9.
INB2	6	4	I	INB input port bit2 with key-change detection
INB1	5	3	I	INB input port bit1 with key-change detection
INB0	4	2	I	INB input port bit0 with key-change detection
X32I	67	65	I	32.768KHz Crystal/R-OSC Input (option)
X32O	68	66	O	32.768KHz crystal output
RESETB	66	64	I	External reset input pin (Low active)
VSS	69	67	P	Ground input
OSCPLL	70	68	I	PLL Input/R-OSC Input (option)
VDD	71	69	P	Power input
TEST	80	78	I	Test input

Legend: I = Input, O = Output, P = Power

4.2. PAD Assignment



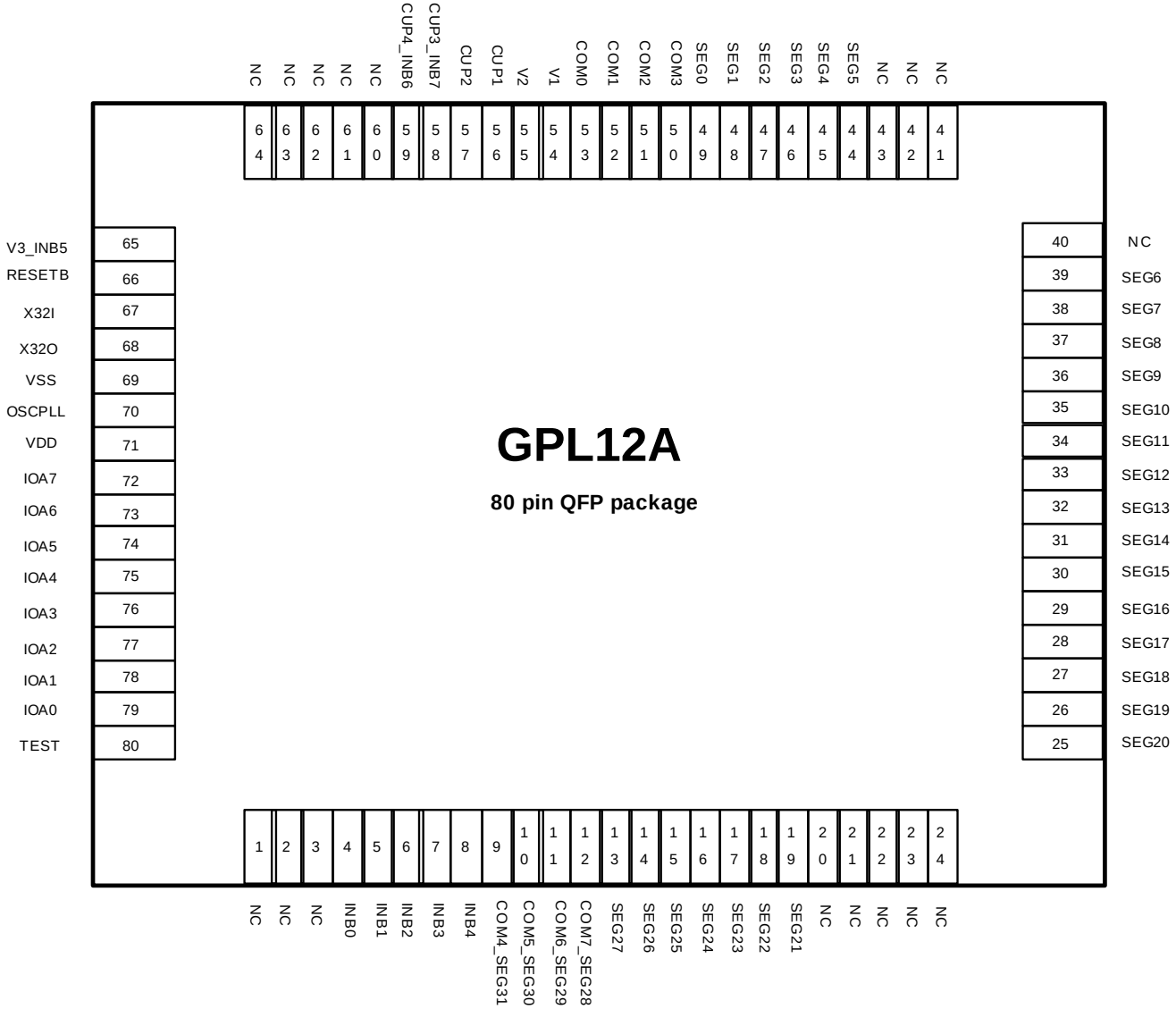
The IC substrate should be connected to VSS or floating.

Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

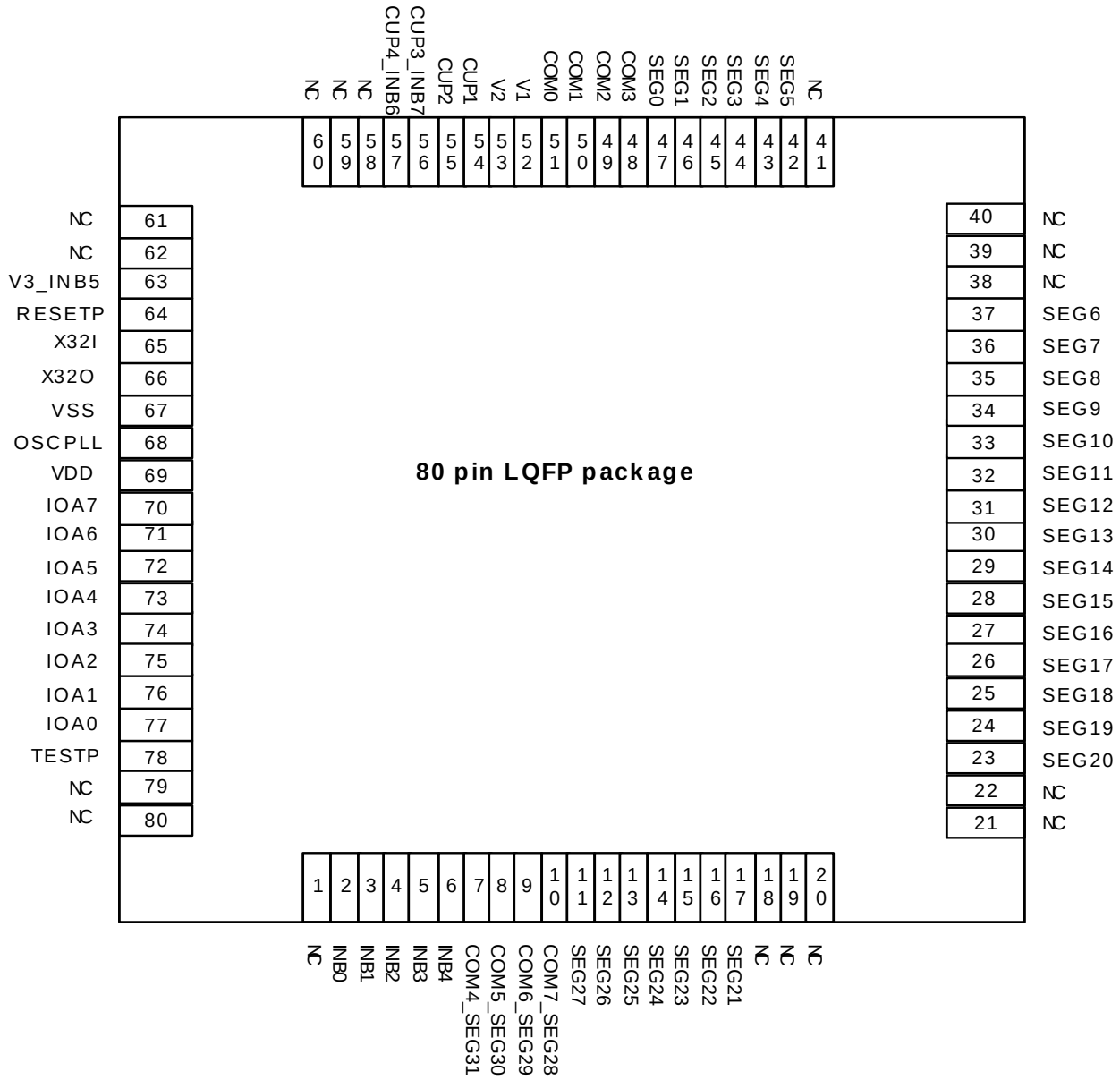
Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

4.3. PIN Map

4.3.1. 80 pin QFP Package (HQ05x)

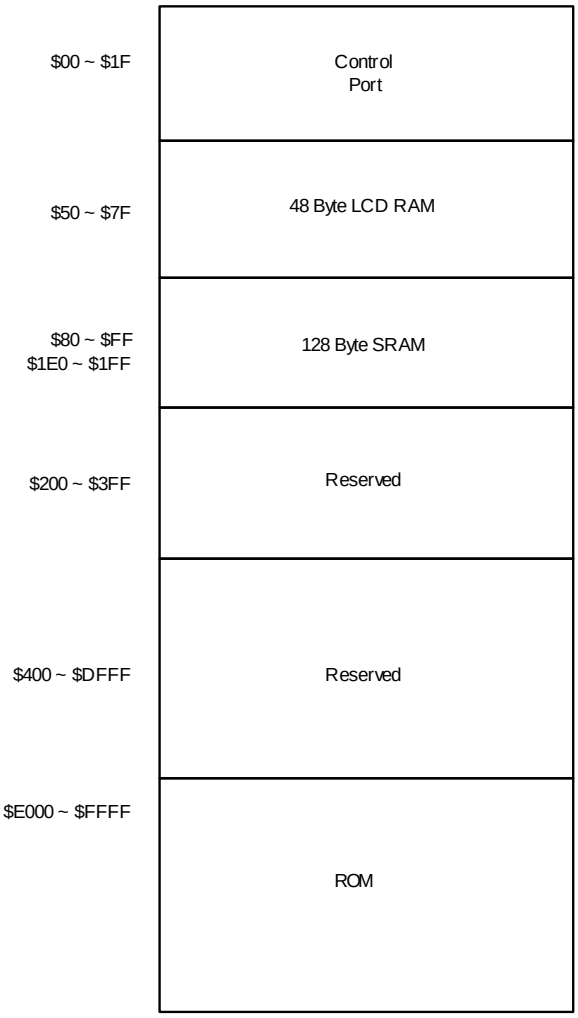


4.3.2. 80 pin LQFP Package (HL04x)



5. FUNCTION DESCRIPTIONS

5.1. Map of Memory and I/Os



Note:

1. 512 bytes testing program ROM: $400 ~ $5FF
2. $0080 ~ $00FF maps to the 128 bytes SRAM, and $01E0 ~ $01FF also maps to $E0 ~ $FF (maximum stack is 32 byte)
3. Illegal Address range: $0020 ~ $004F, $0100 ~ $01DF, $0200 ~ $03FF $0400 ~ $DFFF

5.2. Clock Sources Control

There are two groups of clock sources controlled by two mask-options (HCKOPT / LCKOPT) (1) High-speed clock source: PLL / ROSC (2) Low-speed clock source: 32768Hz R-oscillator / Crystal oscillator

5.2.1. Clock sources combination

	HCKOPT	LCKOPT	
ROSC/C32K	0	0	
ROSC/R32K	0	1	
PLL/C32K	1	X	Note1

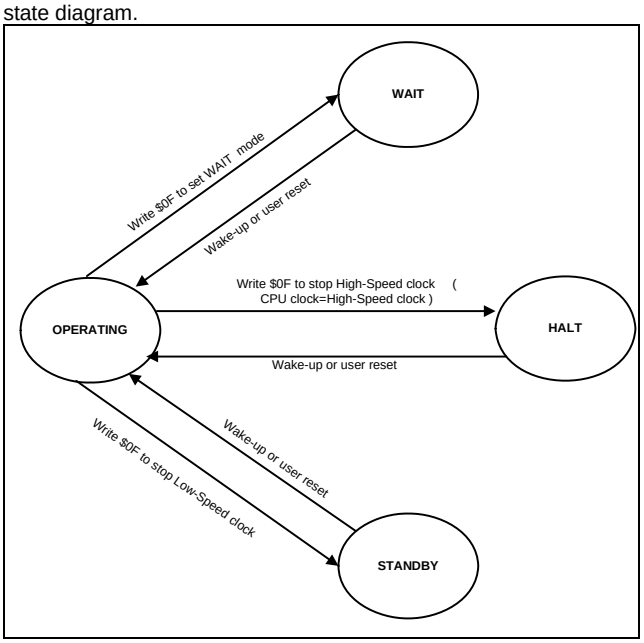
Note 1: No PLL/R32K combination, it is mapped to PLL/C32K mode.

5.2.2. Switching of CPU clock

CPU clock is programmable as (1) high-speed clock / 2 / 4 / 8 / 16 or (2) 32768Hz.

5.3. Operation Modes

There are four operation modes involved in GPL12A - standby, halt, wait and operating. The following figure is the GPL12A state diagram.



The following table summarizes the differences between these modes.

	Operating	Wait	Halt	Standby
CPU clock	ON	OFF	OFF	OFF
PLL/Oscillator	ON	ON	OFF	OFF
32768 crystal / 32768 oscillator	ON	ON	ON	OFF

5.3.1. Operating mode

In operating mode, all functions (CPU, PLL/R-oscillator, 32768Hz crystal /32768Hz oscillator, timer/counter, LCD driver…) are activated. In general, this mode consumes the highest power.

5.3.2. Wait mode

In wait mode, CPU clock halts and waits for an event (key-change, timer overflow…) to wake up. In addition to CPU stop, all other resources are still working. This mode consumes less power than all other peripherals that are activated except CPU.

5.3.3. Halt mode

In halt mode, CPU clock halts and PLL/ROSC clock sources stop and wait for an event (key change, timer overflow…) to wake up. The 32768Hz relevant functions, such as timer/counter and LCD driver, may remain active in halt mode.

5.3.4. Standby mode

The standby mode is a mode that the device is placed in its lowest current consumption state. In standby mode, all functions are turned off. In addition, RAM and I/Os will remain in their previous states.

5.4. LCD Controller/Driver

The GPL12A contains a 360-dot LCD controller/driver in which the configuration can be defined via setting up the LCD Control Register. Once the LCD configuration is completed, the desired patterns can be displayed by filling the LCD RAM with proper data. The LCD driver can also operate during sleep mode by keeping 32768Hz oscillator running. The LCD driver in GPL12A supports 1/3 ~ 1/12 duty and 1/2 ~ 1/4 bias. The LCD frame rate can be adjusted by programming Port_LCDCK_CTL($11) register in small step between 40 Hz ~ 100 Hz.

5.5. Watchdog Timer (WDT)

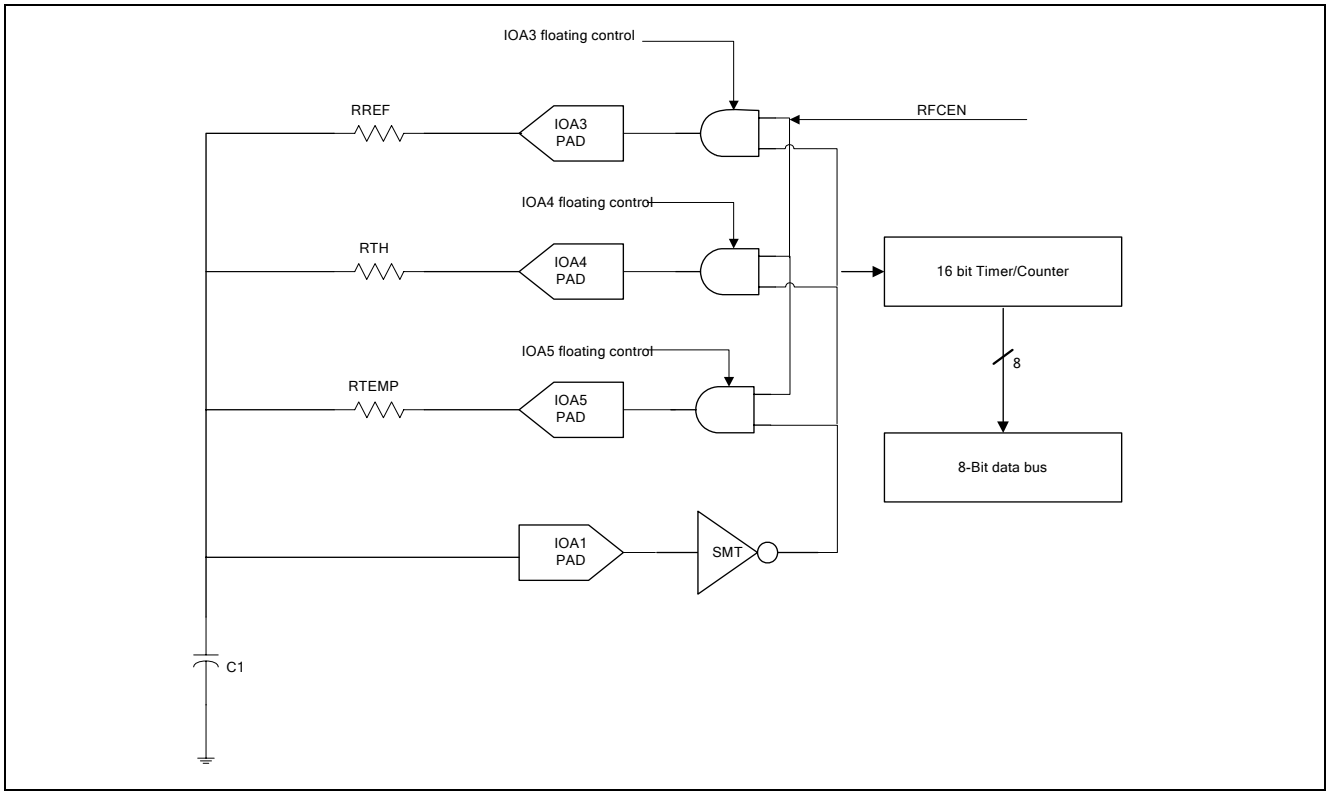
An on-chip watchdog timer is also available in the GPL12A. The WDT is designed to recover system from abnormal operation. If WDT is not cleared within one second, the WDT generates reset signal to CPU. The WDT is recommended to be cleared via software programming in every 0.5 seconds to avoid accidental reset. Note that the WDT works only when 32768Hz clock is activated.

5.6. Wakeup/Interrupt Control

There are eight wakeup sources: 37.9K/N, 32768/N, TMO, EXT1, EXT2, T2Hz, KEYC, and NMI. Interrupt sources can be used as (1) wake-up source only. (2) both wakeup source and interrupt CPU.

5.7. RFC Function

The RFC (Resistor to Frequency Converter) circuit contains a RC oscillation circuit and a 16-bit timer/counter to calculate the resistance of temperature or humidity sensor relative to reference resistor. The circuit is shown below.



5.8. IR Output Control

In IR-application, we must use PLL/32768 Hz crystal combination of clock sources to get PLL Freq = 4.85MHz. Next, the 4.85MHz PLL Freq is sent to the duty controller to generate 37.9KHz and 1/8 duty resolution IR-output pulse. The 37.9KHz IR-output pulse is delivered to Port IOA7 and controlled by software or Timer-overflow.

5.9. Mask Options

PIN	Description	Comment
HCKOPT	0: ROSC; 1: PLL	
LCKOPT	0: 32768 Hz oscillator 1 32768 Hz crystal	
LVROFF	0: LVR enable 1: LVR disable	
LVRLVL	0: 1.9V 1: 2.2V	

5.10. Default Status of PINs

IOA (IOA0 ~ IOA7) => Input with pull-low
INB (IOB0 ~ IOB7) => Input with pull-low
LCD => OFF (Common = Low & Segment = Low)
CUP3_INB6 = INB6
CUP4_INB7 = INB7
V3_INB5 = INB5
COM4_SEG31 = SEG31
COM5_SEG30 = SEG30
COM6_SEG29 = SEG29
COM7_SEG28 = SEG28
INB3 (SEG30/COM9) = INB3
INB4 (SEG31/COM10) = INB4
IOA4 (COM11) = IOA4
IOA5 (COM8) = IOA5
OSCPLL = ROSC (HCKOPT Mask-option=Low)
X32I/R32I = X32K (LCKOPT Mask-option=Low)

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to + 60℃
Storage Temperature	T_{STO}	-50℃ to + 150℃

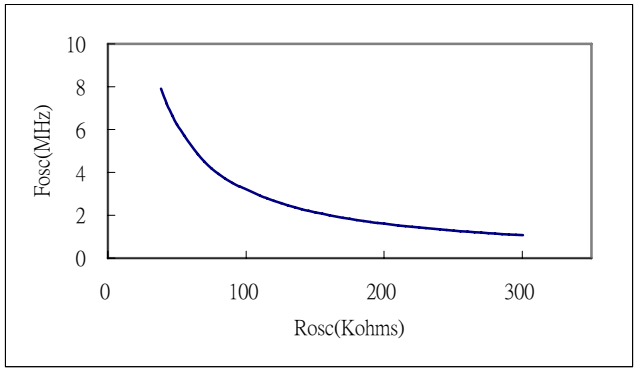
Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

6.2. DC Characteristics(T_A=25℃)

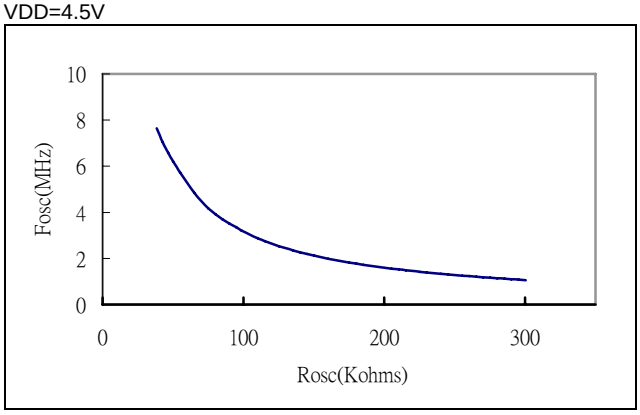
Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.7	-	5.5	V	Maximum CPU speed = 4.0MHz
Operating Voltage	VDD	1.9	-	3.6	V	Maximum CPU speed = 2.5MHz
Operating Current	I_{OP}	-	-	1.0	mA	VDD = 3.0V, CPU = 1.2MHz, PLL ON
		-	-	500	μA	VDD = 3.0V, CPU = 1.0MHz, 2MHz ROSC ON
		-	-	20	μA	VDD = 3.0V, CPU = 32768, 32768 ON, PLL OFF
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 3.0V, PLL & 32768 OFF
Audio Output Current	I_{AUD}	8.0	-	-	mA	VDD = 3.0V
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High Current	I_{OH1}	5.0	-	-	mA	VDD = 3.0V, VOH = 2.4V, IOA[7:0]
Output Low Current	I_{OL1}	8.0	-	-	mA	VDD = 3.0V, VOL = 0.8V, IOA[7:0]
Pull-up Resistor	R_{PU1}	-	120K	-	-	VDD = 3.0V
	R_{PU1}	-	70K	-	-	VDD = 4.5V
Pull-down resistor	R_{PD1}	-	120K	-	-	VDD = 3.0V
	R_{PD1}	-	70K	-	-	VDD = 4.5V

6.3. The Relationships between the R_{osc} and the F_{osc}

VDD=3V

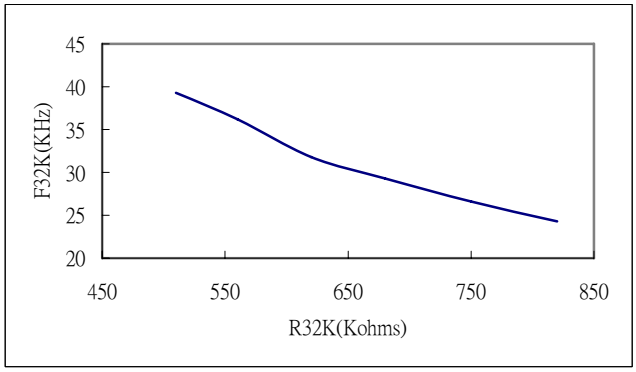


VDD=4.5V

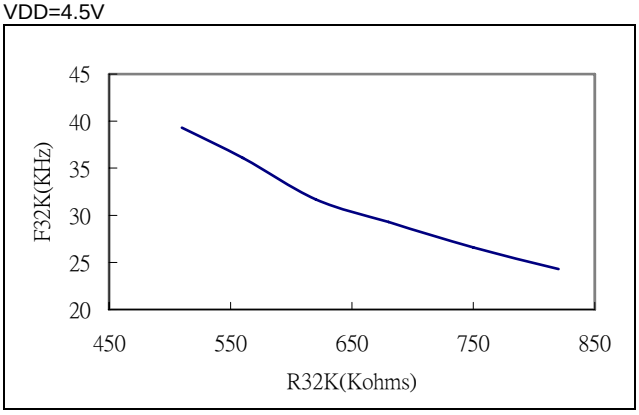


6.4. The Relationships between the R32K and the F32K

VDD=3V

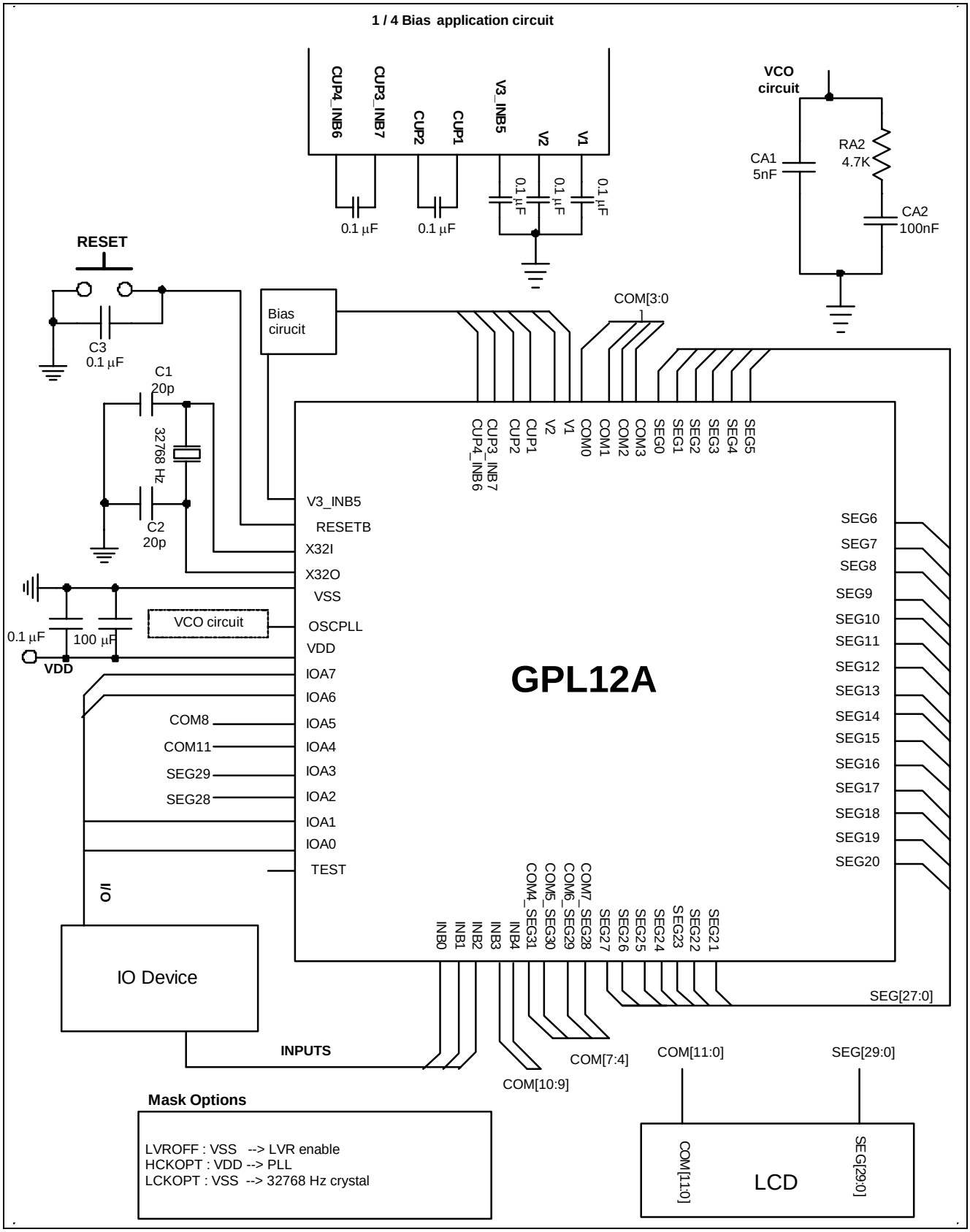


VDD=4.5V

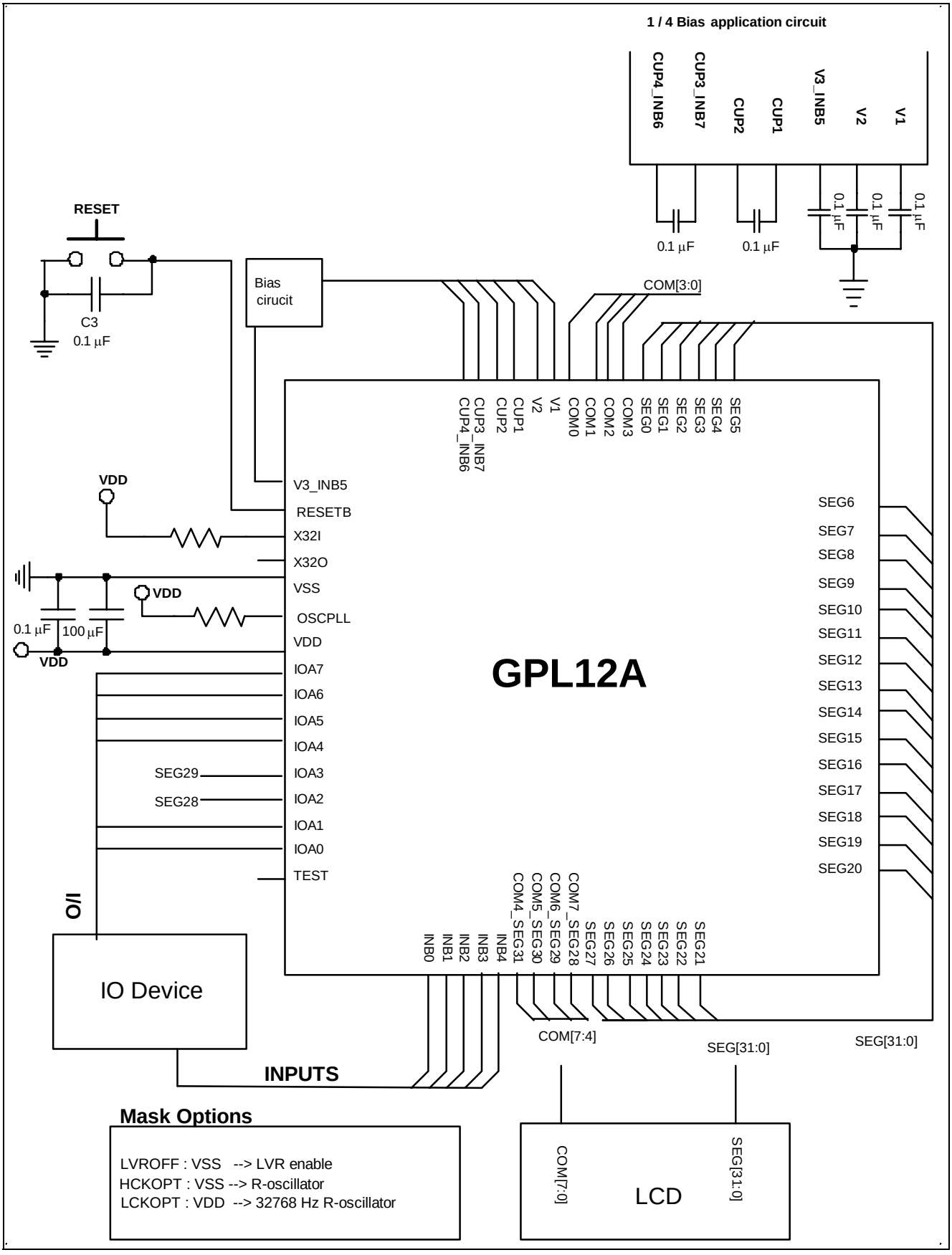


7. APPLICATION CIRCUITS

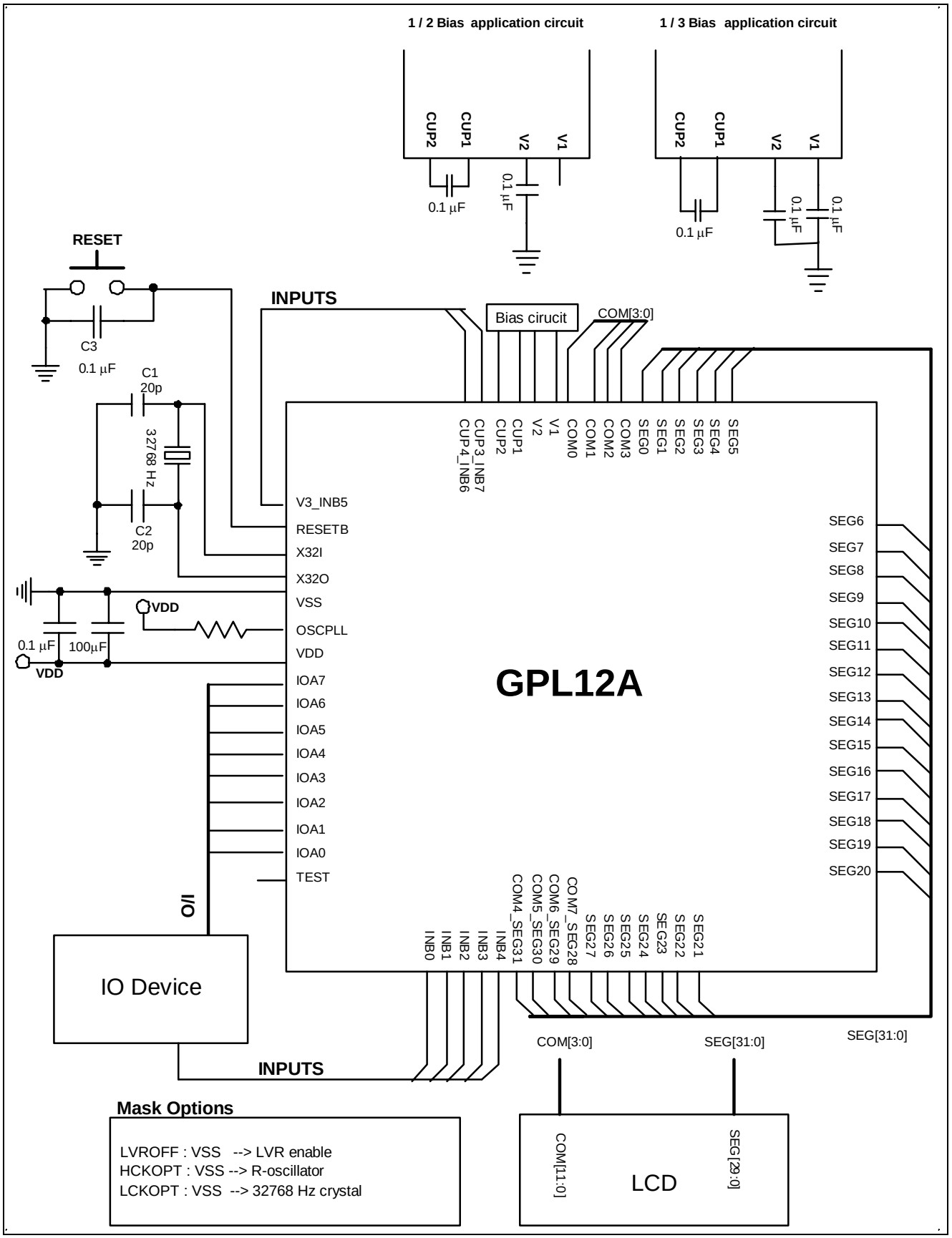
7.1. 360 Dots (12 x 30) LCD Driver, 1/4 Bias, PLL / 32768Hz Crystal



7.2. 256 Dots (8 x 32) LCD Driver, 1/4 Bias, R-Oscillator / 32768Hz R-Oscillator



7.3. 128 Dots (4 x 32) LCD Driver, 1/2 or 1/3 Bias, R-Oscillator / 32768Hz Crystal



8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GPL12A - NnnV - C	Chip form
GPL12A - NnnV - HQ05x	Green Package form - QFP 80
GPL12A - NnnV - HL04x	Green Package form - LQFP 80

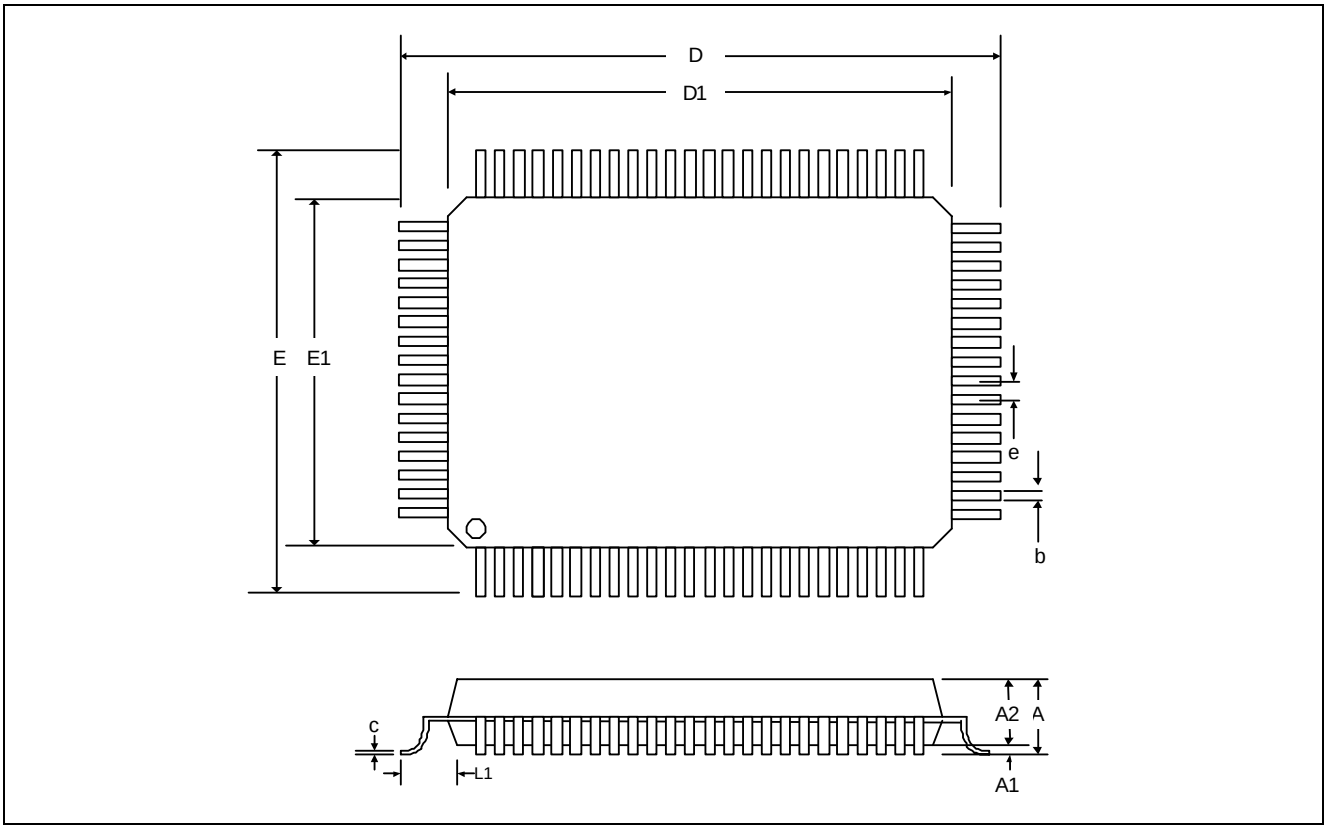
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

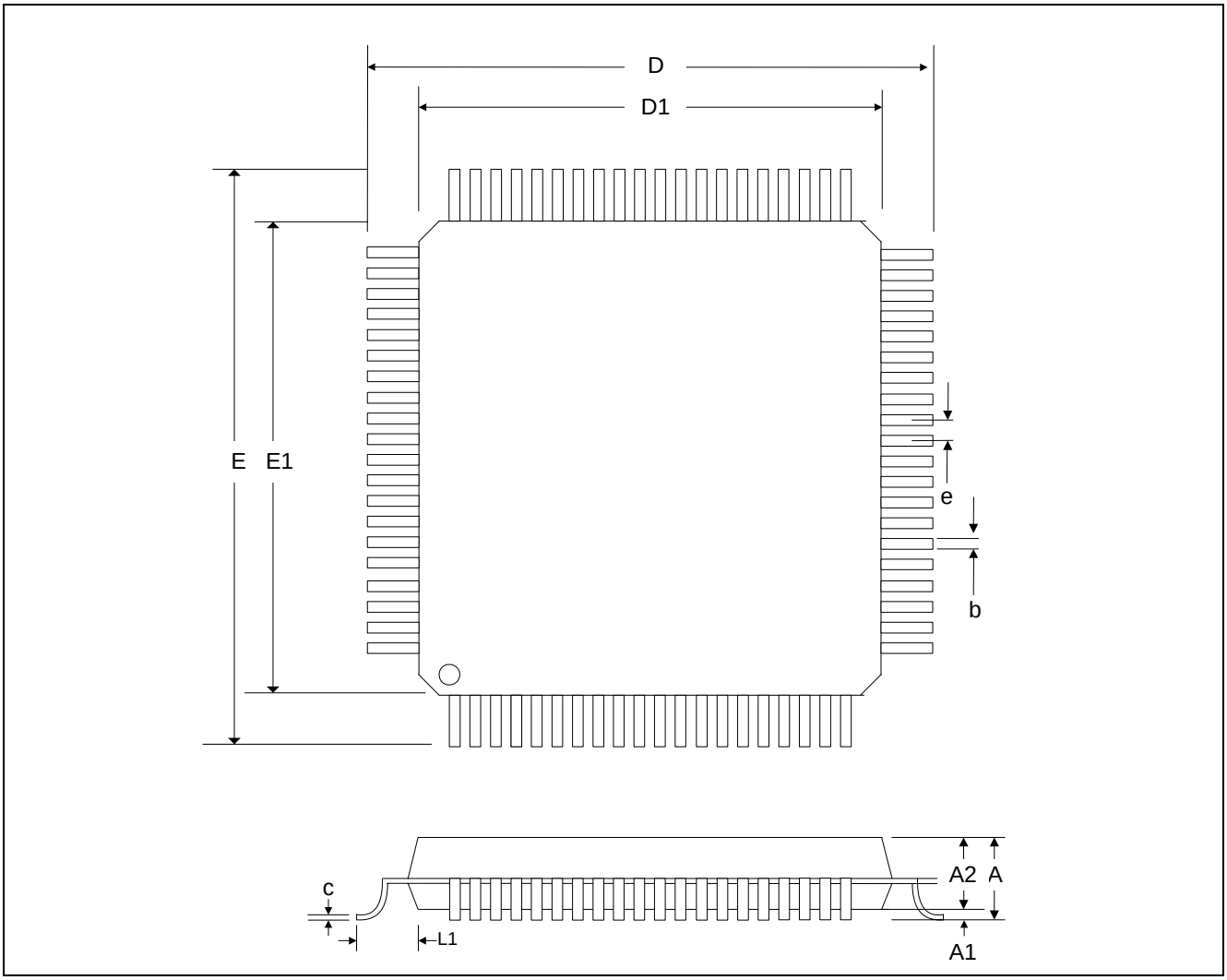
8.2. Package Information

8.2.1. 80 pin QFP (HQ05x)



Symbol	Min.	Nom.	Max.	Unit
A	-	-	3.40	Millimeter
A1	0.25	-	-	Millimeter
A2	2.50	2.72	2.90	Millimeter
b	0.30	0.35	0.45	Millimeter
c	0.11	0.15	0.23	Millimeter
D	23.20 REF			Millimeter
D1	20.00 REF			Millimeter
E	17.20 REF			Millimeter
E1	14.00 REF			Millimeter
e	0.80 REF			Millimeter
L1	1.60 REF			Millimeter

8.2.2. 80 pin LQFP (HL04x)



Symbol	Min.	Nom.	Max.	Unit
A	-	-	1.60	Millimeter
A1	0.05	-	0.15	Millimeter
A2	1.35	1.40	1.45	Millimeter
b	0.17	0.20	0.27	Millimeter
c	0.09	-	0.20	Millimeter
D	14.00 REF			Millimeter
D1	12.00 REF			Millimeter
E	14.00 REF			Millimeter
E1	12.00 REF			Millimeter
e	0.50 REF			Millimeter
L1	1.00 REF			Millimeter

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10. REVISION HISTORY

Date	Revision #	Description	Page
JUL. 27, 2011	1.4	1. Modify “Ordering Information” in section 8.1. 2. Package information change from QQ05 to HQ05. 3. Package information change from QL04 to HL04.	16 6, 16 7, 17
JAN. 13, 2011	1.3	1. Working voltage modified to “1.9V～5.5V”; 2. Maximum CPU speed modified to “4.0MHz@2.7～5.5V；2.5MHz@1.9~3.6V”; 3. Modified low voltage reset description; 4. Add “1.9V/2.2V LVR level” for mask option select; 5. Modified operation voltage at DC Characteristics	3 3 3 10 11
AUG. 7, 2008	1.2	“IOA3” in RFC function diagram change to “IOA1”.	8
SEP. 27, 2005	1.1	Add 6.3~6.4 the illustration about DC characteristics.	9
MAR.16, 2005	1.0	Original Note: The GPL12A data sheet v1.0 is a continued version of SPL12A data sheet v0.2.	17