DATA SHEET

# GPL13A1

## 8K bytes Micro-controller with LCD Driver

Jul. 14, 2015

Version 1.0

# Table of Contents

**PAGE**

# 8K BYTES MICRO-CONTROLLER WITH LCD DRIVER

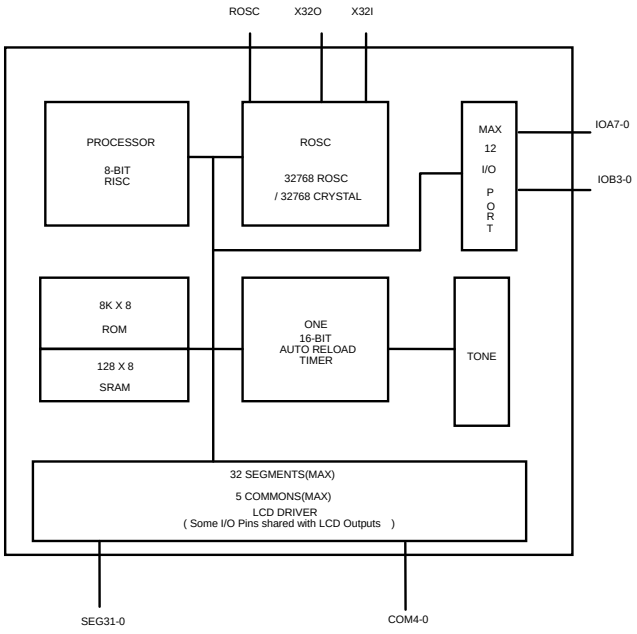
## 1. GENERAL DESCRIPTION

GPL13A1, a mask-version of GPL11A(OTP) family, contains a CMOS 8-bit single chip Micro-controller, LCD drivers, 8K bytes ROM, SRAM, I/O, timer/counter, ROSC, audio/remote control out, and resistor to frequency converter (RFC) function, all in one chip. The GPL13A1 is designed to drive LCD directly and perform controller function as well as arithmetic function efficiently. With an on-chip crystal oscillator, the real-time clock can be easily achieved. For power savings, several power-down modes are controllable by software. The GPL13A1 is widely used for low power electronic products, e.g. remote controller and general-purpose LCD controller.

## 2. FEATURES

- Built-in GENERALPLUS 8-bit CPU
  - 128-byte SRAM
  - 8K-byte ROM
  - Working Voltage: 1.9V - 5.5V (low voltage reset is disabled)
    2.2V - 5.5V (low voltage reset is enabled)
  - Maximum CPU speed: 4.0MHz @ 2.2V ~ 5.5V
    2.5MHz @ 1.9V ~ 5.5V
  - CPU Clock can be switched between High-Speed clock (R-oscillator) divided by 2 / 4 / 8 / 16 or Low-speed clock (32768Hz Crystal-oscillator / 32768Hz R-oscillator)
  - Watchdog timer and illegal address reset circuit are always enabled and will reset CPU if these events occur
  - Eight wakeup sources (37.9K/N, 32768/N, TMO, EXT1, EXT2, T2Hz, KEYC, NMI)
  - Eight interrupt sources
- Dual clock sources:
  - Dual clock sources are controlled by two clock mask options
  - High-Speed clock sources: R-oscillator
  - Low-speed clock sources: 32768 Crystal / 32768 R-oscillator
- Programmable LCD driver
  - 20-byte dual-port SRAM for LCD buffers
  - LCD has 1/2 bias, 1/3 bias selections
  - Maximum LCD 5x32 (160 dots), 5x31 (155 dots), 4x32 (128 dots), 3x32 (96 dots)
- A 16-bit re-loadable timer/counter
- Low voltage reset level is at 2.2V and can be disabled by mask option.
- Four Operating modes: Operating / WAIT / HALT /STANDBY
  - Interrupt will wake CPU up
  - Wakeup from CPU reset or next instruction is programmable
- Built-in RFC (Resistor to Frequency Converter) function
- I/O Port definition:
  - 8 IOA
  - 4 IOB* with key wakeup function, one shared pin with LCD Segment
- Five Reset flags: watchdog, error address, power-on, external reset, and low voltage
- Low Power consumption:
  - Operating current < 500μA @ 3.0V, CPU runs at 1MHz, 2MHz ROSC on
  - Operating current < 20μA @ 3.0V, CPU run 32KHz, 32768Hz crystal on, ROSC off
  - Halt current < 2.0μA @ 3.0V, 1/8 duty, no load, 32768Hz crystal & LCD on, ROSC & CPU off

## 3. BLOCK DIAGRAM




**Note*:** IOB's output function can only be emulated on GPL11B. EV-board cannot emulate IOB's output function.

## 4. SIGNAL DESCRIPTIONS

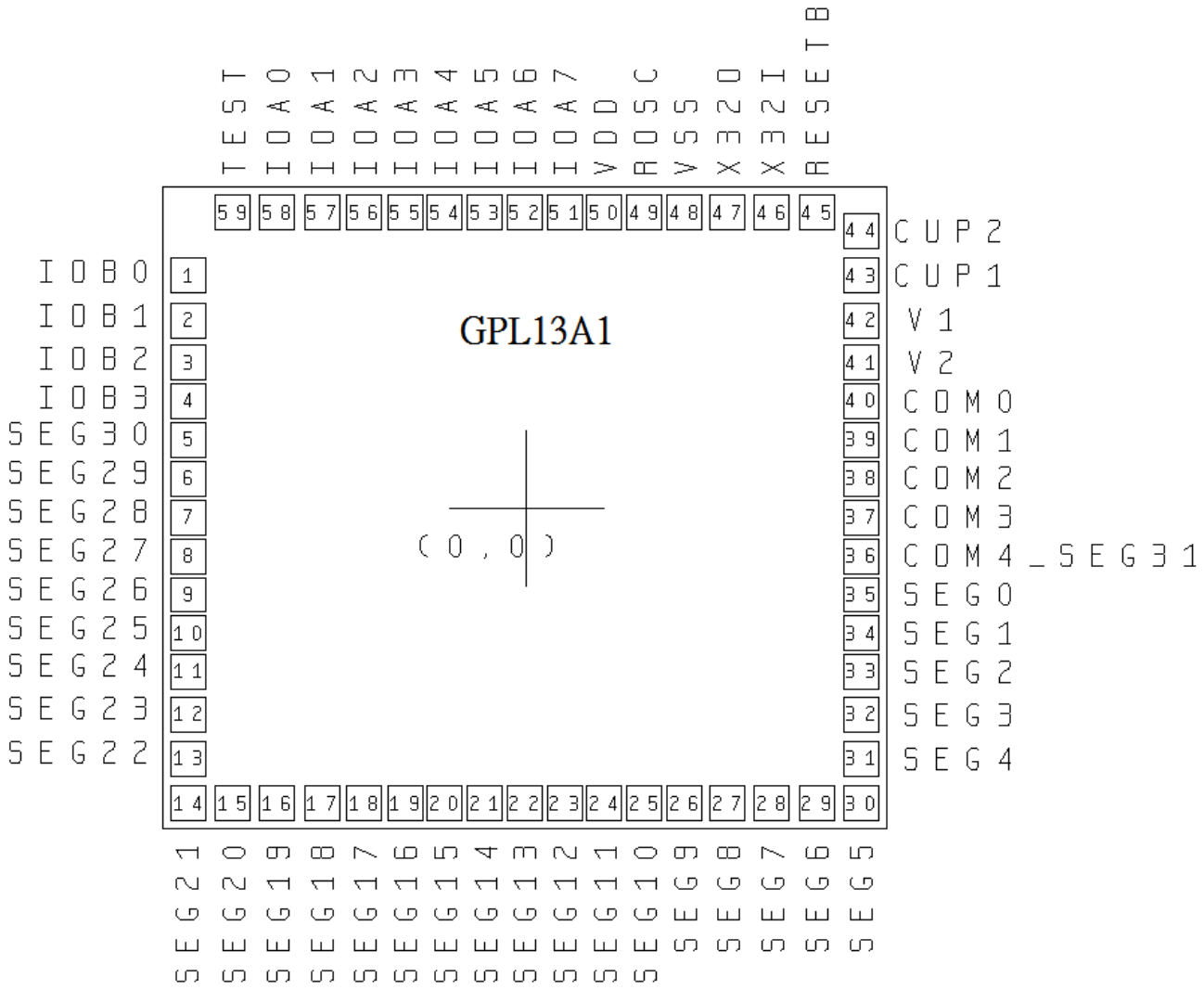
### 4.1. PIN Description

| Mnemonic | Type | Description |
|---|---|---|
| SEG30 - 0 | O | LCD driver segment output. |
| COM4_SEG31 | O | Shared pin for LCD common4 or segment31. |
| COM3 - 0 | O | LCD driver common output. |
| V1<br>V2 | I | Inputs for setting LCD bias. |
| CUP1<br>CUP2 | I | Inputs for setting LCD bias. |
| IOA7 | I/O | IOA port bit7, can be used to output IR carrier. |
| IOA6 | I/O | IOA port bit6, can be used to output tone. |
| IOA5 | I/O | IOA port bit5.<br>In RFC application, used as a pass-through (output) pin and connected to sensor. |
| IOA4 | I/O | IOA port bit4.<br>In RFC application, used as a pass-through (output) pin and connected to sensor. |
| IOA3 | I/O | IOA port bit3.<br>In RFC application, used as a pass-through (output) pin and connected to sensor. |
| IOA2 | I/O | IOA port bit2. |
| IOA1 | I/O | IOA port bit1, Timer external input 2, External Interrupt input 2.<br>In RFC application, used as input-floating pin and connected to sensor & capacitor. |
| IOA0 | I/O | IOA port bit0, Timer external input 1, External Interrupt input 1. |
| IOB3 | I/O | Shared pin for (1) IOB port bit3 with key-change detection (2) LCD segment 31. |
| IOB2 | I/O | IOB port bit2 with key-change detection. |
| IOB1 | I/O | IOB port bit1 with key-change detection. |
| IOB0 | I/O | IOB port bit0 with key-change detection. |
| X32I | I | 32.768KHz Crystal/R-OSC Input (option). |
| X32O | O | 32.768KHz crystal output. |
| RESETB | I | External reset input pin (Low active). |
| VSS | P | Ground input. |
| ROSC | I | R-OSC Input. |
| VDD | P | Power input. |
| TEST | I | Test input. |

Legend: I = Input, O = Output, P = Power

Total 59 pins

### 4.2. PAD Assignment

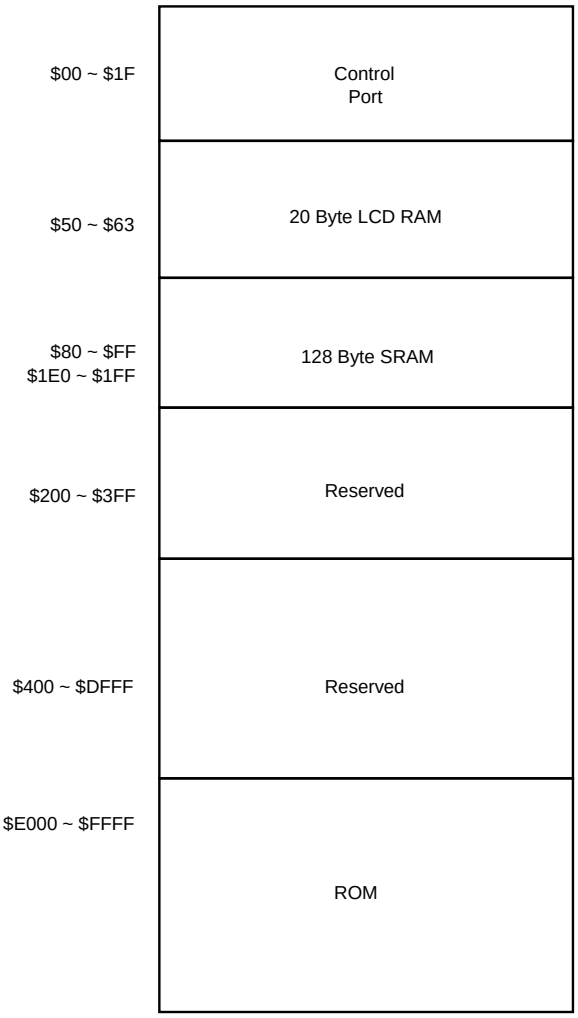



This IC substrate should be connected to VSS

**Note1:** To ensure the IC functions properly, please bond all of VDD and VSS pins.
**Note2:** The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

# 5. FUNCTION DESCRIPTIONS

## 5.1. Map of Memory and I/Os




**Note:**

1. 512 bytes testing program ROM: $400 ~ $5FF
2. $0080 ~ $00FF maps to the 128 bytes SRAM, and $01E0 ~ $01FF also maps to $E0 ~ $FF (maximum stack is 32 byte)
3. Illegal Address range: $0020 ~ $004F, $0100 ~ $01DF, $0200 ~ $03FF $0400 ~ $DFFF

## 5.2. Clock Sources Control

There are two groups of clock sources controlled by two mask-options (HCKOPT / LCKOPT) (1) High-speed clock source: PLL / ROSC (2) Low-speed clock source: 32768Hz R-oscillator / Crystal oscillator.

### 5.2.1. Clock sources combination

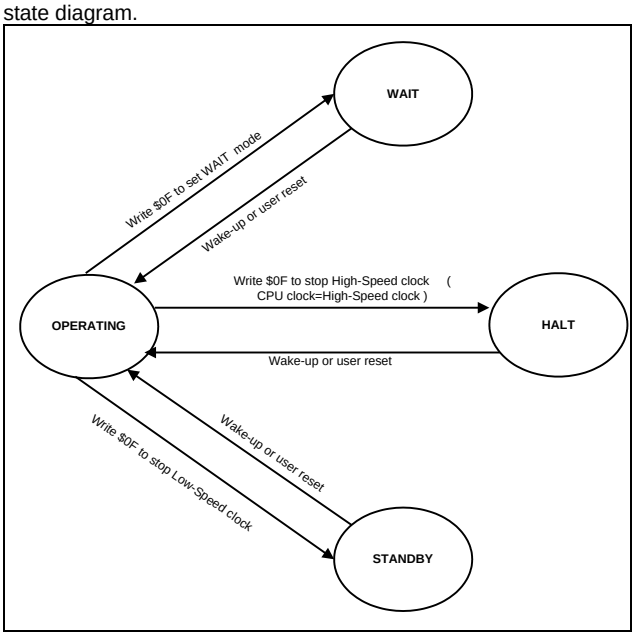
| | HCKOPT | LCKOPT |
|---|---|---|
| ROSC/C32K | 0 | 0 |
| ROSC/R32K | 0 | 1 |
| Reserved | 1 | X |

### 5.2.2. Switching of CPU clock

CPU clock is programmable as (1) high-speed clock / 2 / 4 / 8 / 16 or (2) 32768Hz.

## 5.3. Operation Modes

There are four operation modes involved in GPL13A1 - standby, halt, wait and operating. The following figure is the GPL13A1 state diagram.




The following table summarizes the differences between these modes.

| | Operating | Wait | Halt | Standby |
|---|---|---|---|---|
| CPU clock | ON | OFF | OFF | OFF |
| R-Oscillator | ON | ON | OFF | OFF |
| 32768Hz crystal oscillator/ 32768Hz R-oscillator | ON | ON | ON | OFF |

### 5.3.1. Operating mode

In operating mode, all functions (CPU, R-oscillator, 32768Hz crystal /32768Hz R-oscillator, timer/counter, LCD driver…) are activated. In general, this mode consumes the highest power.

### 5.3.2. Wait mode

In wait mode, CPU clock halts and waits for an event (key-change, timer overflow…) to wake up. In addition to CPU stop, all other resources are still working. This mode consumes less power than all other activated peripherals except CPU.

### 5.3.3. Halt mode

In halt mode, CPU clock halts and ROSC clock sources stops, waits for an event (key change, timer overflow…) to wake up. The 32768Hz relevant functions, such as timer/counter and LCD driver, may remain active in halt mode.

### 5.3.4. Standby mode

The standby mode is a mode that the device is placed in its lowest current consumption state. In standby mode, all functions are turned off. In addition, RAM and I/Os will remain in their previous states.

### 5.4. LCD Controller/Driver

The GPL13A1 contains a 360-dot LCD controller/driver that can be configured to specified patterns via programming the LCD Control register. Once the configuration is completed, desired patterns can be displayed by filling data into LCD RAM. The LCD driver supports 1/3 ~ 1/5 duty and 1/2 ~ 1/3 bias, and its LCD frame rate can be adjusted by programming the Port_LCDCK_CTL($11) register in small step between 40 Hz ~ 100 Hz. The LCD controller/driver can still be operating during sleep mode by keeping the 32768Hz oscillator alive.

### 5.5. Watchdog Timer (WDT)

GPL13A1 also features an on-chip watchdog timer (WDT) that is designed to recover the system from abnormal operation. If WDT is not cleared within one second, the WDT generates a signal to reset CPU and the WDT is recommended to be cleared every 0.5 seconds via software programming to avoid accidental reset. Note that the WDT only works when 32768Hz clock is activated.

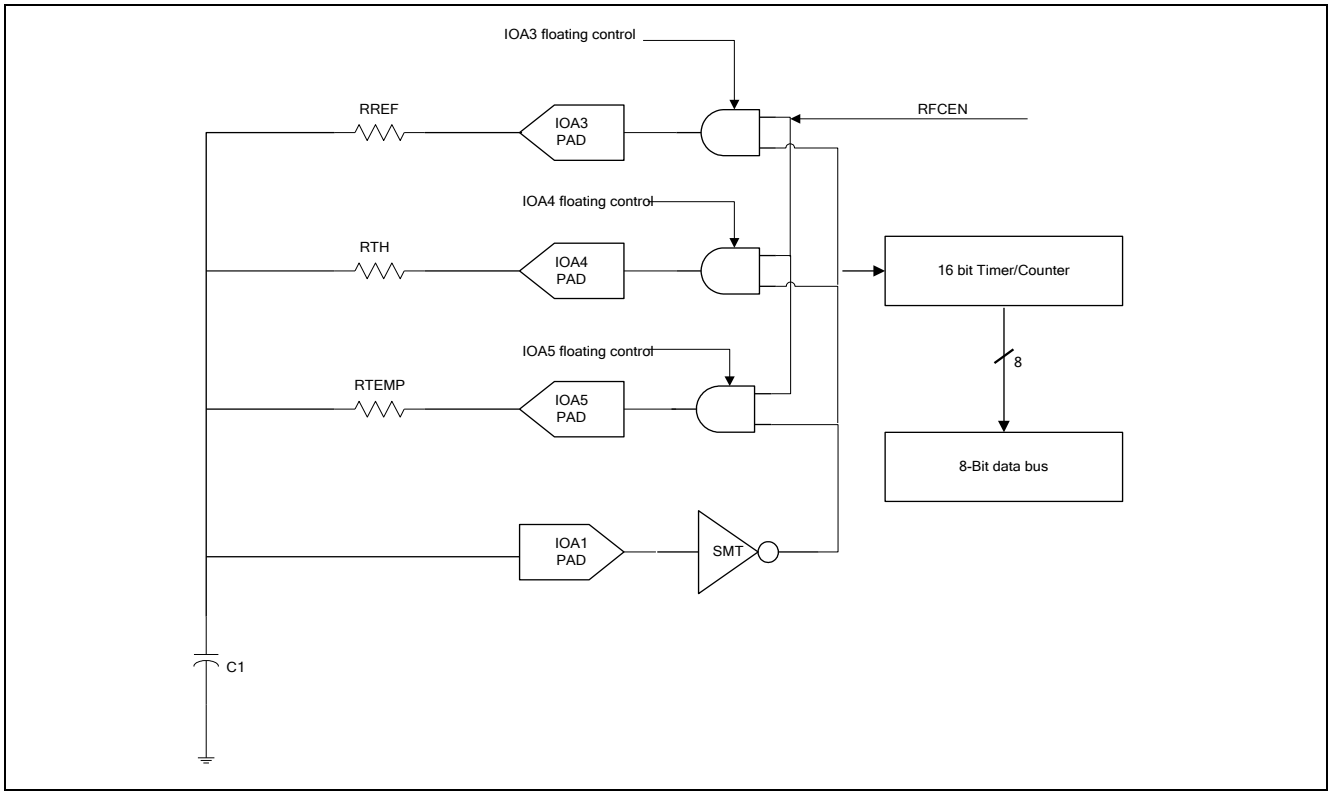
### 5.6. Wakeup/Interrupt Control

There are eight wakeup sources: 37.9K/N, 32768/N, TMO, EXT1, EXT2, T2Hz, KEYC, and NMI.

Interrupt sources can be used as (1) wake-up source only. (2) both wakeup source and interrupt CPU.

### 5.7. RFC Function

The RFC (Resistor to Frequency Converter) circuit contains a RC oscillation circuit and a 16-bit timer/counter to calculate the resistance of temperature or humidity sensor relative to reference resistor. The circuit is shown below.



### 5.8. Mask Options

| Mask option | Description | Comment |
|---|---|---|
| LCKOPT | 1: 32768Hz oscillator<br>2: 32768Hz crystal | |
| LVROFF | 1: LVR enabled<br>2: LVR disabled | |
| IOB3_SEG31_SEL | 1. IOB3 as I/O<br>2. IOB3 as SEG31 | |

### 5.9. Default Status of PINs

IOA (IOA0 ~ IOA7) => Input with pull-low

IOB (IOB0 ~ IOB3) => Input with pull-low

LCD => OFF (Common = Low & Segment = Low)

COM4_SEG31 = SEG31

## 6. ELECTRICAL SPECIFICATIONS

### 6.1. Absolute Maximum Ratings

| Characteristics | Symbol | Ratings |
|---|---|---|
| DC Supply Voltage | V+ | < 7.0V |
| Input Voltage Range | $V_{IN}$ | -0.5V to $V_+$ + 0.5V |
| Operating Temperature | $T_A$ | -10℃ to + 70℃ |
| Storage Temperature | $T_{STO}$ | -50℃ to + 150℃ |

**Note:** Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

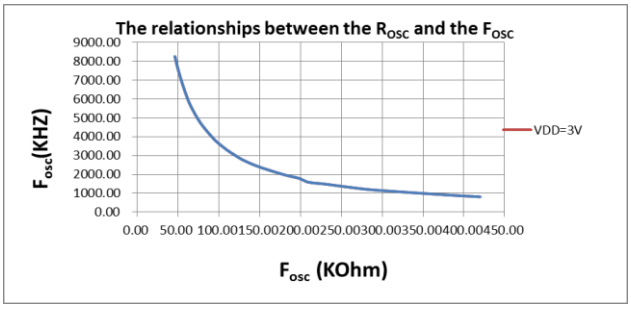
### 6.2. DC Characteristics(VDD=3.0V, $T_A$=25℃, unless otherwise specified)

| Characteristics | Symbol | Limit | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operating Voltage | VDD | 2.2* | - | 5.5 | V | Maximum CPU speed = 4.0MHz |
| Operating Voltage | VDD | 1.9* | - | 5.5 | V | Maximum CPU speed = 2.5MHz |
| Operating Current | $I_{OP}$ | - | 500 | - | μA | VDD = 3.0V, CPU = 1.0MHz, 2MHz ROSC ON |
| | | - | 20 | - | μA | VDD = 3.0V, CPU = 32768, 32768 ON, ROSC OFF |
| Halt Current | $I_{HALT}$ | - | 2 | - | μA | VDD = 3.0V, CPU OFF, 32768 xtal ON, ROSC OFF, LCD ON, No load |
| Standby Current | $I_{STBY}$ | - | - | 1.0 | μA | VDD = 3.0V, ROSC & 32768 OFF |
| Audio Output Current | $I_{AUD}$ | 8.0 | - | - | mA | VDD = 3.0V |
| Input High Level | $V_{IH}$ | 2.0 | - | - | V | VDD = 3.0V |
| Input Low Level | $V_{IL}$ | - | - | 0.8 | V | VDD = 3.0V |
| Output High Current | $I_{OH1}$ | 5.0 | - | - | mA | VDD = 3.0V, VOH = 2.4V, IOA[7:0] |
| Output Low Current | $I_{OL1}$ | 8.0 | - | - | mA | VDD = 3.0V, VOL = 0.8V, IOA[7:0] |
| Pull-up Resistor | $R_{PU1}$ | - | 140K | - | - | VDD = 3.0V |
| | $R_{PU1}$ | - | 80K | - | - | VDD = 4.5V |
| Pull-down Resistor | $R_{PD1}$ | - | 150K | - | - | VDD = 3.0V |
| | $R_{PD1}$ | - | 80K | - | - | VDD = 4.5V |

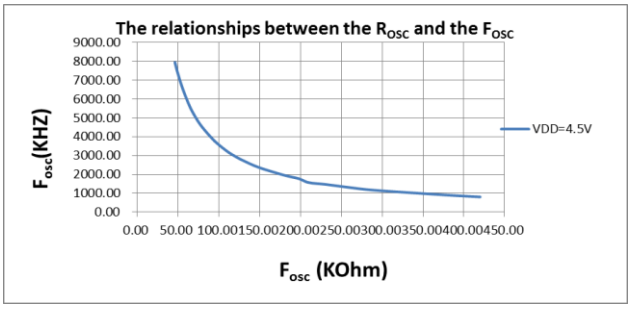
**Note* :** VDD, min may have +-0.1V variation due to process issue.

### 6.3. The Relationships between the $F_{OSC}$ and the $R_{OSC}$

#### 6.3.1. VDD=3V

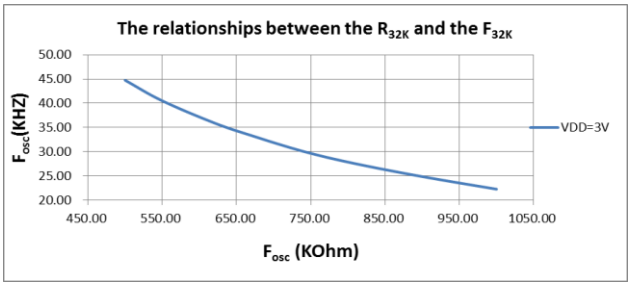



#### 6.3.2. VDD=4.5V

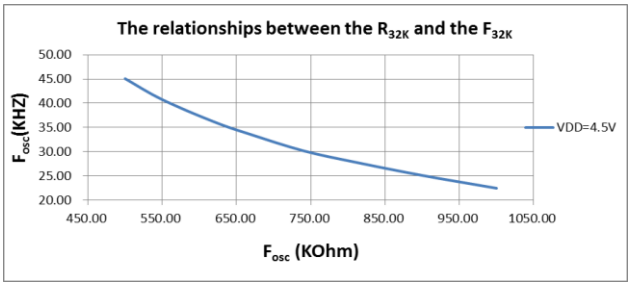


### 6.4. The Relationships between the F32K and the R32K

#### 6.4.1. VDD=3.0V

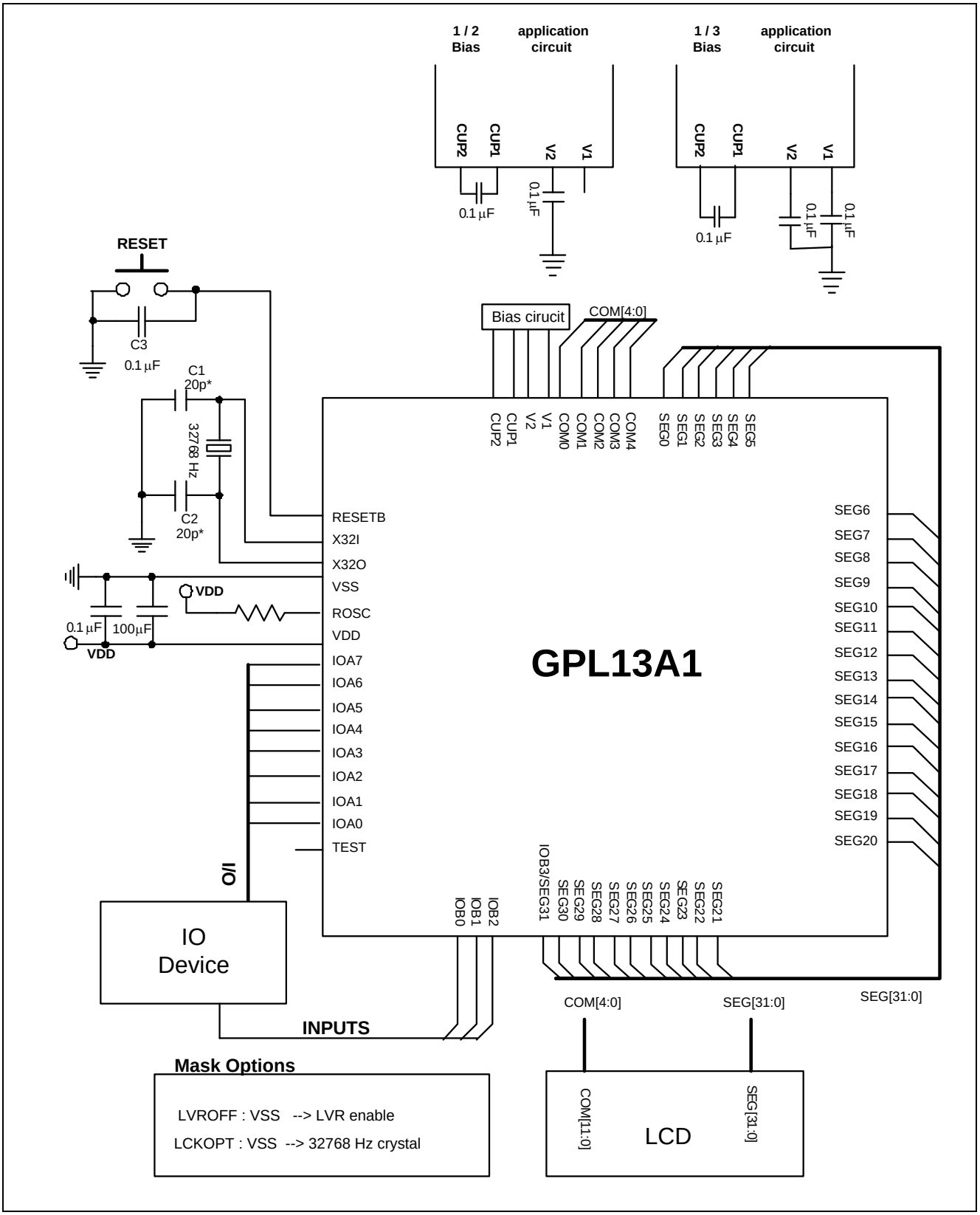



#### 6.4.2. VDD=4.5V



## 7. APPLICATION CIRCUITS

### 7.1. 160 Dots (5 x 32) LCD Driver, 1/2 or 1/3 Bias, R-Oscillator / 32768Hz Crystal




**Note*:** C1/C2 values in above application circuit are for design guidance only. Different capacitor values may be required for different crystals used. Usually, the values of C1/C2 are in the range of 12 ~ 20pF.

## 8. PACKAGE/PAD LOCATIONS

### 8.1. Ordering Information

| Product Number | Package Type |
|---|---|
| GPL13A1 - C | Chip form |

## 9. DISCLAIMER

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## 10. REVISION HISTORY

| Date | Revision # | Description | Page |
|---|---|---|---|
| Jul. 14, 2015 | 1.0 | Generating GPL13A1 Data Sheet | 14 |
| Mar. 18, 2015 | 0.1 | Original. | 13 |