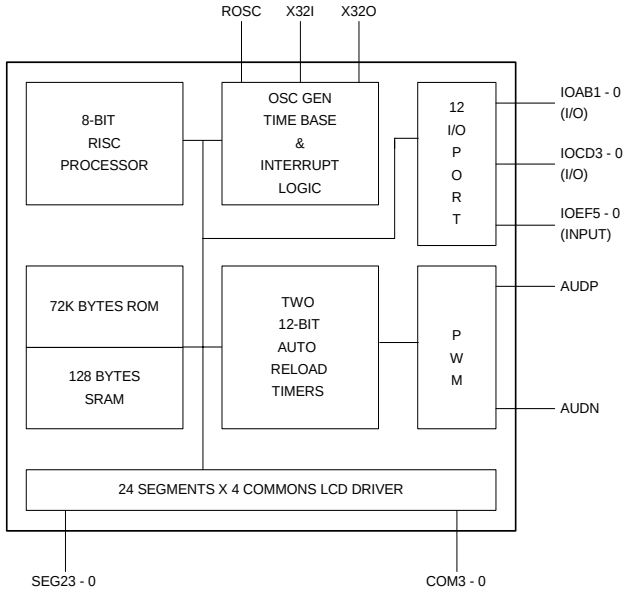
# 72KB LCD CONTROLLER / DRIVER

## 1. GENERAL DESCRIPTION

The GPL15B1 is a CMOS 8-bit single chip microprocessor which contains RAM, ROM, I/Os, interrupt controller, 8-bit PWM audio output and automatic display controller/driver for LCD. For power saving, a software controllable standby switch is also built-in. This chip is implemented with advanced design and process technology. It is very suitable for LCD type handheld products. The ROM space of this chip can be used to store program or audio data. (The speech data is about 18 seconds at 7KHz sampling rate by using 4bit-ADPCM)

## 2. BLOCK DIAGRAM




## 3. FEATURES

- Built-in 8-bit CPU
- 128 bytes SRAM
- 72K bytes ROM
- Max. CPU frequency: 2.0MHz @ 3.0V
- Wide operating voltage: 2.4V - 3.6V
  3.6V - 5.5V
- Built-in 32.768KHz oscillator circuit for real time clock
- Built-in RC oscillator(only one resistor is needed)
- Internal time base generator
- Key wake-up mode
- Provide 7 INT sources
- Operating current: 400μA/600KHz @ 3.0V
- Very low standby current, $I_{STBY}$ < 1μA
- 24 segments x 4 commons LCD driver
- LCD 1/2, 1/3 bias, 1/2, 1/3, 1/4 duty
- Two 12-bit timers
- 6 general I/O pins, 6 input pins
- Provide standby function (stop osc)
- Built-in 8-bit PWM output (directly drive a speaker)

**Note: Patent Circuit Included.**
**Tawain Patent No. 68824.**

## 4. SIGNAL DESCRIPTIONS

| Mnemonic | PIN No. | Type | Description |
|---|---|---|---|
| SEG23 - 0 | 36 - 13 | O | LCD driver segment output |
| COM3 - 0 | 37 - 40 | O | LCD driver common output |
| IOAB1 - 0 | 12 - 11 | I/O | I/O port |
| IOEF5 - 0 | 1 - 6 | I | INPUT port (also for key wake-up input) |
| IOCD3 - 0 | 10 - 7 | I/O | I/O port |
| ROSC | 49 | I | R-osc input, connect to VDD through resistor |
| RESET | 50 | I | System reset input |
| AUDP | 52 | O | PWM Audio output |
| AUDN | 54 | O | PWM Audio output |
| X32I | 48 | I | 32.768KHz crystal input (provide LCD frequency) |
| X32O | 47 | O | 32.768KHz crystal output |
| TEST | 46 | I | Test input |
| VDD | 42, 53 | I | Positive supply voltage input |
| VSS | 51 | I | Ground input |
| VDD1, VDD2 | 43, 41 | I | Inputs for setting LCD bias |
| CUP1, CUP2 | 44, 45 | I | Inputs for setting LCD bias |

## 5. FUNCTIONAL DESCRIPTIONS

### 5.1. ROM Area

GPL15B1 is a large ROM based micro-controller with 96 segments LCD driver. The large ROM can be defined as program ROM, LCD font and audio data continuously without any limitation. To access the ROM area, user should program the BANK SELECT register ($07) first, then access the bank #1 or bank #2 by addressing the higher bank address ($8000 - $FFFF) to fetch the data.

### 5.2. Stop Clock Mode

GPL15B1 supports a power saving mode for those applications needing very low standby current. The user simply enables the wake-up sources to stop the CPU clock by writing the STOP CLOCK register($09). Thus CPU will go to standby mode and the RAM and I/O remain in their previous state until awakened. There are three sources of wake-up in this chip, PORT IOEF wake-up, TIMER 0 wake up and 2 Hz wake up. After the chip is awakened, the internal CPU will go to the RESET state. The RAM and I/O are not affected by this wake-up reset.

### 5.3. Map of Memory and I/Os

*I/O PORT:

— PORT IOAB $0002

IOCD $0003

IOEF $0004

— I/O CONFIG $0000

*NMI SOURCE:

— INT1 (from TIMER 1)

*INT SOURCE

— INT0 (from TIMER 0)

— INT1 (from TIMER 1)

— 2KHz

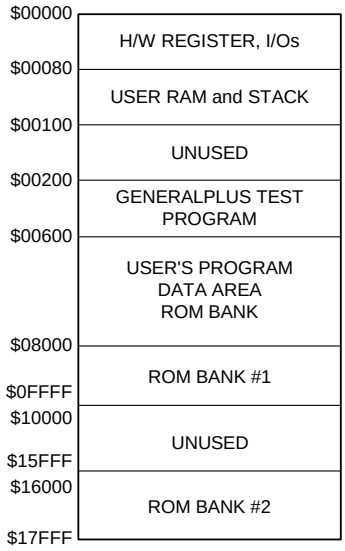
— LCDL (1/3, 1/4 duty 256Hz; 1/2 duty 128Hz)

— 128Hz

— EXT INT

— 2Hz

*MEMORY MAP (ROM view)




### 5.4. Timer/Counter

GPL15B1 contains two 12-bit timer/counters, TM0 and TM1 respectively. In the timer mode, TMA and TMB are reloadable up-counters. When the timer overflows from 0FFF to 0000, the carry signal will generate the INT signal if the corresponding bit is enabled in INT ENABLE register ($0d). The timer will auto reload to the user's preset value and up-count again. If TM0 is specified as a counter, the user can reset the counter by loading 0 into register $14 and $1C. After the counter is activated, the count value can also be read from above registers on-the-fly and the read instruction will not affect the counter's value or reset it.

The clock source of the timer/counter are selected as the following:

| Timer/Counter | | Addr. | Clock Source |
|---|---|---|---|
| TM0 | 12 BIT TIMER | $0014<br>$001C | CPU CLOCK (T) or T/4 |
| | 12 BIT COUNTER | $0014<br>$001C | T/128, T/256, T/2048 or EXT CLK |
| MODE SELECT REGISTER | | $000B | Select TM0 timer or counter |
| TIMER CLOCK SELECTOR | | $001C | Select T or T/4 |

### 5.5. Speech and Melody

Since GPL15B1 could provide large ROM size and wide CPU operation speed, it is most suitable for speech and melody synthesis. For speech synthesis, this chip could provide INT for precise sampling frequency. Users may record or synthesize the sound and digitize it into the ROM. The sound could be played back in the sequence of the control functions as designed by the internal user's program. Several algorithms are suggested to be used for the high fidelity and good compression of sound: PCM, LOG PCM, DM and ADPCM. For melody synthesis, GPL15B1 provides dual tone mode, once entered the dual tone mode, users mere only program the TM0 and TM1 to tone frequency for each channel, count the envelope of each channel, and the hardware may toggle the tone wave automatically without using INT to handle it.

### 5.6. LCD Controller

GPL15B1 contains a total of 96 segments of LCD controller and drivers. In normal operation, the LCD is refreshed by LCDL interrupt. The INT routine will read the number of common patterns which are under service, and send the next common pattern to the LCD port ($10H - $13H) from the RAM buffer. In stop clock mode, the hardware will auto refresh the LCD after writing to OPTION register ($1FH). The LCD driver is designed to fit most LCD specifications in GPL15B1: It can either be programmed as 1/2 or 1/3 bias, The duty is also programmable from 1/2, 1/3 or 1/4 duty.

### 5.7. PWM Output

Internally, GPL15B1 has two set PWMs (one for each channel). GPL15B1 uses Pulse Width Modulation could directly drive speaker or buzzer without any buffer or AMP circuit.

## 6. ELECTRICAL SPECIFICATIONS

### 6.1. Absolute Maximum Ratings

| Characteristics | Symbol | Ratings |
|---|---|---|
| DC Supply Voltage | $V_+$ | < 7.0V |
| Input Voltage Range | $V_{IN}$ | -0.5V to $V_+$ + 0.5V |
| Operating Temperature | $T_A$ | 0℃ to +60℃ |
| Storage Temperature | $T_{STO}$ | -50℃ to +150℃ |

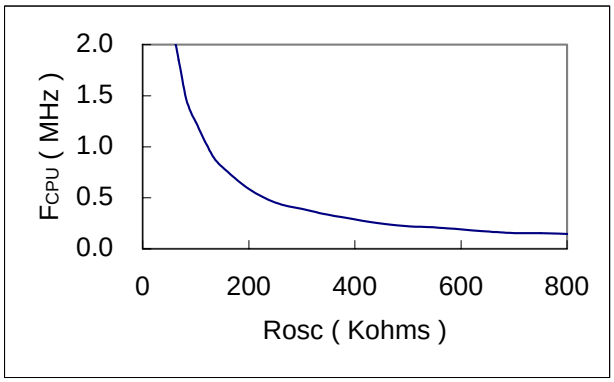
**Note:** Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

### 6.2. DC Characteristics (VDD = 3.0V, $V_{OH}$ = 2.4V, $V_{OL}$ = 0.8V, $T_A$ = 25℃)

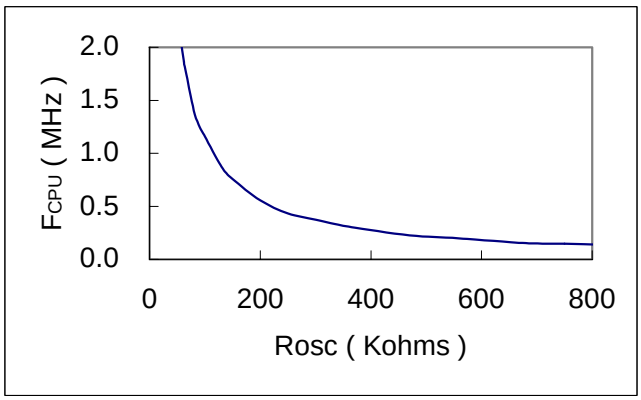
| Characteristics | Symbol | Limit | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operating Voltage | VDD | 2.4 | - | 3.6 | V | For 2-battery |
| | | 3.6 | - | 5.5 | V | For 3-battery |
| Operating Current | $I_{OP}$ | - | 400 | - | μA | $F_{CPU}$ = 1.2MHz @ 3.0V, no load |
| Standby Current | $I_{STBY}$ | - | - | 1.0 | μA | VDD = 3.0V, 32768Hz OFF |
| OSC Frequency | $F_{OSC2}$ | - | - | 4.0 | MHz | VDD = 3.0V |
| Audio Output Current | $I_{OH}$ | - | -16 | - | mA | VDD = 3.0V |
| | $I_{OL}$ | - | 24 | - | mA | VDD = 3.0V |
| Input High Level | $V_{IH}$ | 2.0 | - | - | V | VDD = 3.0V |
| Input Low Level | $V_{IL}$ | - | - | 0.8 | V | VDD = 3.0V |
| Output High I (I/O) | $I_{OH}$ | -200 | - | - | μA | $V_{OH}$ = 2.4V |
| Output Sink I (I/O) | $I_{OL}$ | 500 | - | - | μA | $V_{OL}$ = 0.8V |
| Input Resistor | $R_{IN}$ | - | 50 | - | KΩ | For input only |
| OSC Resistor | $R_{OSC}$ | - | 150 | - | KΩ | $F_{OSC}$ = 1.2MHz @ 3.0V |
| CPU Clock | $F_{CPU}$ | - | - | 2.0 | MHz | $F_{CPU}$ = $F_{OSC}$/2 @ 3.0V |

### 6.3. The Relationship between the $R_{OSC}$ and the $F_{CPU}$

#### 6.3.1. VDD = 3.0V, $T_A$ = 25℃

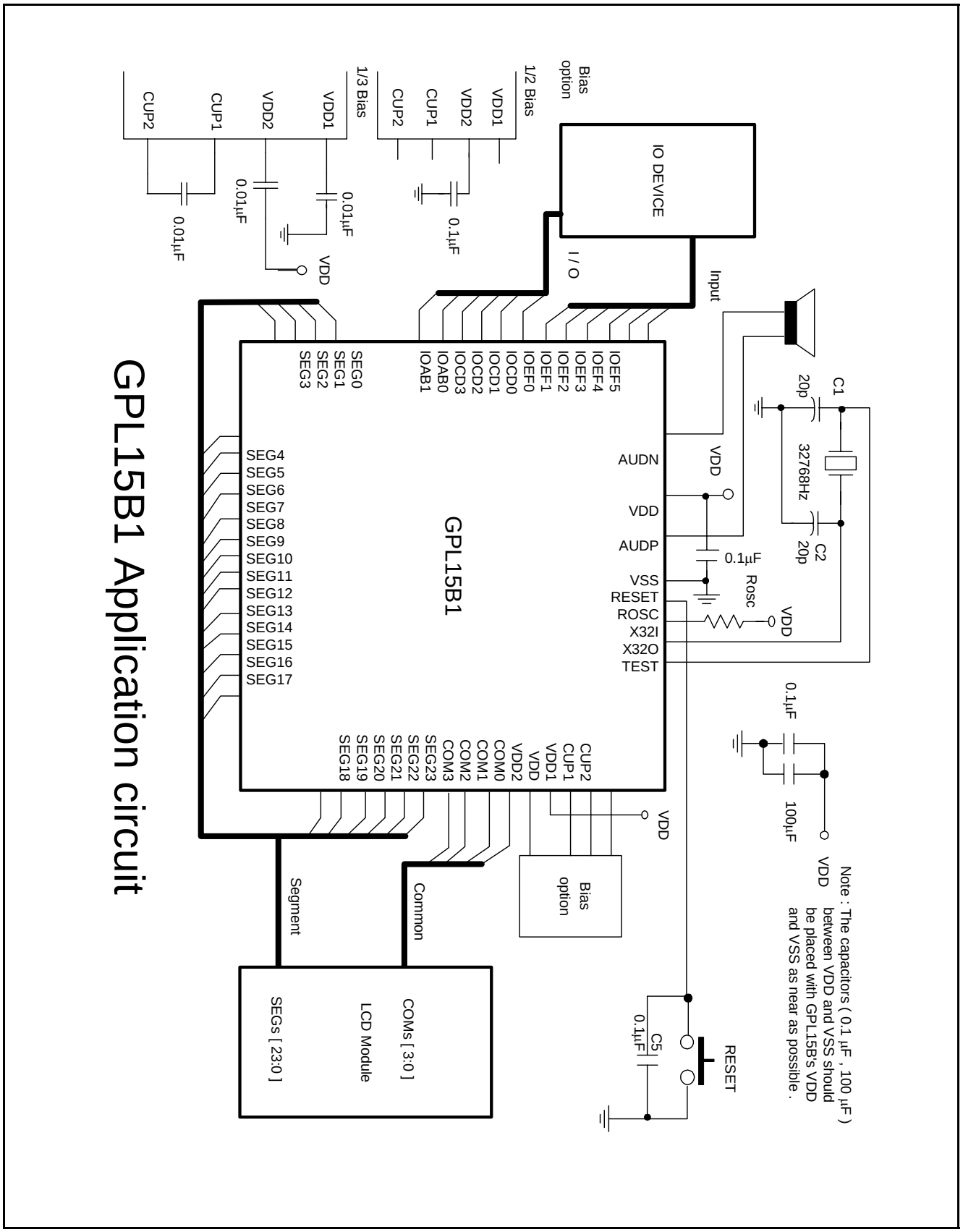



#### 6.3.2. VDD = 4.5V, $T_A$ = 25℃

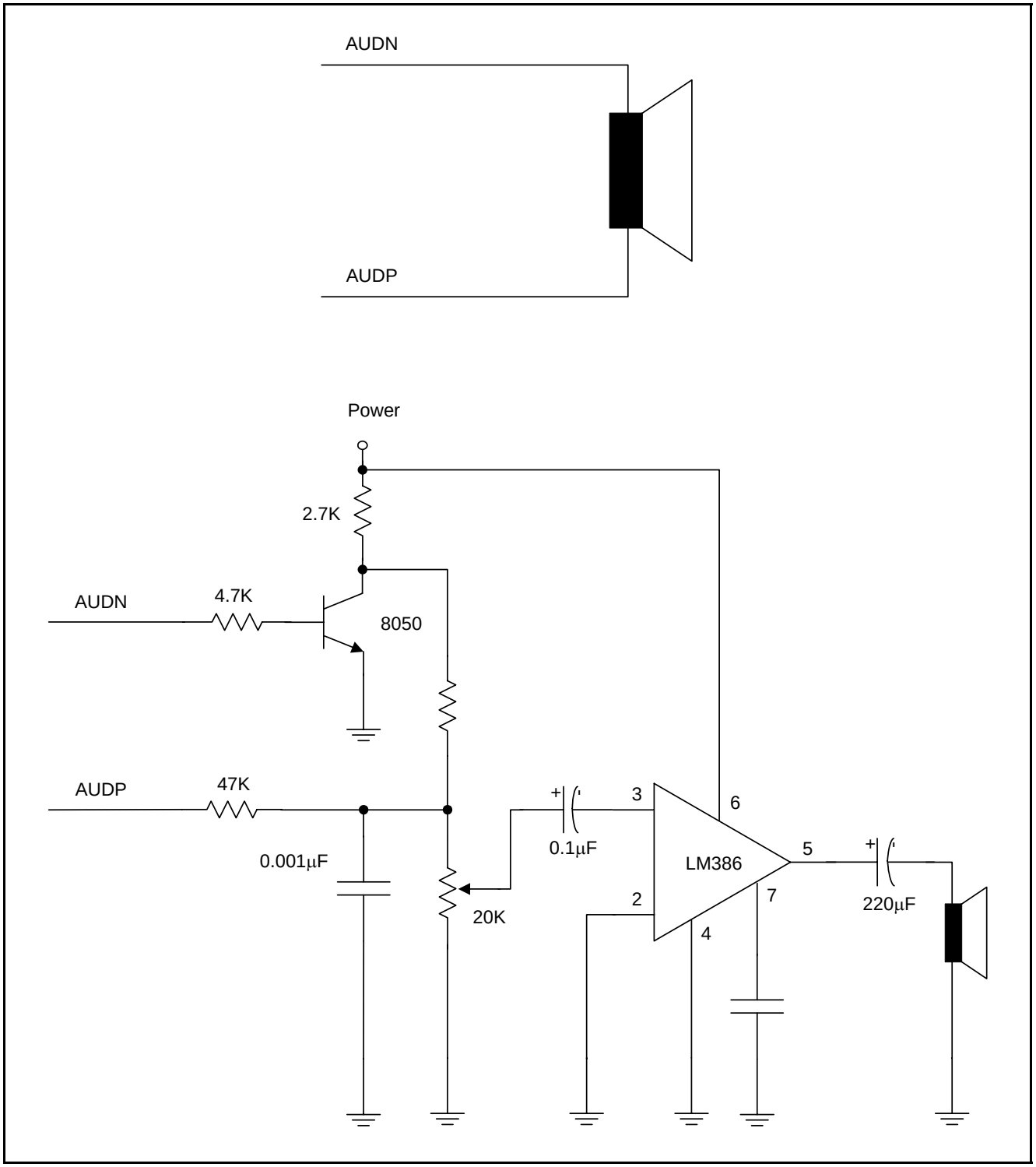


## 7. APPLICATION CIRCUITS

### 7.1. Application Circuit

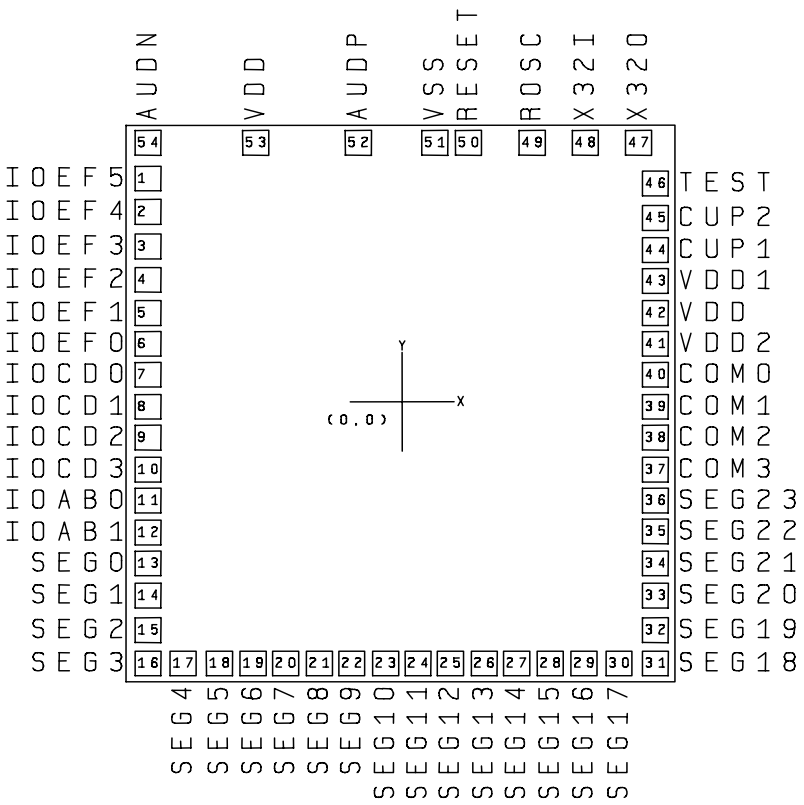


### 7.2. Audio Driver/Amplifier for PWM Mode



## 8. PACKAGE/PAD LOCATIONS

### 8.1. PAD Assignment




This IC substrate should be connected to VSS

**Note1:** The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

### 8.2. Ordering Information

| Product Number | Package Type |
|---|---|
| GPL15B1-NnnV-C | Chip form |

**Note1:** Code number is assigned for customer.

**Note2:** Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

### 8.3. PAD Assignment

| PAD No. | PAD Name | X | Y | PAD No. | PAD Name | X | Y |
|---|---|---|---|---|---|---|---|
| 1 | IOEF5 | -981 | 905 | 28 | SEG15 | 569 | -1061 |
| 2 | IOEF4 | -981 | 768 | 29 | SEG16 | 699 | -1061 |
| 3 | IOEF3 | -981 | 630 | 30 | SEG17 | 837 | -1060 |
| 4 | IOEF2 | -981 | 494 | 31 | SEG18 | 975 | -1060 |
| 5 | IOEF1 | -980 | 361 | 32 | SEG19 | 974 | -924 |
| 6 | IOEF0 | -981 | 235 | 33 | SEG20 | 974 | -787 |
| 7 | IOCD0 | -982 | 108 | 34 | SEG21 | 974 | -654 |
| 8 | IOCD1 | -980 | -20 | 35 | SEG22 | 973 | -527 |
| 9 | IOCD2 | -980 | -146 | 36 | SEG23 | 974 | -400 |
| 10 | IOCD3 | -980 | -274 | 37 | COM3 | 974 | -273 |
| 11 | IOAB0 | -981 | -401 | 38 | COM2 | 974 | -146 |
| 12 | IOAB1 | -981 | -528 | 39 | COM1 | 974 | -19 |
| 13 | SEG0 | -980 | -655 | 40 | COM0 | 974 | 108 |
| 14 | SEG1 | -981 | -787 | 41 | VDD2 | 974 | 235 |
| 15 | SEG2 | -981 | -923 | 42 | VDD | 974 | 361 |
| 16 | SEG3 | -981 | -1060 | 43 | VDD1 | 973 | 489 |
| 17 | SEG4 | -843 | -1061 | 44 | CUP1 | 974 | 614 |
| 18 | SEG5 | -706 | -1060 | 45 | CUP2 | 974 | 747 |
| 19 | SEG6 | -575 | -1061 | 46 | TEST | 974 | 885 |
| 20 | SEG7 | -448 | -1060 | 47 | X32O | 912 | 1052 |
| 21 | SEG8 | -320 | -1060 | 48 | X32I | 705 | 1052 |
| 22 | SEG9 | -193 | -1060 | 49 | ROSC | 498 | 1051 |
| 23 | SEG10 | -67 | -1060 | 50 | RESET | 257 | 1052 |
| 24 | SEG11 | 60 | -1060 | 51 | VSS | 125 | 1051 |
| 25 | SEG12 | 187 | -1061 | 52 | AUDP | -170 | 1052 |
| 26 | SEG13 | 315 | -1061 | 53 | VDD | -564 | 1051 |
| 27 | SEG14 | 441 | -1060 | 54 | AUDN | -980 | 1052 |

## 9. DISCLAIMER

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## 10. REVISION HISTORY

| Date | Revision # | Description | Page |
|---|---|---|---|
| MAR. 23, 2005 | 1.0 | Original<br>Note: The GPL15B1 data sheet v1.0 is a continued version of SPL15B1 data sheet v1.2. | 11 |